

# TUSB544 USB TYPE-C™ 8.1 Gbps Multi-Protocol Linear Redriver

## 1 Features

- Protocol Agnostic Reversible 4 Channel Linear Redriver Supporting up to 8.1 Gbps
- Supports USB Type-C with USB 3.1 Gen1 and DisplayPort 1.4 as Alternate Mode.
- Supports Processors with USB 3.1 and DisplayPort Mux Integrated for Type-C Applications
- Supports Signal Conditioning Inside Type-C Cable
- Cross-Point Mux for SBU Signals
- GPIO and I<sup>2</sup>C Control for Channel Direction and Equalization
- Advanced Power Management by Monitoring USB Power States and Snooping DP Link Training
- Linear Equalization up to 11 dB at 4.05 GHz
- Configuration through GPIO or I<sup>2</sup>C
- Hot-Plug Capable
- Single 3.3 V Supply
- Industrial Temperature: -40°C to 85°C TUSB544I
- Commercial Temperature: 0°C to 70°C TUSB544
- 4 mm x 6 mm, 0.4 mm Pitch, 40-pin QFN Package

## 2 Applications

- Tablets
- Notebooks
- Desktops
- Docking Stations

## 3 Description

The TUSB544 is a USB Type-C Alt Mode redriver switch supporting data rates up to 8.1 Gbps. This protocol-agnostic linear redriver is capable of supporting USB Type-C Alt Mode interfaces including DisplayPort.

The TUSB544 provides several levels of receive linear equalization to compensate for cable and board trace loss due to inter symbol interference (ISI). Operates on a single 3.3 V supply and comes in a commercial and industrial temperature range.

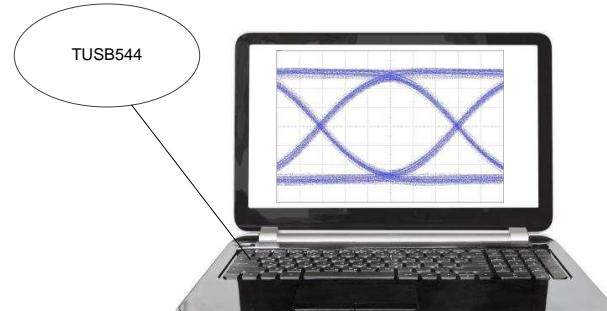
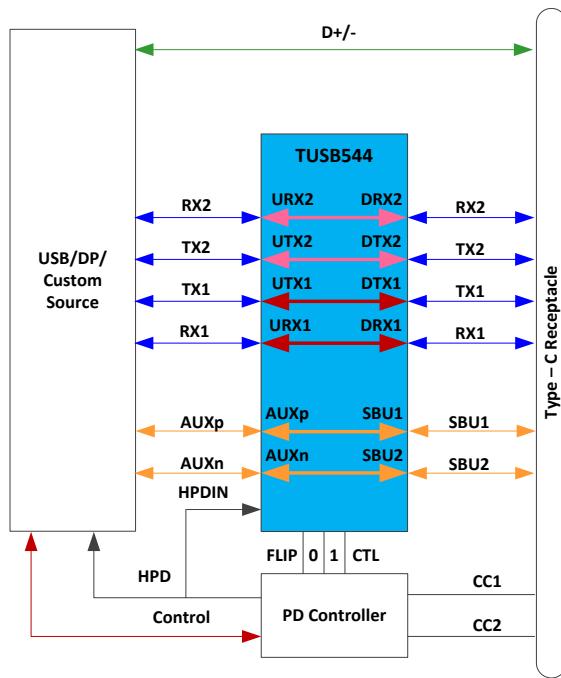
All four lanes of the TUSB544 are reversible making it a versatile signal conditioner that can be used in many applications.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB544		
TUSB544I	WQFN (40)	4.00 mm x 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## Simplified Schematic



Copyright © 2017, Texas Instruments Incorporated



An **IMPORTANT NOTICE** at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. **PRODUCTION DATA**.

## Table of Contents

<b>1</b>	<b>Features</b>	<b>1</b>	7.4	Device Functional Modes	18
<b>2</b>	<b>Applications</b>	<b>1</b>	7.5	Programming	29
<b>3</b>	<b>Description</b>	<b>1</b>	7.6	Register Maps	30
<b>4</b>	<b>Revision History</b>	<b>2</b>	<b>8</b>	<b>Application and Implementation</b>	<b>39</b>
<b>5</b>	<b>Pin Configuration and Functions</b>	<b>3</b>	8.1	Application Information	39
<b>6</b>	<b>Specifications</b>	<b>5</b>	8.2	Typical Application	39
6.1	Absolute Maximum Ratings	5	8.3	System Examples	43
6.2	ESD Ratings	5	<b>9</b>	<b>Power Supply Recommendations</b>	<b>50</b>
6.3	Recommended Operating Conditions	5	<b>10</b>	<b>Layout</b>	<b>51</b>
6.4	Thermal Information	6	10.1	Layout Guidelines	51
6.5	Power Supply Characteristics	6	10.2	Layout Example	51
6.6	DC Electrical Characteristics	6	<b>11</b>	<b>Device and Documentation Support</b>	<b>52</b>
6.7	AC Electrical Characteristics	7	11.1	Documentation Support	52
6.8	Timing Requirements	9	11.2	Receiving Notification of Documentation Updates	52
6.9	Switching Characteristics	9	11.3	Community Resources	52
6.10	Typical Characteristics	12	11.4	Trademarks	52
<b>7</b>	<b>Detailed Description</b>	<b>15</b>	11.5	Electrostatic Discharge Caution	52
7.1	Overview	15	11.6	Glossary	52
7.2	Functional Block Diagram	16	<b>12</b>	<b>Mechanical, Packaging, and Orderable</b>	<b>52</b>
7.3	Feature Description	17	<b>Information</b>		

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision A (April 2017) to Revision B

**Page**

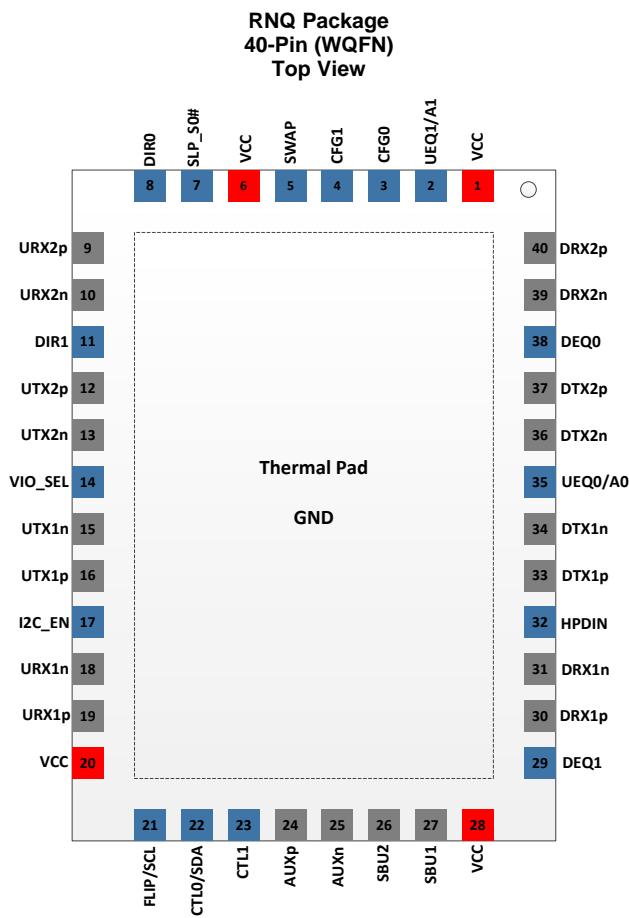
• Added a MIN value of 0.5 pF to $C_{L12C}$ in the <i>DC Electrical Characteristics</i> table .....	7
• Changed $V_{RX-DC-CM}$ , deleted the MIN and MAX values and added TYP = 0 V in the <i>AC Electrical Characteristics</i> table.....	7
• Changed $EQ_{SS}$ Description From: "Receiver equalization" To: "Receiver equalization at maximum setting" in the <i>AC Electrical Characteristics</i> table .....	7
• Changed $EQ_{SS}$ From: MAX = 9.8 dB To: MAX = 9 dB in the <i>AC Electrical Characteristics</i> table .....	7
• Changed $V_{TX-DC-CM}$ , deleted the MIN and MAX values and added TYP = 1.75 V in the <i>AC Electrical Characteristics</i> table .	7
• Changed $RL_{TX-DIFF}$ From: TYP = -14 dB To: TYP = -13 dB in the <i>AC Electrical Characteristics</i> table.....	8
• Changed $RL_{TX-CM}$ From: TYP = -13 dB To: TYP = -11 dB in the <i>AC Electrical Characteristics</i> table .....	8
• Changed $G_{LF}$ From: MAX = 2.5 dB To: MAX = 1 dB in the <i>AC Electrical Characteristics</i> table .....	8
• Changed $V_{IC}$ , deleted the MIN and MAX values and added TYP = 0 V in the <i>AC Electrical Characteristics</i> table .....	8
• Changed the $EQ_{DP}$ entry in the <i>AC Electrical Characteristics</i> table .....	8
• Changed $V_{TX(DC-CM)}$ , deleted the MIN and MAX values and added TYP = 1.75 V in the <i>AC Electrical Characteristics</i> table	8
• Changed the $t_{IDLEExit\_DISC}$ value From: TYP = 10 $\mu$ s To TYP = 15 ms in the <i>Timing Requirements</i> table.....	9
• Changed the $t_{CTRL1\_DEBOUNCE}$ value From: MIN = 2 ms To: MIN = 3 ms in the <i>Switching Characteristics</i> table .....	9

### Changes from Original (April 2017) to Revision A

**Page**

• Changed SUB1, SUB2, AUXn, and AUXp pin labels on the Sink side of <a href="#">Figure 45</a> .....	47
• Changed SUB1, SUB2, AUXn, and AUXp pin labels on the Sink side of <a href="#">Figure 46</a> .....	47

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VCC	P	3.3 V Power Supply
2	UEQ1/A1	4 Level I	This pin along with UEQ0 sets the high-frequency equalizer gain for upstream facing URX1, URX2, UTX1, UTX2 receivers. Up to 9.4 dB of EQ available. When I2C_EN =0, this pin will also set TUSB544 I2C address. Refer to <a href="#">Table 10</a> .
3	CFG0	4 Level I	CFG0. This pin along with CFG1 will select VOD linearity range and DC gain for all the downstream and upstream channels. Refer to <a href="#">Table 8</a> for VOD linearity range and DC gain options.
4	CFG1	4 Level I	CFG1. This pin along with CFG0 will set VOD linearity range and DC gain for all the downstream and upstream channels. Refer to <a href="#">Table 8</a> for VOD linearity range and DC gain options.
5	SWAP	2 Level I	This pin swaps all the channel directions and EQ settings of downstream facing and upstream facing data path inputs. 0 – Do not swap channel directions and EQ settings (Default) 1. – Swap channel directions and EQ settings.
6	VCC	P	3.3V Power Supply
7	SLP_S0#	2 Level I	This pin when asserted low will disable Receiver Detect functionality. While this pin is low and TUSB544 is in U2/U3, TUSB544 will disable LOS and LFPS detection circuitry and RX termination for both channels will remain enabled. If this pin is low and TUSB544 is in Disconnect state, the RX detect functionality will be disabled and RX termination for both channels will be disabled. 0 – RX Detect disabled 1 – RX Detect enabled (Default)
8	DIR0	2 Level I	This pin along with DIR1 sets the data path signal direction format. Refer to <a href="#">Table 4</a> for signal direction formats.
9	URX2p	Diff I/O	Differential positive input/output for upstream facing RX2 port.
10	URX2n	Diff I/O	Differential negative input/output for upstream facing RX2 port.

## Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
11	DIR1	2 Level I/O	This pin along with DIR0 sets the data path signal direction format. Refer to <a href="#">Table 4</a> for signal direction formats.
12	UTX2p	Diff I/O	Differential positive input/output for upstream facing TX2 port.
13	UTX2n	Diff I/O	Differential negative input/output for upstream facing TX2 port.
14	VIO_SEL	4 Level I/O	This pin selects I/O voltage levels for the GPIO configuration pins and the I <sup>2</sup> C interface: 0 = 3.3-V configuration I/O voltage, 3.3-V I <sup>2</sup> C interface (Default) R = 3.3-V configuration I/O voltage, 1.8-V I <sup>2</sup> C interface F = 1.8-V configuration I/O voltage, 3.3-V I <sup>2</sup> C interface 1 = 1.8-V configuration I/O voltage, 1.8-V I <sup>2</sup> C interface.
15	UTX1n	Diff I/O	Differential negative input/output for upstream facing TX1 port.
16	UTX1p	Diff I/O	Differential positive input/output for upstream facing TX1 port.
17	I <sup>2</sup> C_EN	4 Level I	I <sup>2</sup> C Programming or Pin Strap Programming Select. 0 = GPIO Mode (I <sup>2</sup> C disabled) R = TI Test Mode (I <sup>2</sup> C enabled) F = GPIO Mode, AUX Snoop Disabled (I <sup>2</sup> C disabled) 1 = I <sup>2</sup> C enabled.
18	URX1n	Diff I/O	Differential negative input/output for upstream facing RX1 port.
19	URX1p	Diff I/O	Differential positive input/output for upstream facing RX1 port.
20	VCC	P	3.3V Power Supply
21	FLIP/SCL	2 Level I (Failsafe)	When I <sup>2</sup> C_EN='0' this is Flip control pin, otherwise this pin is I <sup>2</sup> C clock.
22	CTL0/SDA	2 Level I (Failsafe)	When I <sup>2</sup> C_EN='0' this is a USB3.1 Switch control pin, otherwise this pin is I <sup>2</sup> C data.
23	CTL1	2 Level I (PD)	DP Alt mode Switch Control Pin. When I <sup>2</sup> C_EN = '0', this pin will enable or disable DisplayPort functionality. Otherwise DisplayPort functionality is enabled and disabled through I <sup>2</sup> C registers. L = DisplayPort Disabled. H = DisplayPort Enabled. When I <sup>2</sup> C_EN = 0, this pin is not used by device.
24	AUXp	I/O, CMOS	AUXp. DisplayPort AUX positive I/O connected to the DisplayPort source or sink through an AC coupling capacitor. In addition to AC coupling capacitor, this pin also requires a 100-kΩ resistor to GND between the AC coupling capacitor and the AUXp pin if the TUSB544 is used on the DisplayPort source side, or a 1-MΩ resistor to DP_PWR (3.3V) between the AC coupling capacitor and the AUXp pin if TUSB544 is used on the DisplayPort sink side. This pin along with AUXn is used by the TUSB544 for AUX snooping and is routed to SBU1/2 based on the orientation of the Type-C plug.
25	AUXn	I/O, CMOS	AUXn. DisplayPort AUX I/O connected to the DisplayPort source or sink through an AC coupling capacitor. In addition to AC coupling capacitor, this pin also requires a 100-kΩ resistor to DP_PWR (3.3V) between the AC coupling capacitor and the AUXn pin if the TUSB544 is used on the DisplayPort source side, or a 1-MΩ resistor to GND between the AC coupling capacitor and the AUXn pin if TUSB544 is used on the DisplayPort sink side. This pin along with AUXp is used by the TUSB544 for AUX snooping and is routed to SBU1/2 based on the orientation of the Type-C plug.
26	SBU2	I/O, CMOS	SBU2. When the TUSB544 is used on the DisplayPort source side, this pin should be DC coupled to the SBU2 pin of the Type-C receptacle. When the TUSB544 is used on the DisplayPort sink side, this pin should be DC coupled to the SBU1 pin of the Type-C receptacle. A 2-MΩ resistor to GND is also recommended.
27	SBU1	I/O, CMOS	SBU1. When the TUSB544 is used on the DisplayPort source side, this pin should be DC coupled to the SBU1 pin of the Type-C receptacle. When the TUSB544 is used on the DisplayPort sink side, this pin should be DC coupled to the SBU2 pin of the Type-C receptacle. A 2-MΩ resistor to GND is also recommended.
28	VCC	P	3.3V Power Supply
29	DEQ1	4 Level I	This pin along with DEQ0 sets the high-frequency equalizer gain for downstream facing DRX1, DRX2, DTX1, DTX2 receivers. Up to 11 dB of EQ available.
30	DRX1p	Diff I/O	Differential positive input/output for downstream facing RX1 port.
31	DRX1n	Diff I/O	Differential negative input/output for downstream facing RX1 port.
32	HPDIN	2 Level I (PD)	When I <sup>2</sup> C_EN = 0, this pin is an input for Hot Plug Detect received from DisplayPort sink. When HPDIN is Low for greater than 2ms, all DisplayPort lanes are disabled and AUX to SBU switch will remain closed.
33	DTX1p	Diff I/O	Differential positive input/output for downstream facing TX1 port.
34	DTX1n	Diff I/O	Differential negative input/output for downstream facing TX1 port.
35	UEQ0/A0	4 Level I	This pin along with UEQ1 sets the high-frequency equalizer gain for upstream facing URX1, URX2, UTX1, UTX2 receivers. Up to 9.4 dB of EQ available. When I <sup>2</sup> C_EN !=0, this pin will also set TUSB544's I <sup>2</sup> C address. Refer to <a href="#">Table 10</a> .
36	DTX2n	Diff I/O	Differential negative input/output for downstream facing TX2 port.

### Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
37	DTX2p	Diff I/O	Differential positive input/output for downstream facing TX2 port.
38	DEQ0	4 Level I	This pin along with DEQ1 sets the high-frequency equalizer gain for downstream facing URX1, URX2, UTX1, UTX2 receivers. Up to 11 dB of EQ available.
39	DRX2n	Diff I/O	Differential negative input/output for downstream facing RX2 port.
40	DRX2p	Diff I/O	Differential positive input/output for downstream facing RX2 port.
Thermal Pad		GND	Ground

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply Voltage	V <sub>CC</sub>	-0.3	4	V
Voltage Range at any input or output pin	Differential voltage between positive and negative inputs	-2.5	2.5	V
	Voltage at differential inputs	-0.5	V <sub>CC</sub> + 0.5	V
	CMOS Inputs	-0.5	V <sub>CC</sub> + 0.5	V
Maximum junction temperature, T <sub>J</sub>			125	°C
Storage temperature, T <sub>STG</sub>		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±6	kV
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT	
V <sub>CC</sub>	Main power supply	3	3.3	3.6	V	
	Supply ramp requirement			100	ms	
V <sub>I2C</sub>	Supply that external resistors on SDA and SCL are pulled up to.	1.70		3.6	V	
V <sub>PSN</sub>	Supply Noise on V <sub>CC</sub> terminals			100	mV	
T <sub>A</sub>	Operating free-air temperature		TUSB544	0	70	°C
			TUSB544I	-40	85	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TUSB544	UNIT
		RNQ (QFN)	
		40 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	37.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	20.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	9.5	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.2	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	9.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	2.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Power Supply Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
P <sub>CC-ACTIVE-USB</sub>	Average active power USB Only	Link in U0 with GEN1 data transmission. EQ control pins = NC, K28.5 pattern at 5 Gbps, V <sub>ID</sub> = 1000 mV <sub>p-p</sub> ; VOD Linearity = 900 mV <sub>p-p</sub> ; CTL1 = L; CTL0 = H		297		mW
P <sub>CC-ACTIVE-USB-DP1</sub>	Average active power USB + 2 Lane DP	Link in U0 with GEN1 data transmission. EQ control pins = NC, K28.5 pattern at 5 Gbps, V <sub>ID</sub> = 1000 mV <sub>p-p</sub> ; VOD Linearity = 900 mV <sub>p-p</sub> ; CTL1 = H; CTL0 = H		578		mW
P <sub>CC-ACTIVE-USB-CUSTOM</sub>	Average active power USB + 2 Channel Custom Alt Mode	Link in U0 with GEN1 data transmission. EQ control pins = NC, K28.5 pattern at 5 Gbps, V <sub>ID</sub> = 1000 mV <sub>p-p</sub> ; VOD Linearity = 900 mV <sub>p-p</sub> ; CTL1 = H; CTL0 = H		578		mW
P <sub>CC-Active-DP</sub>	Average active power 4 Lane DP Only	Four active DP lanes operating at 8.1 Gbps; EQ control pins = NC, K28.5 pattern at 5 Gbps, V <sub>ID</sub> = 1000 mV <sub>p-p</sub> ; VOD Linearity = 900 mV <sub>p-p</sub> ; CTL1 = H; CTL0 = L;		564		mW
P <sub>CC-NC-USB</sub>	Average power with no connection	No GEN1 device is connected to TXP/TXN; CTL1 = L; CTL0 = H;		2.5		mW
P <sub>CC-U2U3</sub>	Average power in U2/U3	Link in U2 or U3 USB Mode Only; CTL1 = L; CTL0 = H;		2.0		mW
P <sub>CC-SHUTDOWN</sub>	Device Shutdown	CTL1 = L; CTL0 = L; I <sub>2C_EN</sub> = 0;		0.65		mW

## 6.6 DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>4-State CMOS Inputs(UEQ[1:0];DEQ[1:0], CFG[1:0], A[1:0], I<sub>2C_EN</sub>, V<sub>IO_SEL</sub>)</b>					
I <sub>IH</sub>	High level input current	V <sub>CC</sub> = 3.6 V <sub>IN</sub> = 3.6 V	20	80	µA
I <sub>IL</sub>	Low level input current	V <sub>CC</sub> = 3.6 V; V <sub>IN</sub> = 0 V	-160	-40	µA
4-Level V <sub>TH</sub>	Threshold 0 / R	V <sub>CC</sub> = 3.3 V		0.55	V
	Threshold R/ Float	V <sub>CC</sub> = 3.3 V		1.65	V
	Threshold Float / 1	V <sub>CC</sub> = 3.3 V		2.7	V
R <sub>PU</sub>	Internal pull-up resistance			35	kΩ
R <sub>PD</sub>	Internal pull-down resistance			95	kΩ
<b>2-State CMOS Input (CTL0, CTL1, FLIP, HPDIN, SLP_S0#, SWAP, DIR[1:0]).</b>					
V <sub>IH</sub>	High-level input voltage		0.7×V <sub>IO</sub>	3.6	V
V <sub>IL</sub>	Low-level input voltage		0	0.3×V <sub>IO</sub>	V
R <sub>PD</sub>	Internal pull-down resistance for CTL1			500	kΩ
I <sub>IH</sub>	High-level input current	V <sub>IN</sub> = 3.6 V	-25	25	µA
I <sub>IL</sub>	Low-level input current	V <sub>IN</sub> = GND, V <sub>CC</sub> = 3.6 V	-25	25	µA
<b>I<sup>2</sup>C Control Pins SCL, SDA</b>					

## DC Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IH}$	High-level input voltage	$0.7 \times V_{I2C}$		3.6	V
$V_{IL}$	Low-level input voltage	$I2C\_EN = 0$	0	$0.3 \times V_{I2C}$	V
$V_{OL}$	Low-level output voltage	$I2C\_EN = 0; I_{OL} = 3 \text{ mA}$	0	0.4	V
$I_{OL}$	Low-level output current	$I2C\_EN = 0; V_{OL} = 0.4 \text{ V}$	20		mA
$I_{I2C}$	Input current on SDA pin	$0.1 \times V_{I2C} < \text{Input voltage} < 3.3 \text{ V}$	-10	10	$\mu\text{A}$
$C_{I2C}$	Input capacitance		0.5	10	pF

## 6.7 AC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>USB Gen 1 Differential Receiver (UTX1P/N, UTX2P/N, DRX1P/N, DRX2P/N)</b>					
$V_{RX-DIFF-PP}$	Input differential peak-peak voltage swing linear dynamic range	AC-coupled differential peak-to-peak signal measured post CTLE through a reference channel		2000	mVpp
$V_{RX-DC-CM}$	Common-mode voltage bias in the receiver (DC)			0	V
$R_{RX-DIFF-DC}$	Differential input impedance (DC)	Present after a GEN1 device is detected on receiver pins	72	120	$\Omega$
$R_{RX-CM-DC}$	Receiver DC common mode impedance	Present after a GEN1 device is detected on receiver pins	18	30	$\Omega$
$Z_{RX-HIGH-IMP-DC-POS}$	Common-mode input impedance with termination disabled (DC)	Present when no GEN1 device is detected on receiver pins. Measured over the range of 0-500mV with respect to GND.	25		k $\Omega$
$V_{SIGNAL-DET-DIFF-PP}$	Input differential peak-to-peak signal detect assert level	At 5 Gbps, no loss at the input, PRBS7 pattern		80	mV
$V_{RX-IDLE-DET-DIFF-PP}$	Input differential peak-to-peak signal detect de-assert Level	At 5 Gbps, no loss at the input, PRBS7 pattern		60	mV
$V_{RX-LFPS-DET-DIFF-PP}$	Low frequency periodic signaling (LFPS) detect threshold	Below the minimum is squelched.	100	300	mV
$V_{RX-CM-AC-P}$	Peak RX AC common-mode voltage	Measured at package pin		150	mV
$C_{RX}$	RX input capacitance to GND	At 2.5 GHz		0.5	pF
$RL_{RX-DIFF}$	Differential return Loss	50 MHz – 1.25 GHz at 90 $\Omega$		-16	dB
		2.5 GHz at 90 $\Omega$		-14	dB
$RL_{RX-CM}$	Common-mode return loss	50 MHz – 2.5 GHz at 90 $\Omega$		-13	dB
$EQ_{SS}$	Receiver equalization at maximum setting	UEQ[1:0] and DEQ[1:0]. at 2.5 GHz		9	dB
<b>USB Gen 1 Differential Transmitter (DTX1P/N, DTX2P/N, URX1P/N, URX2P/N)</b>					
$V_{TX-DIFF-PP}$	Transmitter dynamic differential voltage swing range.		1600		mV <sub>PP</sub>
$V_{TX-RCV-DETECT}$	Amount of voltage change allowed during receiver detection			600	mV
$V_{TX-CM-IDLE-DELTA}$	Transmitter idle common-mode voltage change while in U2/U3 and not actively transmitting LFPS	-600		600	mV
$V_{TX-DC-CM}$	Common-mode voltage bias in the transmitter (DC)		1.75		V
$V_{TX-CM-AC-PP-ACTIVE}$	Tx AC common-mode voltage active	Max mismatch from Txp + Txn for both time and amplitude		100	mV <sub>PP</sub>
$V_{TX-IDLE-DIFF-AC-PP}$	AC electrical idle differential peak-to-peak output voltage	At package pins	0	10	mV
$V_{TX-IDLE-DIFF-DC}$	DC electrical idle differential output voltage	At package pins after low pass filter to remove AC component	0	14	mV
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute DC common-mode voltage between U1 and U0	At package pin		200	mV
$R_{TX-DIFF}$	Differential impedance of the driver		75	120	$\Omega$
$C_{AC-COUPLING}$	AC coupling capacitor		75	265	nF
$R_{TX-CM}$	Common-mode impedance of the driver	Measured with respect to AC ground over 0–500 mV	18	30	$\Omega$

## AC Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{TX\text{-SHORT}}$	TX short circuit current	TXP/N shorted to GND			67	mA
$RL_{TX\text{-DIFF}}$	Differential return loss	50 MHz – 1.25 GHz at 90 $\Omega$		-16		dB
		2.5 GHz at 90 $\Omega$		-13		dB
$RL_{TX\text{-CM}}$	Common-mode return loss	50 MHz – 2.5 GHz at 90 $\Omega$		-11		dB
<b>AC Characteristics</b>						
Crosstalk	Differential crosstalk between any signal pairs	at 4.05 GHz		-30		dB
$G_{LF}$	Low frequency voltage gain	at 10 MHz, 200 mV <sub>PP</sub> < $V_{ID}$ < 2000 mV <sub>PP</sub> ; 0-dB low-frequency gain setting	-1	0	1	dB
$CP_{1\text{dB-LF}}$	Low frequency 1-dB compression point	at 10 MHz, 200 mV <sub>PP</sub> < $V_{ID}$ < 2000 mV <sub>PP</sub> ; VOD linearity setting = 1100mV <sub>PP</sub>		1100		mV <sub>PP</sub>
$CP_{1\text{dB-HF}}$	High frequency 1-dB compression point	at 4.05 GHz, 200 mV <sub>PP</sub> < $V_{ID}$ < 2000 mV <sub>PP</sub> ; VOD linearity setting = 1100mV <sub>PP</sub>		1200		mV <sub>PP</sub>
$f_{LF}$	Low frequency cutoff	200 mV <sub>PP</sub> < $V_{ID}$ < 2000 mV <sub>PP</sub>		25	50	kHz
DJ	TX output deterministic jitter		200 mV <sub>PP</sub> < $V_{ID}$ < 2000 mV <sub>PP</sub> , PRBS7, 5 Gbps		0.05	Ulpp
	200 mV <sub>PP</sub> < $V_{ID}$ < 2000 mV <sub>PP</sub> , PRBS7, 8.1 Gbps			0.08	Ulpp	
TJ	TX output total jitter		200 mV <sub>PP</sub> < $V_{ID}$ < 2000 mV <sub>PP</sub> , PRBS7, 5 Gbps		0.08	Ulpp
	200 mV <sub>PP</sub> < $V_{ID}$ < 2000 mV <sub>PP</sub> , PRBS7, 8.1 Gbps			0.135	Ulpp	
<b>DisplayPort Receiver UTX1P/N, UTX2P/N, URX1P/N, URX2P/N</b>						
$V_{ID\_PP}$	Peak-to-peak input differential dynamic voltage range			2000		mV <sub>PP</sub>
$V_{IC}$	Input common mode voltage			0		V
$C_{AC}$	AC coupling capacitance		75		200	nF
$EQ_{DP}$	Receiver equalizer at maximum setting	DEQ[1:0],UEQ[1:0] at 4.05 GHz		9.5		dB
$d_R$	Data rate	HBR3			8.1	Gbps
$R_{ti}$	Input termination resistance		80	100	120	$\Omega$
<b>DisplayPort Transmitter DTX1P/N, DTX2P/N, DRX1P/N, DRX2P/N</b>						
$V_{TX\text{-DIFFPP}}$	VOD dynamic range			1500		mV
$I_{TX\text{-SHORT}}$	TX short circuit current	TXP/N shorted to GND			67	mA
$V_{TX\text{(DC-CM)}}$	Common-mode voltage bias in the transmitter (DC)			1.75		V
<b>AUXP/N and SBU1/2</b>						
$R_{ON}$	Output ON resistance	$V_{CC} = 3.3$ V; $V_I = 0$ to 0.4 V for AUXP; $V_I = 2.7$ V to 3.6 V for AUXN		5	10	$\Omega$
$\Delta R_{ON}$	ON resistance mismatch within pair	$V_{CC} = 3.3$ V; $V_I = 0$ to 0.4V for AUXP; $V_I = 2.7V$ to 3.6V for AUXN			1	$\Omega$
$R_{ON\_FLAT}$	ON resistance flatness ( $R_{ON\text{ max}} - R_{ON\text{ min}}$ ) measured at identical $V_{CC}$ and temperature	$V_{CC} = 3.3$ V; $V_I = 0$ to 0.4V for AUXP; $V_I = 2.7V$ to 3.6 V for AUXN			2	$\Omega$
$V_{AUXP\_DC\_CM}$	AUX Channel DC common mode voltage for AUXP and SBU1.	$V_{CC} = 3.3$ V	0		0.4	V
$V_{AUXN\_DC\_CM}$	AUX Channel DC common mode voltage for AUXN and SBU2	$V_{CC} = 3.3$ V	2.7		3.6	V
$C_{AUX\_ON}$	ON-state capacitance	$V_{CC} = 3.3V$ ; CTL1 = 1; $V_I = 0V$ or 3.3V		4	7	pF
$C_{AUX\_OFF}$	OFF-state capacitance	$V_{CC} = 3.3V$ ; CTL1 = 0; $V_I = 0V$ or 3.3V		3	6	pF

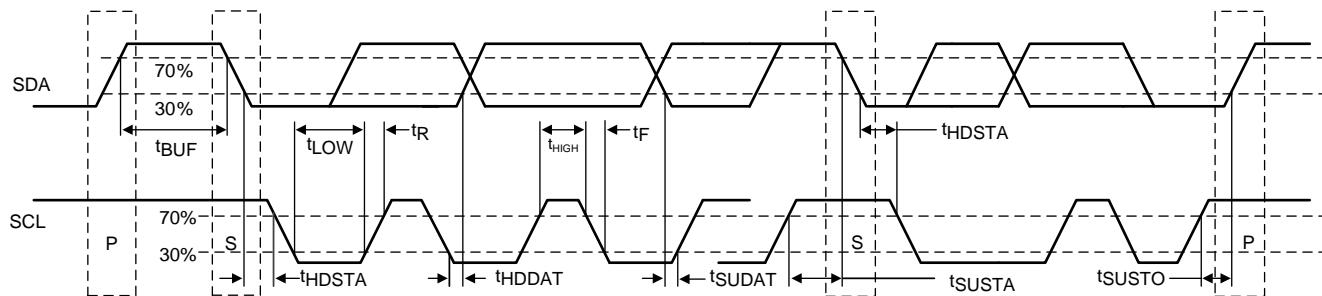
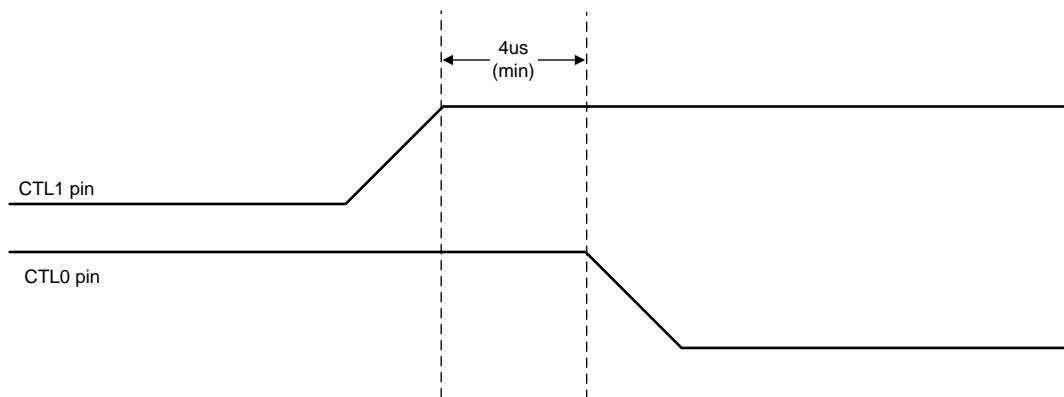
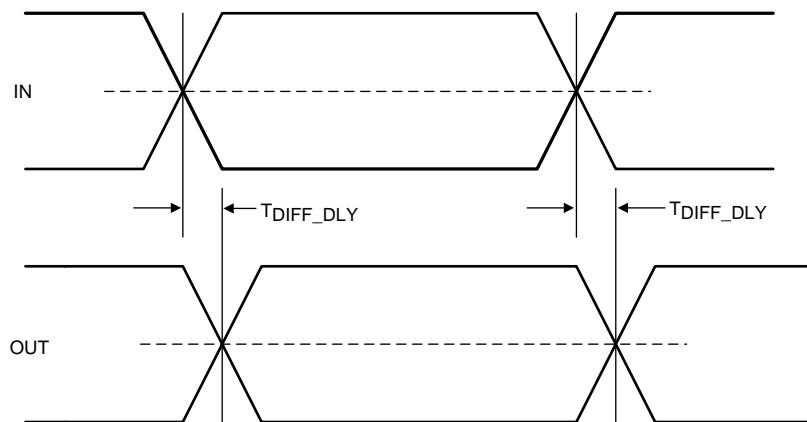
## 6.8 Timing Requirements

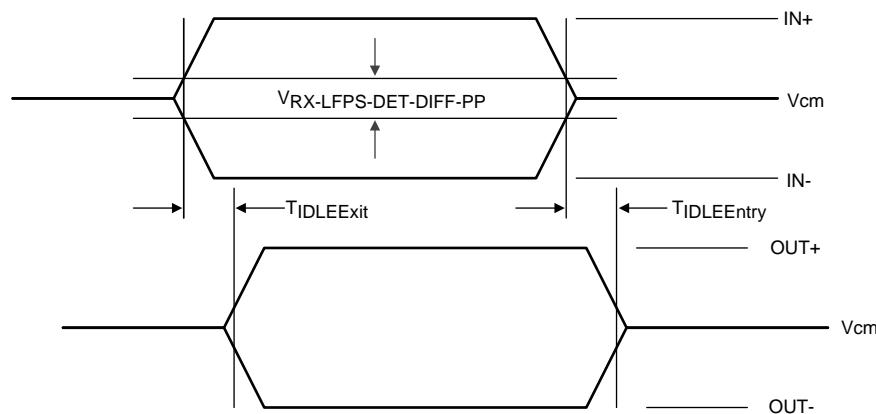
			MIN	NOM	MAX	UNIT
<b>USB Gen 2</b>						
$t_{IDLEEntry}$	Delay from U0 to electrical idle	See <a href="#">Figure 4</a>		10		ns
$t_{DELExit\_U1}$	U1 exist time: break in electrical idle to the transmission of LFPS	See <a href="#">Figure 4</a>		6		ns
$t_{IDLEExit\_U2U3}$	U2/U3 exit time: break in electrical idle to transmission of LFPS		10			μs
$t_{RXDET\_INTVL}$	RX detect interval while in Disconnect			12		ms
$t_{IDLEExit\_DISC}$	Disconnect Exit Time		15			ms
$t_{Exit\_SHTDN}$	Shutdown Exit Time		1			ms
$t_{DIFF\_DLY}$	Differential Propagation Delay	See <a href="#">Figure 3</a>		300		ps
$t_R, t_F$	Output Rise/Fall time (see <a href="#">Figure 5</a> )	20%-80% of differential voltage measured 1 inch from the output pin		40		ps
$t_{RF\_MM}$	Output Rise/Fall time mismatch	20%-80% of differential voltage measured 1 inch from the output pin			2.6	ps

## 6.9 Switching Characteristics

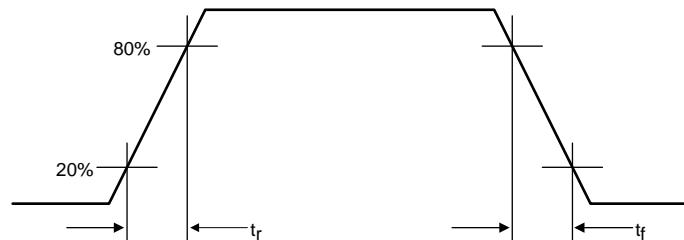
over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>AUXP/N and SBU1/2</b>					
$t_{AUX\_PD}$	Switch propagation delay		400		ps
$t_{AUX\_SW\_OFF}$	Switching time CTL1 to switch OFF. Not including $T_{CTL1\_DEBOUNCE}$ .		500		ns
$t_{AUX\_SW\_ON}$	Switching time CTL1 to switch ON		500		ns
$t_{AUX\_INTRA}$	Intra-pair output skew		100		ps
<b>USB3.1 and DisplayPort mode transition requirement GPIO mode</b>					
$t_{GP\_USB\_4DP}$	Min overlap of CTL1 and CTL1 when transitioning from USB 3.1 only mode to 4-Lane DisplayPort mode or vice versa.		4		μs
<b>CTL1 and HPDIN</b>					
$t_{CTL1\_DEBOUNCE}$	CTL1 and HPDIN debounce time when transitioning from H to L	3	10		ms
<b>I<sup>2</sup>C (Refer to <a href="#">Figure 1</a>)</b>					
$f_{SCL}$	I <sup>2</sup> C clock frequency		1		MHz
$t_{BUF}$	Bus free time between START and STOP conditions	0.5			μs
$t_{HDSTA}$	Hold time after repeated START condition. After this period, the first clock pulse is generated	0.26			μs
$t_{LOW}$	Low period of the I <sup>2</sup> C clock	0.5			μs
$t_{HIGH}$	High period of the I <sup>2</sup> C clock	0.26			μs
$t_{SUSTA}$	Setup time for a repeated START condition	0.26			μs
$t_{HDDAT}$	Data hold time	0			μs
$t_{SUDAT}$	Data setup time	50			ns
$t_R$	Rise time of both SDA and SCL signals		120		ns
$t_F$	Fall time of both SDA and SCL signals	20 × (V <sub>I<sup>2</sup>C</sub> /5.5 V)	120		ns
$t_{SUSTO}$	Setup time for STOP condition	0.26			μs
$C_b$	Capacitive load for each bus line		100		pF

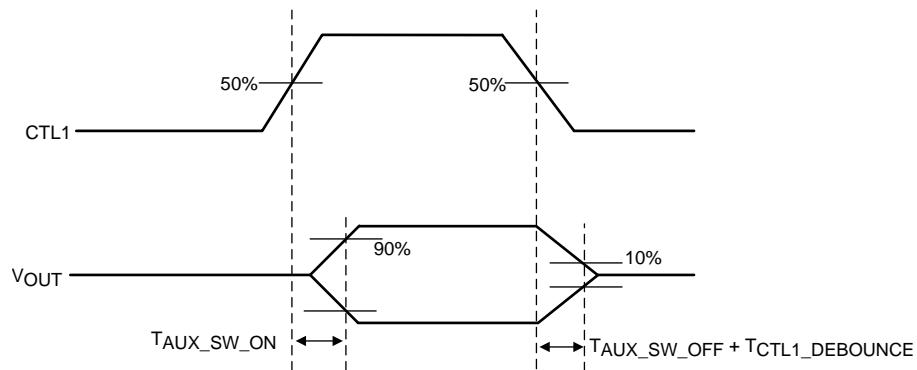

**Figure 1. I2C Timing Diagram Definitions**

**Figure 2. USB3.1 to 4-Lane DisplayPort in GPIO Mode**

**Figure 3. Propagation Delay**



**Figure 4. Electrical Idle Mode Exit and Entry Delay**

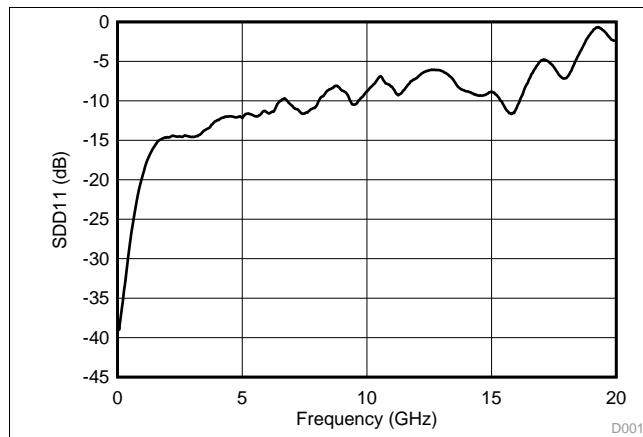


**Figure 5. Output Rise and Fall Times**

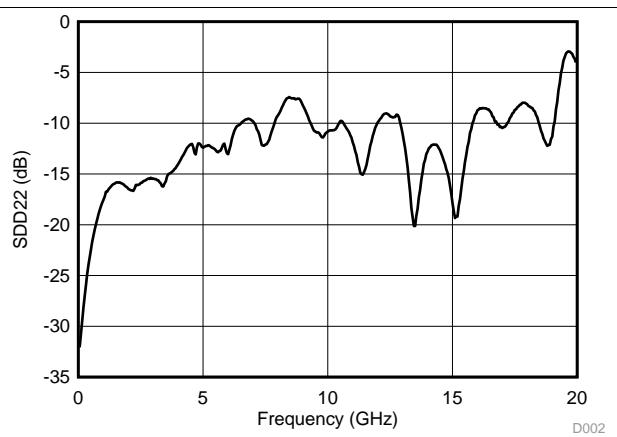


**Figure 6. AUX and SBU Switch ON and OFF Timing Diagram**

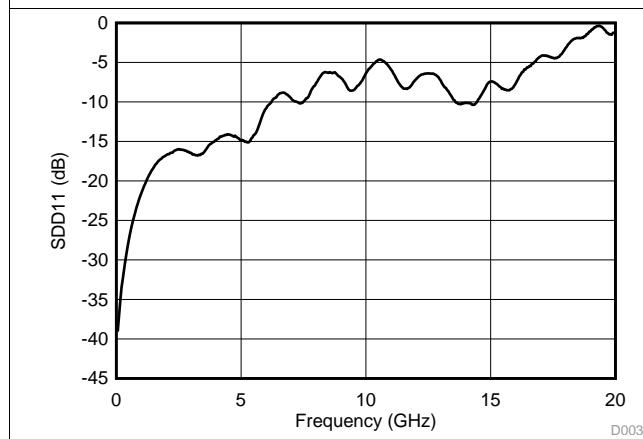
## 6.10 Typical Characteristics



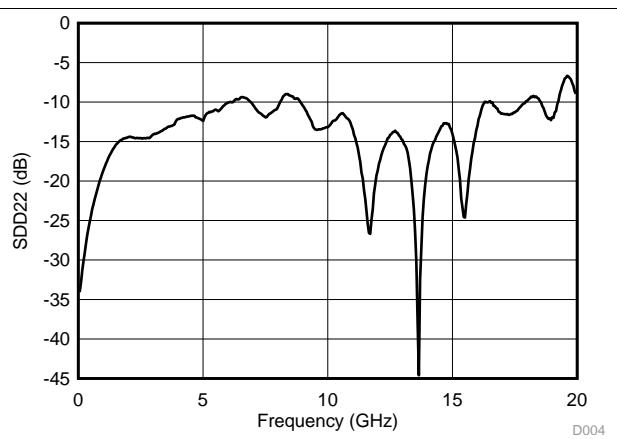
**Figure 7. Input Return Loss Performance of the Downstream Ports**



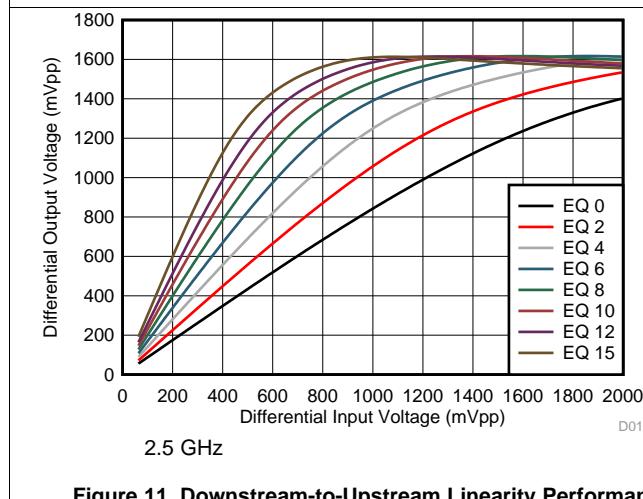
**Figure 8. Output Return Loss Performance of the Downstream Ports**



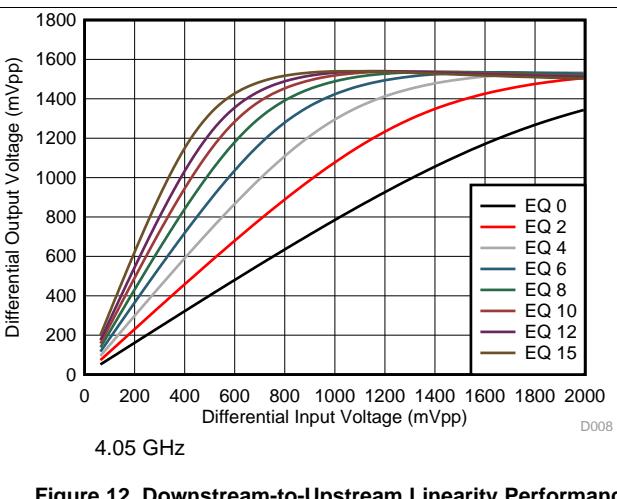
**Figure 9. Input Return Loss Performance of the Upstream Ports**



**Figure 10. Output Return Loss Performance of the Upstream Ports**

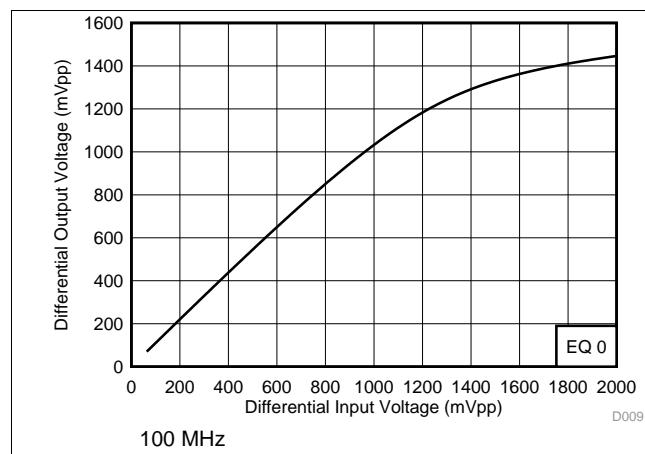


**Figure 11. Downstream-to-Upstream Linearity Performance at 2.5 GHz**

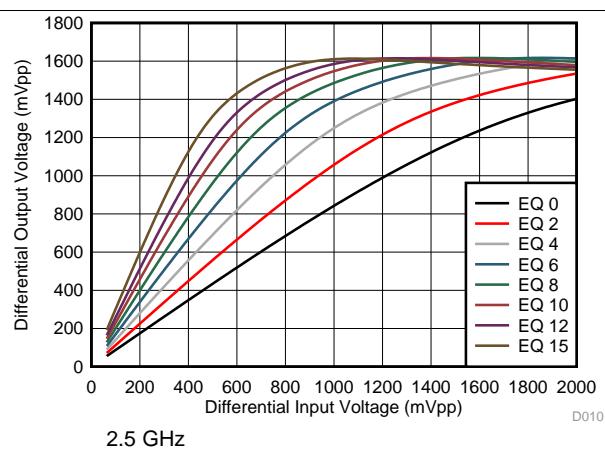


**Figure 12. Downstream-to-Upstream Linearity Performance at 4.05 GHz**

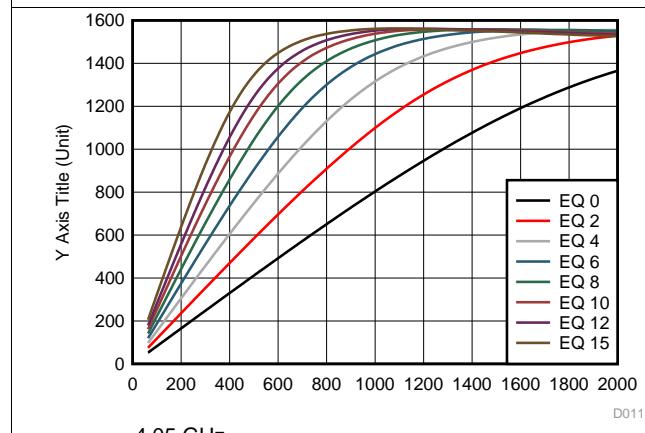
## Typical Characteristics (continued)



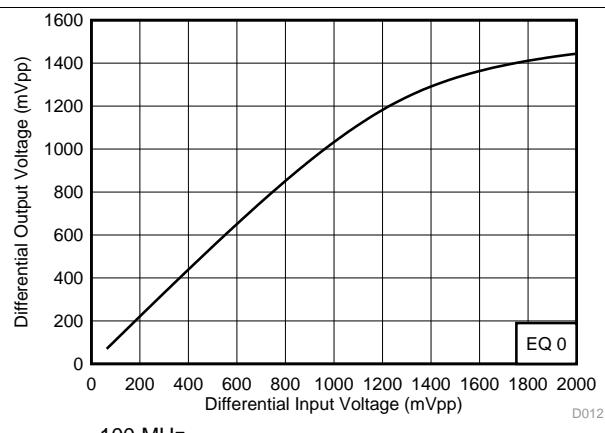
**Figure 13. Downstream-to-Upstream Linearity Performance at 100 MHz**



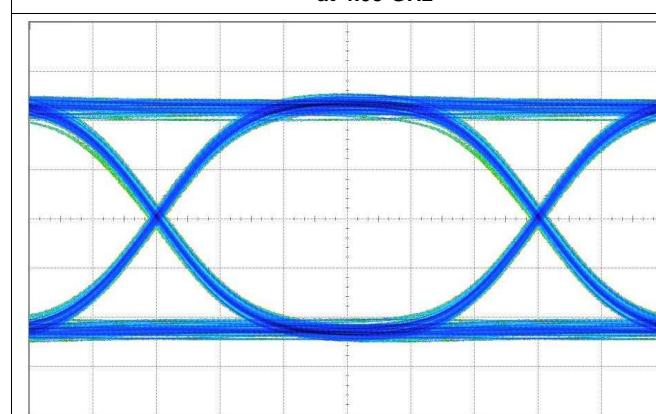
**Figure 14. Upstream-to-Downstream Linearity Performance at 2.5 GHz**



**Figure 15. Upstream-to-Downstream Linearity Performance at 4.05 GHz**



**Figure 16. Upstream-to-Downstream Linearity Performance at 100 MHz**

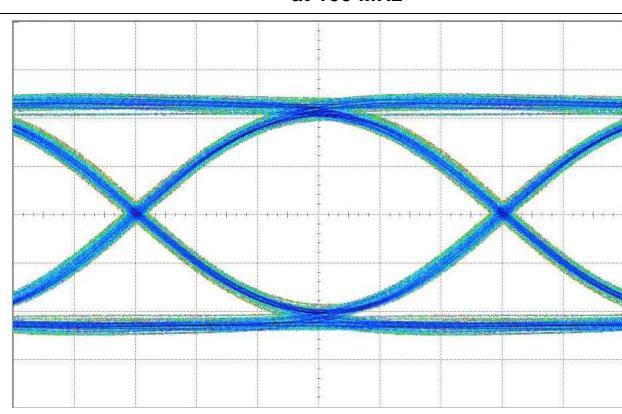


Source Data Rate: 5 Gbps  
Data Pattern: PRBS7

Channel Upstream-to-Downstream, 12 in 6 mil Input PCB  
Channel

Settings EQ Setting: 7 DC Gain Setting: 0 dB  
Linear Range Setting: 1100 mVpp

**Figure 17. Output Eye-Pattern Performance at 5 Gbps**

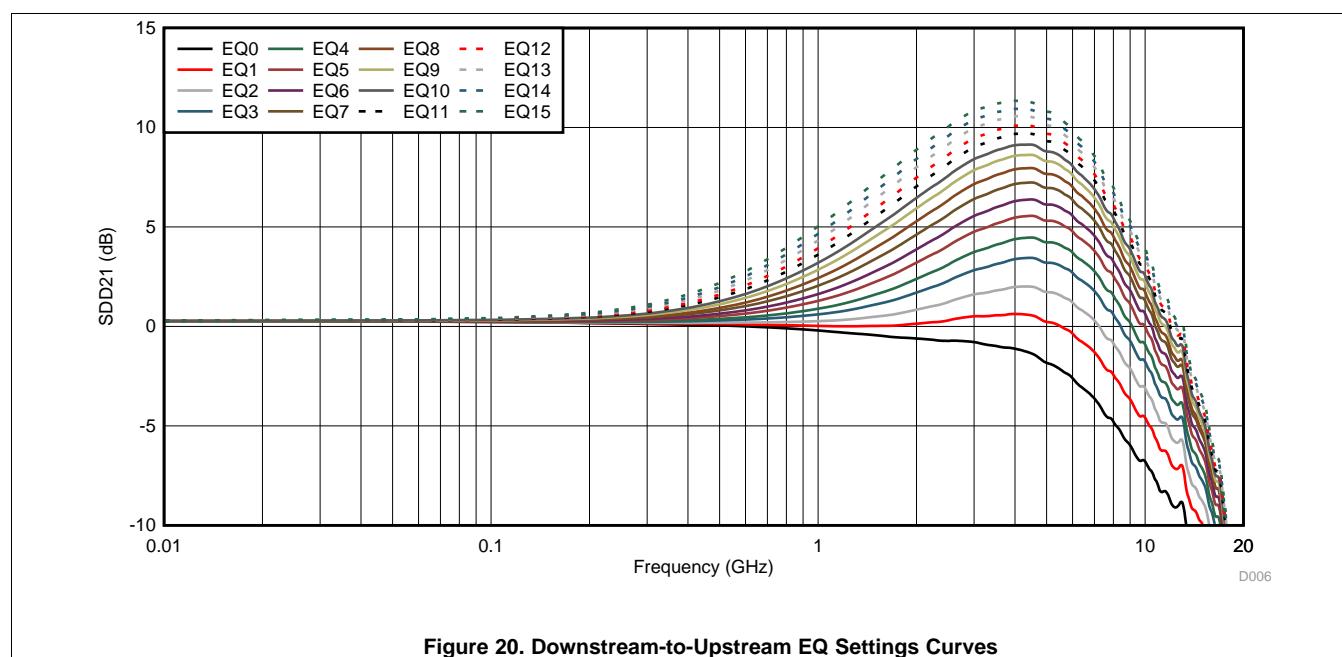
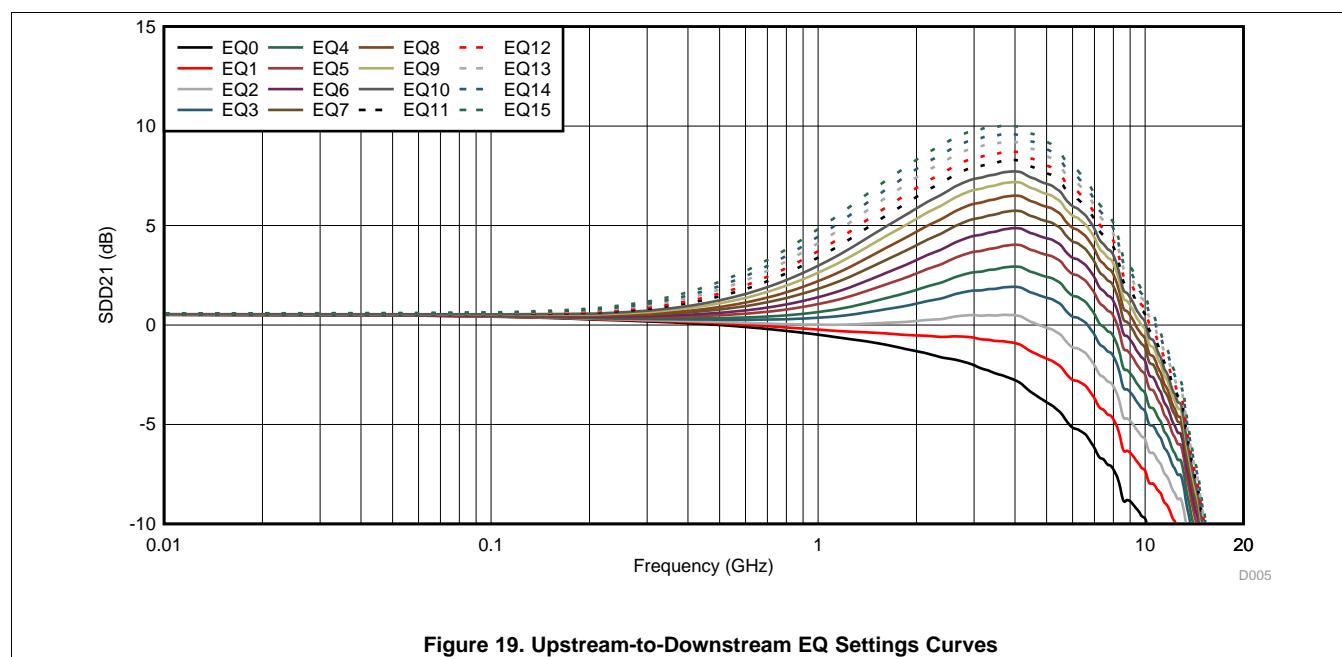


Source Data Rate: 8.1 Gbps  
Data Pattern: PRBS7

Channel Upstream-to-Downstream, 12 in 6 mil Input PCB  
Channel

Settings EQ Setting: 7 DC Gain Setting: 0 dB  
Linear Range Setting: 1100 mVpp

**Figure 18. Output Eye-Pattern Performance at 8.1 Gbps**

**Typical Characteristics (continued)**


## 7 Detailed Description

### 7.1 Overview

The TUSB544 is a USB Type-C Alt Mode re-driver switch supporting data rates up to 8.1 Gbps. This device implements 5th generation USB re-driver technology. The device is utilized for configurations C, D, E, and F from the VESA DisplayPort Alt Mode on USB Type-C Standard. It can also be configured to support custom USB Type-C alternate modes.

The TUSB544 provides several levels of receive equalization to compensate for cable and board trace loss due to inter-symbol interference (ISI) when USB 3.1 GEN1 or DisplayPort (or other Alt modes) signals travel across a PCB or cable. This device requires a 3.3V power supply. It comes for both commercial temperature range and industrial temperature range operation.

For host (source) or device (sink) applications the TUSB544 enables the system to pass both transmitter compliance and receiver jitter tolerance tests for USB 3.1 Gen 1 and DisplayPort version 1.4 HBR3. The re-driver recovers incoming data by applying equalization that compensates for channel loss, and drives out signals with a high differential voltage. Each channel has a receiver equalizer with selectable gain settings. Equalization control for upstream and downstream facing ports can be set using UEQ[1:0], and DEQ[1:0] pins respectively or through the I<sup>2</sup>C interface.

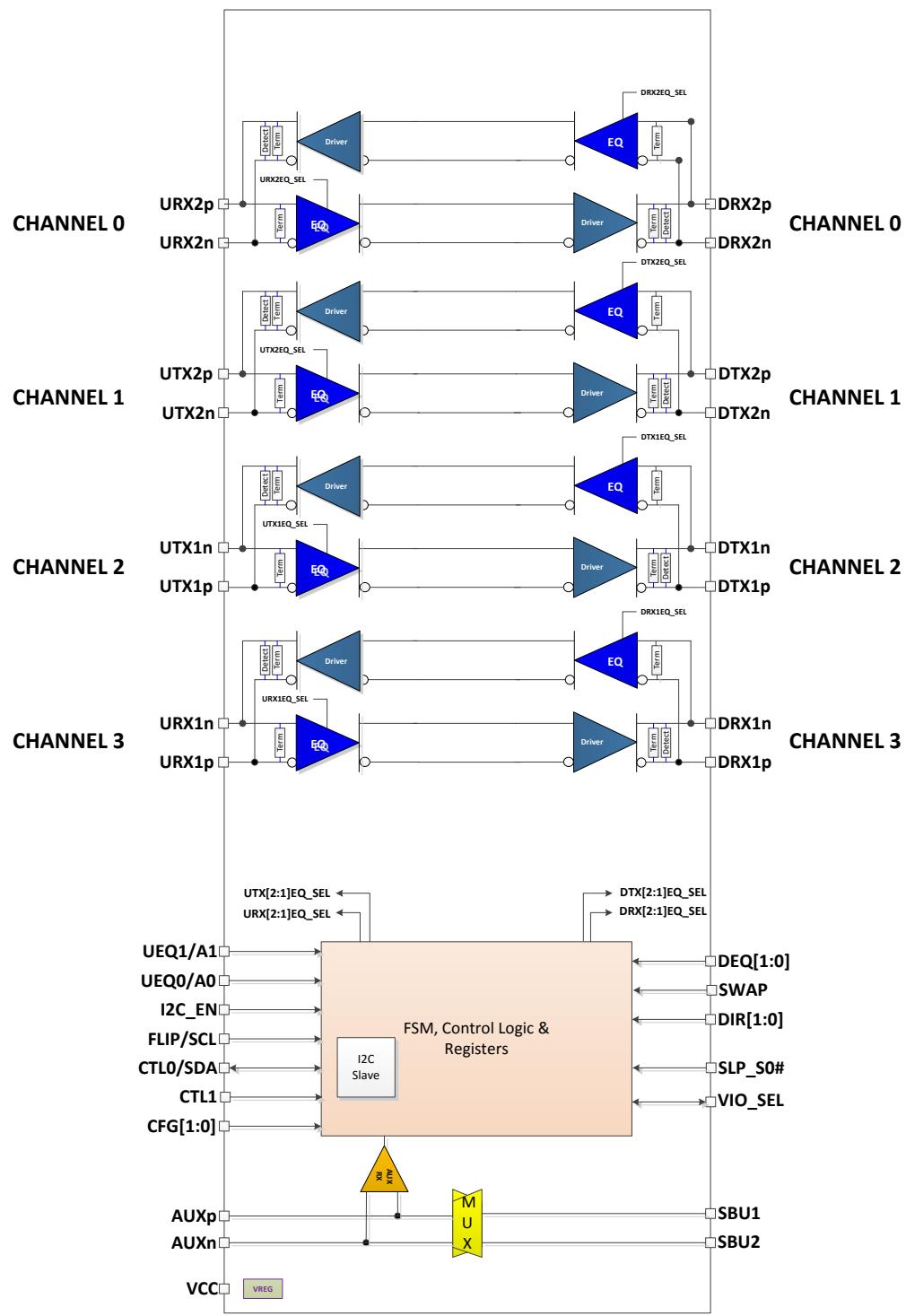
Moreover, the CFG[1:0] or the equivalent I<sup>2</sup>C registers provide the ability to control the EQ DC gain and the voltage linearity range for all the channels (Refer to [Table 8](#)). This flexible control makes it easy to set up the device to pass various standard compliance requirements.

The TUSB544 advanced state machine makes it transparent to hosts and devices. After power up, the TUSB544. periodically performs receiver detection on the TX pairs. If it detects a USB 3.1 GEN1 receiver, the RX termination is enabled, and the TUSB544 is ready to re-drive.

The TUSB544 provides extremely flexible data path signal direction control using the CTL[1:0], FLIP, DIR[1:0], and SWAP pins or through the I<sup>2</sup>C interface. Refer to [Table 4](#) for detailed information on the input to output signal pin mapping.

The device ultra-low-power architecture operates at a 3.3 V power supply and achieves enhanced performance. The automatic LFPS De-Emphasis control further enables the system to be USB 3.1 compliant.

## 7.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated

## 7.3 Feature Description

### 7.3.1 USB 3.1

The TUSB544 supports USB 3.1 data rates up to 5 Gbps. The TUSB544 supports all the USB defined power states (U0, U1, U2, and U3). Because the TUSB544 is a linear re-driver, it can't decode USB3.1 physical layer traffic. The TUSB544 monitors the actual physical layer conditions like receiver termination, electrical idle, LFPS, and SuperSpeed signaling rate to determine the USB power state of the USB3.1 interface.

The TUSB544 features an intelligent low frequency periodic signaling (LFPS) detector. The LFPS detector automatically senses the low frequency signals and disables receiver equalization functionality. When not receiving LFPS, the TUSB544 will enable receiver equalization based on the UEQ[1:0] and DEQ[1:0] pins or values programmed into UEQ[3:0]\_SEL, and DEQ[3:0]\_SEL registers.

### 7.3.2 DisplayPort

The TUSB544 supports up to 4 DisplayPort lanes at data rates up to 8.1Gbps (HBR3). The TUSB544, when configured in DisplayPort mode, monitors the native AUX traffic as it traverses between DisplayPort source and DisplayPort sink. For the purposes of reducing power, the TUSB544 will manage the number of active DisplayPort lanes based on the content of the AUX transactions. The TUSB544 snoops native AUX writes to DisplayPort sink's DPCD registers 0x00101 (LANE\_COUNT\_SET) and 0x00600 (SET\_POWER\_STATE). TUSB544 will disable/enable lanes based on value written to LANE\_COUNT\_SET. The TUSB544 will disable all lanes when SET\_POWER\_STATE is in the D3. Otherwise active lanes will be based on value of LANE\_COUNT\_SET.

DisplayPort AUX snooping is enabled by default but can be disabled by changing the AUX\_SNOOP\_DISABLE register. Once AUX snoop is disabled, management of TUSB544's DisplayPort lanes are controlled through various configuration registers.

### 7.3.3 4-level Inputs

The TUSB544 has (I2C\_EN, UEQ[1:0], DEQ[1:0], CFG[1:0], and A[1:0]) 4-level inputs pins that are used to control the equalization gain, voltage linearity range, and place TUSB544 into different modes of operation. These 4-level inputs utilize a resistor divider to help set the 4 valid levels and provide a wider range of control settings. There is an internal 30 kΩ pull-up and a 94kΩ pull-down. These resistors, together with the external resistor connection combine to achieve the desired voltage level.

**Table 1. 4-Level Control Pin Settings**

LEVEL	SETTINGS
0	Option 1: Tie 1 KΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 KΩ 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 KΩ 5% to V <sub>CC</sub> . Option 2: Tie directly to V <sub>CC</sub> .

#### NOTE

All four-level inputs are latched on rising edge of internal reset. After  $T_{cfg\_hd}$ , the internal pull-up and pull-down resistors will be isolated in order to save power.

### 7.3.4 Receiver Linear Equalization

The purpose of receiver equalization is to compensate for channel insertion loss and inter-symbol interference in the system. The receiver overcomes these losses by attenuating the low frequency components of the signals with respect to the high frequency components. The proper gain setting should be selected to match the channel insertion loss. Two 4-level input pins enable up to 16 possible equalization settings. The upstream path, and the downstream path each have their own two 4-level inputs for equalization settings; UEQ[1:0] and DEQ[1:0] respectively. The TUSB544 also provides the flexibility of adjusting equalization settings through I2C registers URX[2:1]EQ\_SEL, UTX[2:1]EQ\_SEL, DRX[2:1]EQ\_SEL, and DTX[2:1]EQ\_SEL for each individual channel and for each direction (upstream or downstream).

## 7.4 Device Functional Modes

### 7.4.1 Device Configuration in GPIO mode

The TUSB544 is in GPIO configuration when I2C\_EN = "0". The TUSB544 supports operational combinations with USB and two different Type-C Alternate Modes.. One combination includes USB and Alternate Mode DisplayPort, and the other combination includes USB and custom Alternate Mode. For each operational combination the data path directions can be further set using the DIR[1:0] pins or through I2C to enable the device to operate in the source or sink sides. Please refer to [Table 2](#) for all the configuration of all the operational modes.

When the device is set to operate in a USB and Alternate Mode DisplayPort the following configurations can be further set: USB3.1 only, 2 DisplayPort lanes + USB3.1, or 4 DisplayPort lanes (no USB3.1). The CTL1 pin controls whether DisplayPort is enabled. The combination of CTL1 and CTL0 selects between USB3.1 only, 2 lanes of DisplayPort, or 4-lanes of DisplayPort as detailed in [Table 2](#). The AUXP/N to SBU1/2 mapping is controlled based on [Table 3](#).

When the device is set to operate in a USB and custom Alternate Mode the following configurations can be further set: USB3.1 only, 2 Channels of custom Alternate Mode + USB3.1, or 4 Channels of custom Alternate Mode (no USB3.1). The CTL1 pin controls whether custom Alternate Mode is enabled. The combination of CTL1 and CTL0 selects between USB3.1 only, 2 channels of custom Alternate Mode, or 4 channels of custom Alternate Mode as detailed in [Table 2](#). The AUXP/N to SBU1/2 mapping is controlled based on [Table 3](#).

Further data path direction control can be achieved using the SWAP pin. When set high, the SWAP pin reverses the data path direction on all the channels and swaps the equalization settings of the upstream and downstream facing input ports. This pin may be found useful in active cable application with TUSB544 installed on only one end. The SWAP pin can be set based on which cable end is plugged to the source or sink side receptacle

After power-up (VCC from 0 V to 3.3 V), the TUSB544 will default to USB3.1 mode. The USB PD controller, upon detecting no device attached to Type-C port or USB3.1 operation not required by attached device, must take TUSB544 out of USB3.1 mode by transitioning the CTL0 pin from L to H and back to L.

**Table 2. GPIO Configuration Control**

DIR1 PIN	DIR0 PIN	CTL1 PIN	CTL0 PIN	FLIP PIN	TUSB544 CONFIGURATION	VESA DisplayPort ALT MODE DFP_D Configuration
USB + DisplayPort Alternate Mode (Source Side)						
L	L	L	L	L	Power Down/Cable Mode	—
L	L	L	L	H	Power Down/Cable Mode	—
L	L	L	H	L	One Port USB 3.1 - No Flip	—
L	L	L	H	H	One Port USB 3.1 – With Flip	—
L	L	H	L	L	4 Lane DP - No Flip	C and E
L	L	H	L	H	4 Lane DP – with Flip	C and E
L	L	H	H	L	One Port USB 3.1 + 2 Lane DP- No Flip	D and F
L	L	H	H	H	One Port USB 3.1 + 2 Lane DP– with Flip	D and F
USB + DisplayPort Alternate Mode (Sink Side)						
L	H	L	L	L	Power Down/Cable Mode	—
L	H	L	L	H	Power Down/Cable Mode	—
L	H	L	H	L	One Port USB 3.1 - No Flip	—
L	H	L	H	H	One Port USB 3.1 – With Flip	—
L	H	H	L	L	4 Lane DP - No Flip	C and E
L	H	H	L	H	4 Lane DP – With Flip	C and E
L	H	H	H	L	One Port USB 3.1 + 2 Lane DP- No Flip	D and F
L	H	H	H	H	One Port USB 3.1 + 2 Lane DP– With Flip	D and F

**Device Functional Modes (continued)**
**Table 2. GPIO Configuration Control (continued)**

DIR1 PIN	DIR0 PIN	CTL1 PIN	CTL0 PIN	FLIP PIN	TUSB544 CONFIGURATION	VESA DisplayPort ALT MODE DFP_D Configuration
USB + Custom Alternate Mode (Source Side)						
H	L	L	L	L	Power Down/Cable Mode	–
H	L	L	L	H	Power Down/Cable Mode	–
H	L	L	H	L	One Port USB 3.1 - No Flip	–
H	L	L	H	H	One Port USB 3.1 – With Flip	–
H	L	H	L	L	4 Channel Custom Alt Mode - No Flip	–
H	L	H	L	H	4 Channel Custom Alt Mode– With Flip	–
H	L	H	H	L	One Port USB 3.1 + 2 Channel Custom Alt Mode- No Flip	–
H	L	H	H	H	One Port USB 3.1 + 2 Channel Custom Alt Mode – With Flip	–
USB + Custom Alternate Mode (Sink Side)						
H	H	L	L	L	Power Down/Cable Mode	–
H	H	L	L	H	Power Down/Cable Mode	–
H	H	L	H	L	One Port USB 3.1 - No Flip	–
H	H	L	H	H	One Port USB 3.1 – With Flip	–
H	H	H	L	L	4 Channel Custom Alt Mode - No Flip	–
H	H	H	L	H	4 Channel Custom Alt Mode– With Flip	–
H	H	H	H	L	One Port USB 3.1 + 2 Channel Custom Alt Mode- No Flip	–
H	H	H	H	H	One Port USB 3.1 + 2 Channel Custom Alt Mode – With Flip	–

**Table 3. GPIO AUXP/N to SBU1/2 Mapping**

CTL1 pin	FLIP pin	Mapping
H	L	AUXP -> SBU1 AUXN -> SBU2
H	H	AUXP -> SBU2 AUXN -> SBU1
L > 2ms	X	Open

Details the TUSB544 mux routing. This table is valid for both I<sup>2</sup>C and GPIO.

**Table 4. INPUT to OUTPUT Mapping**

					From	To
DIR1 PIN	DIR0 PIN	CTL1 PIN	CTL0 PIN	FLIP PIN	Input Pin	Output Pin
USB + DisplayPort Alternate Mode (Source Side)						
L	L	L	L	L	NA	NA
L	L	L	L	H	NA	NA
L	L	L	H	L	DRX1P	URX1P (SSRXP)
					DRX1N	URX1N (SSRXN)
					UTX1P (SSTXP)	DTX1P
					UTX1N (SSTXN)	DTX1N
L	L	L	H	H	DRX2P	URX2P (SSRXP)
					DRX2N	URX2N (SSRXN)
					UTX2P (SSTXP)	DTX2P
					UTX2N (SSTXN)	DTX2N
L	L	H	L	L	URX2P (DP0P)	DRX2P
					URX2N (DP0N)	DRX2N
					UTX2P (DP1P)	DTX2P
					UTX2N (DP1N)	DTX2N
					UTX1P (DP2P)	DTX1P
					UTX1N (DP2N)	DTX1N
					URX1P (DP3P)	DRX1P
					URX1N (DP3N)	DRX1N
L	L	H	L	H	URX1P (DP0P)	DRX1P
					URX1N (DP0N)	DRX1N
					UTX1P (DP1P)	DTX1P
					UTX1N (DP1N)	DTX1N
					UTX2P (DP2P)	DTX2P
					UTX2N (DP2N)	DTX2N
					URX2P (DP3P)	DRX2P
					URX2N (DP3N)	DRX2N
L	L	H	H	L	DRX1P	URX1P (SSRXP)
					DRX1N	URX1N (SSRXN)
					UTX1P (SSTXP)	DTX1P
					UTX1N (SSTXN)	DTX1N
					URX2P (DP0P)	DRX2P
					URX2N (DP0N)	DRX2N
					UTX2P (DP1P)	DTX2P
					UTX2N (DP1N)	DTX2N
L	L	H	H	H	DRX2P	URX2P (SSRXP)
					DRX2N	URX2N (SSRXN)
					UTX2P (SSTXP)	DTX2P
					UTX2N (SSTXN)	DTX2N
					URX1P (DP0P)	DRX1P
					URX1N (DP0N)	DRX1N
					UTX1P (DP1P)	DTX1P
					UTX1N (DP1N)	DTX1N
USB + DisplayPort Alternate Mode (Sink Side)						

**Table 4. INPUT to OUTPUT Mapping (continued)**

					From	To
DIR1 PIN	DIR0 PIN	CTL1 PIN	CTL0 PIN	FLIP PIN	Input Pin	Output Pin
L	H	L	L	L	NA	NA
L	H	L	L	H	NA	NA
L	H	L	H	L	UTX2P	DTX2P (SSRXP)
					UTX2N	DTX2N (SSRXN)
					DRX2P (SSTXP)	URX2P
					DRX2N (SSTXN)	URX2N
L	H	L	H	H	UTX1P	DTX1P (SSRXP)
					UTX1N	DTX1N (SSRXN)
					DRX1P (SSTXP)	URX1P
					DRX1N (SSTXN)	URX1N
L	H	H	L	L	URX2P	DRX2P (DP3P)
					URX2N	DRX2N (DP3N)
					UTX2P	DTX2P (DP2P)
					UTX2N	DTX2N (DP2N)
					UTX1P	DTX1P (DP1P)
					UTX1N	DTX1N (DP1N)
					URX1P	DRX1P (DP0P)
					URX2N	DRX2N (DP0N)
L	H	H	L	H	URX1N	DRX1N (DP1N)
					URX1P	DRX1P (DP3P)
					URX1N	DRX1N (DP3N)
					UTX1P	DTX1P (DP2P)
					UTX1N	DTX1N (DP2N)
					UTX2P	DTX2P (DP1P)
					UTX2N	DTX2N (DP1N)
					URX2P	DRX2P (DP0P)
					URX2N	DRX2N (DP0N)
					DRX2P (SSRXP)	URX2P
L	H	H	H	L	DRX2N (SSRXN)	URX2N
					UTX2P	DTX2P (SSTXP)
					UTX2N	DTX2N (SSTXN)
					URX1P	DRX1P (DP0P)
					URX1N	DRX1N (DP0N)
					UTX1P	DTX1P (DP1P)
					UTX1N	DTX1N (DP1N)
					DRX1P (SSRXP)	URX1P
L	H	H	H	H	DRX1N (SSRXN)	URX1N
					UTX1P	DTX1P (SSTXP)
					UTX1N	DTX1N (SSTXN)
					URX2P	DRX2P (DP0P)
					URX2N	DRX2N (DP0N)
					UTX2P	DTX2P (DP1P)
					UTX2N	DTX2N (DP1N)
					DRX2P (SSRXP)	URX2P
USB + Custom Alternate Mode (Source Side)					DRX1N (SSRXN)	URX2N
H	L	L	L	L	NA	NA
H	L	L	L	H	NA	NA

**Table 4. INPUT to OUTPUT Mapping (continued)**

					From	To
DIR1 PIN	DIR0 PIN	CTL1 PIN	CTL0 PIN	FLIP PIN	Input Pin	Output Pin
H	L	L	H	L	DRX1P	URX1P (SSRXP)
					DRX1N	URX1N (SSRXN)
					UTX1P (SSTXP)	DTX1P
					UTX1N (SSTXN)	DTX1N
H	L	L	H	H	DRX2P	URX2P (SSRXP)
					DRX2N	URX2N (SSRXN)
					UTX2P (SSTXP)	DTX2P
					UTX2N (SSTXN)	DTX2N
H	L	H	L	L	DRX2P	URX2P (LN1RXP)
					DRX2N	URX2N (LN1RXN)
					UTX2P (LN1TXP)	DTX2P
					UTX2N (LN1TXN)	DTX2N
					UTX1P (LN0TXP)	DTX1P
					UTX1N (LN0TXN)	DTX1N
					DRX1P	URX1P (LN0RXP)
					DRX1N	URX1N (LN0RXN)
H	L	H	L	H	DRX1P	URX1P (LN1RXP)
					DRX1N	URX1N (LN1RXN)
					UTX1P (LN1TXP)	DTX1P
					UTX1N (LN1TXN)	DTX1N
					UTX2P (LN0TXP)	DTX2P
					UTX2N (LN0TXN)	DTX2N
H	L	H	H	L	DRX2P	URX2P (LN0RXP)
					DRX2N	URX2N (LN0RXN)
					DRX1P	URX1P (SSRXP)
					DRX1N	URX1N (SSRXN)
					UTX1P (SSTXP)	DTX1P
					UTX1N (SSTXN)	DTX1N
					UTX2P (LN0TXP)	DTX2P
					UTX2N (LN0TXN)	DTX2N
H	L	H	H	H	DRX2P	URX2P (SSRXP)
					DRX2N	URX2N (SSRXN)
					UTX2P (SSTXP)	DTX2P
					UTX2N (SSTXN)	DTX2N
					UTX1P (LN0TXP)	DTX1P
					UTX1N (LN0TXN)	DTX1N
					DRX1P	URX1P (LN0RXP)
					DRX1N	URX1N (LN0RXN)
USB + Custom Alternate Mode (Sink Side)					NA	NA
H	H	L	L	L	NA	NA
H	H	L	L	H	NA	NA

**Table 4. INPUT to OUTPUT Mapping (continued)**

					From	To
DIR1 PIN	DIR0 PIN	CTL1 PIN	CTL0 PIN	FLIP PIN	Input Pin	Output Pin
H	H	L	H	L	UTX2P	DTX2P (SSRXP)
					UTX2N	DTX2N (SSRXN)
					DRX2P (SSTXP)	URX2P
					DRX2N (SSTXN)	URX2N
H	H	L	H	H	UTX1P	DTX1P (SSRXP)
					UTX1N	DTX1N (SSRXN)
					DRX1P (SSTXP)	URX1P
					DRX1N (SSTXN)	URX1N
H	H	H	L	L	DRX2P	URX2P (LN1TXP)
					DRX2N	URX2N (LN1TXN)
					UTX2P (LN1RXP)	DTX2P
					UTX2N (LN1RXN)	DTX2N
					UTX1P (LN0RXP)	DTX1P
					UTX1N (LN0RXN)	DTX1N
					DRX1P	URX1P (LN0RXP)
					DRX1N	URX1N (LN0RXN)
H	H	H	L	H	DRX2P	URX2P (LN0RXP)
					DRX2N	URX2N (LN0RXN)
					UTX2P (LN0RXP)	DTX2P
					UTX2N (LN0RXN)	DTX2N
					UTX1P (LN0RXP)	DTX1P
					UTX1N (LN0RXN)	DTX1N
					DRX1P	URX1P (LN0TXP)
					DRX1N	URX1N (LN0TXN)
H	H	H	H	L	UTX2P	DTX2P (SSRXP)
					UTX2N	DTX2N (SSRXN)
					DRX2P (SSTXP)	URX2P
					DRX2N (SSTXN)	URX2N
					UTX1P	DTX1P (LN0RXP)
					UTX1N	DTX1N (LN0RXN)
					DRX1P (LN0TXP)	URX1P
					DRX1N (LN0TXN)	URX1N
H	H	H	H	H	UTX1P	DTX1P (SSRXP)
					UTX1N	DTX1N (SSRXN)
					DRX1P (SSTXP)	URX1P
					DRX1N (SSTXN)	URX1N
					DRX2P	URX2P (LN0TXP)
					DRX2N	URX2N (LN0TXN)
					UTX2P (LN0RXP)	DTX2P
					UTX2N (LN0RXN)	DTX2N

#### 7.4.2 Device Configuration in I2C Mode

The TUSB544 is in I2C mode when I2C\_EN is not equal to “0”. The same configurations defined in GPIO mode are also available in I2C mode. The TUSB544’s USB3.1, DisplayPort, and custom Alternate Mode configuration is controlled based on [Table 5](#). The AUXP/N to SBU1/2 mapping control is based on [Table 5](#).

**Table 5. I2C Configuration Control**

Registers					TUSB544 Configuration	VESA DisplayPort Alt Mode DFP_D Configuration
DIRSEL1	DIRSEL0	CTLSEL1	CTLSEL0	FLIPSEL		
USB + DisplayPort Alternate Mode (Source Side)						
L	L	L	L	L	Power Down	–
L	L	L	L	H	Power Down	–
L	L	L	H	L	One Port USB 3.1 - No Flip	–
L	L	L	H	H	One Port USB 3.1 – With Flip	–
L	L	H	L	L	4 Lane DP - No Flip	C and E
L	L	H	L	H	4 Lane DP – With Flip	C and E
L	L	H	H	L	One Port USB 3.1 + 2 Lane DP- No Flip	D and F
L	L	H	H	H	One Port USB 3.1 + 2 Lane DP– With Flip	D and F
USB + DisplayPort Alternate Mode (Sink Side)						
L	H	L	L	L	Power Down	–
L	H	L	L	H	Power Down	–
L	H	L	H	L	One Port USB 3.1 - No Flip	–
L	H	L	H	H	One Port USB 3.1 – With Flip	–
L	H	H	L	L	4 Lane DP - No Flip	C and E
L	H	H	L	H	4 Lane DP – With Flip	C and E
L	H	H	H	L	One Port USB 3.1 + 2 Lane DP- No Flip	D and F
L	H	H	H	H	One Port USB 3.1 + 2 Lane DP– With Flip	D and F
USB + Custom Alternate Mode (Source Side)						
H	L	L	L	L	Power Down	–
H	L	L	L	H	Power Down	–
H	L	L	H	L	One Port USB 3.1 - No Flip	–
H	L	L	H	H	One Port USB 3.1 – With Flip	–
H	L	H	L	L	4 Channel Custom Alt Mode - No Flip	–
H	L	H	L	H	4 Channel Custom Alt Mode– With Flip	–
H	L	H	H	L	One Port USB 3.1 + 2 Channel Custom Alt Mode- No Flip	–
H	L	H	H	H	One Port USB 3.1 + 2 Channel Custom Alt Mode – With Flip	–
USB + Custom Alternate Mode (Sink Side)						
H	H	L	L	L	Power Down	–
H	H	L	L	H	Power Down	–
H	H	L	H	L	One Port USB 3.1 - No Flip	–
H	H	L	H	H	One Port USB 3.1 – With Flip	–
H	H	H	L	L	4 Channel Custom Alt Mode - No Flip	–
H	H	H	L	H	4 Channel Custom Alt Mode– With Flip	–
H	H	H	H	L	One Port USB 3.1 + 2 Channel Custom Alt Mode- No Flip	–

**Table 5. I2C Configuration Control (continued)**

Registers					TUSB544 Configuration	VESA DisplayPort Alt Mode DFP_D Configuration
DIRSEL1	DIRSEL0	CTLSEL1	CTLSEL0	FLIPSEL		
H	H	H	H	H	One Port USB 3.1 + 2 Channel Custom Alt Mode – With Flip	–

**Table 6. I2C AUXP/N to SBU1/2 Mapping**

Registers			Mapping
AUX_SBU_OVR	CTLSEL1	FLIPSEL	
00	H	L	AUXp -> SBU1 AUXn -> SBU2
00	H	H	AUXp -> SBU2 AUXn -> SBU1
00	L	X	Open
01	X	X	AUXp -> SBU1 AUXn -> SBU2
10	X	X	AUXp -> SBU2 AUXn -> SBU1
11	X	X	Open

#### 7.4.3 DisplayPort Mode

The TUSB544 supports up to four DisplayPort lanes at datarates up to 8.1Gbps. TUSB544 can be enabled for DisplayPort through GPIO control or through I2C register control. When I2C\_EN is '0', DisplayPort is controlled based on [Table 2](#). When not in GPIO mode, enable of DisplayPort functionality is controlled through I<sup>2</sup>C registers.

#### 7.4.4 Custom Alternate Mode

The TUSB544 supports up to two lanes (or 4 channels) of custom Alternate Mode at datarates up to 8.1Gbps. TUSB544 can be enabled for custom Alternate Mode through GPIO control or through I<sup>2</sup>C register control. When I2C\_EN is '0', custom Alternate Mode is controlled based on [Table 2](#). When not in GPIO mode, enable of custom Alternate Mode functionality is controlled through I2C registers. In I2C mode, the operation of this mode requires setting up AUX\_SNOOP\_DISABLE register 0x13 bit 7 to 0.

#### 7.4.5 Cable Mode

Cable mode is designed for applications within a cable, where the PD controller may not be able to provide USB/DP mode information. It is therefore necessary for the device to recognize the correct mode and automatically update modes on-the-fly. In GPIO mode, cable mode is set by keeping the CTL0 and CTL1 pins low at all times. In I2C mode, cable mode is set by writing a 1 to register 0x0A.6. It is expected that the PD controller can provide HPDIN. In cable mode, this pin is synonymous with CTL1 in normal mode. When high, DP mode will be active (with or without USB), and when low, USB-only will be active.

AUX snooping is active by default in cable mode. Through AUX snooping the device can be set in either 1 lane DP, 2 lane DP or 4 lane DP. If AUX snooping is disabled in cable mode, 2-lane DP mode is activated when HPDIN is set high. 4-lane DP mode is ultimately set if USB mode is not detected.

#### 7.4.6 Linear EQ Configuration

TUSB544 receiver lanes have controls for receiver equalization for upstream and downstream facing ports. The receiver equalization gain value can be controlled either through I2C registers or through GPIOs. [Table 7](#) details the gain value for each available combination when TUSB544 is in GPIO mode. These same options are also available per channel and for upstream and downstream facing ports in I2C mode by updating registers URX[2:1]EQ\_SEL, UTX[2:1]EQ\_SEL, DRX[2:1]EQ\_SEL, and DTX[2:1]EQ\_SEL.

**Table 7. TUSB544 Receiver Equalization GPIO Control**

Downstream Facing Ports				Upstream Facing Port			
DEQ1 pin Level	DEQ0 pin Level	EQ GAIN 2.5GHz (dB)	EQ GAIN 4.05GHz (dB)	UEQ1 pin Level	UEQ0 pin Level	EQ GAIN 2.5GHz (dB)	EQ GAIN 4.05GHz (dB)
0	0	-1.0	-1.4	0	0	-2.2	-3.3
0	R	0.1	0.4	0	R	-1.1	-1.5
0	F	1.0	1.7	0	F	-0.2	0.0
0	1	2.1	3.2	0	1	0.9	1.4
R	0	2.9	4.1	R	0	1.8	2.4
R	R	3.8	5.2	R	R	2.7	3.5
R	F	4.6	6.1	R	F	3.4	4.3
R	1	5.4	6.9	R	1	4.3	5.2
F	0	6.1	7.7	F	0	5.0	6.0
F	R	6.8	8.3	F	R	5.7	6.6
F	F	7.3	8.8	F	F	6.2	7.2
F	1	7.9	9.4	F	1	6.8	7.7
1	0	8.4	9.8	1	0	7.3	8.1
1	R	8.9	10.3	1	R	7.8	8.6
1	F	9.3	10.6	1	F	8.2	9.0
1	1	9.8	11.0	1	1	8.7	9.4

#### 7.4.7 Adjustable VOD Linear Range and DC Gain

The CFG0 and CFG1 pins can be used to adjust the TUSB544 differential output voltage (VOD) swing linear range and receiver equalization DC gain for both downstream and upstream data path directions. [Table 8](#) details the available options.

**Table 8. VOD Linear Range and DC Gain**

Setting #	CFG1 pin Level	CFG0 pin Level	Downstream DC Gain (dB)	Upstream DC Gain (dB)	Downstream VOD Linear Range (mVpp)	Upstream VOD Linear Range (mVpp)
1	0	0	1	0	900	900
2	0	R	0	1	900	900
3	0	F	0	0	900	900
4	0	1	1	1	900	900
5	R	0	0	0	1100	1100
6	R	R	1	0	1100	1100
7	R	F	0	1	1100	1100
8	R	1	2	2	1100	1100
9	F	0	Reserved	Reserved	Reserved	Reserved
10	F	R	Reserved	Reserved	Reserved	Reserved
11	F	F	Reserved	Reserved	Reserved	Reserved
12	F	1	Reserved	Reserved	Reserved	Reserved
13	1	0	Reserved	Reserved	Reserved	Reserved
14	1	R	Reserved	Reserved	Reserved	Reserved
15	1	F	Reserved	Reserved	Reserved	Reserved
16	1	1	Reserved	Reserved	Reserved	Reserved

#### 7.4.8 USB3.1 modes

The TUSB544 monitors the physical layer conditions like receiver termination, electrical idle, LFPS, and SuperSpeed signaling rate to determine the state of the USB3.1 interface. Depending on the state of the USB 3.1 interface, the TUSB544 can be in one of four primary modes of operation when USB 3.1 is enabled (CTL0 = H or CTLSEL0 = 1b1): Disconnect, U2/U3, U1, and U0.

The Disconnect mode is the state in which TUSB544 has not detected far-end termination on both upstream facing port (UFP) or downstream facing port (DFP). The disconnect mode is the lowest power mode of each of the four modes. The TUSB544 will remain in this mode until far-end receiver termination has been detected on both UFP and DFP. The TUSB544 will immediately exit this mode and enter U0 once far-end termination is detected.

Once in U0 mode, the TUSB544 will redrive all traffic received on UFP and DFP. U0 is the highest power mode of all USB3.1 modes. The TUSB544 will remain in U0 mode until electrical idle occurs on both UFP and DFP. Upon detecting electrical idle, the TUSB544 will immediately transition to U1.

The U1 mode is the intermediate mode between U0 mode and U2/U3 mode. In U1 mode, the TUSB544's UFP and DFP receiver termination will remain enabled. The UFP and DFP transmitter DC common mode is maintained. The power consumption in U1 will be similar to power consumption of U0.

Next to the disconnect mode, the U2 and U3 mode is next lowest power state. While in this mode, the TUSB544 will periodically perform far-end receiver detection. Anytime the far-end receiver termination is not detected on either UFP or DFP, the TUSB544 will leave the U2 and U3 mode and transition to the Disconnect mode. It will also monitor for a valid LFPS. Upon detection of a valid LFPS, the TUSB544 will immediately transition to the U0 mode. In U2 and U3 mode, the TUSB544's receiver terminations will remain enabled but the TX DC common mode voltage will not be maintained.

When SLP\_S0# is asserted low it will disable Receiver Detect functionality. While SLP\_S0# is low and TUSB544 is in U2 and U3, TUSB544 will disable LOS and LFPS detection circuitry and RX termination for both channels will remain enabled. This allows even lower TUSB544 power consumption while in the U2 and U3 mode. Once SLP\_S0# is asserted high, the TUSB544 will again start performing far-end receiver detection as well as monitor LFPS so it can know when to exit the U2 and U3 mode.

When SLP\_S0# is asserted low and the TUSB544 is in Disconnect mode, the TUSB544 will remain in Disconnect mode and never perform far-end receiver detection. This allows even lower TUSB544 power consumption while in the Disconnect mode. Once SLP\_S0# is asserted high, the TUSB544 will again start performing far-end receiver detection so it can know when to exit the Disconnect mode.

### 7.4.9 Operation Timing – Power Up

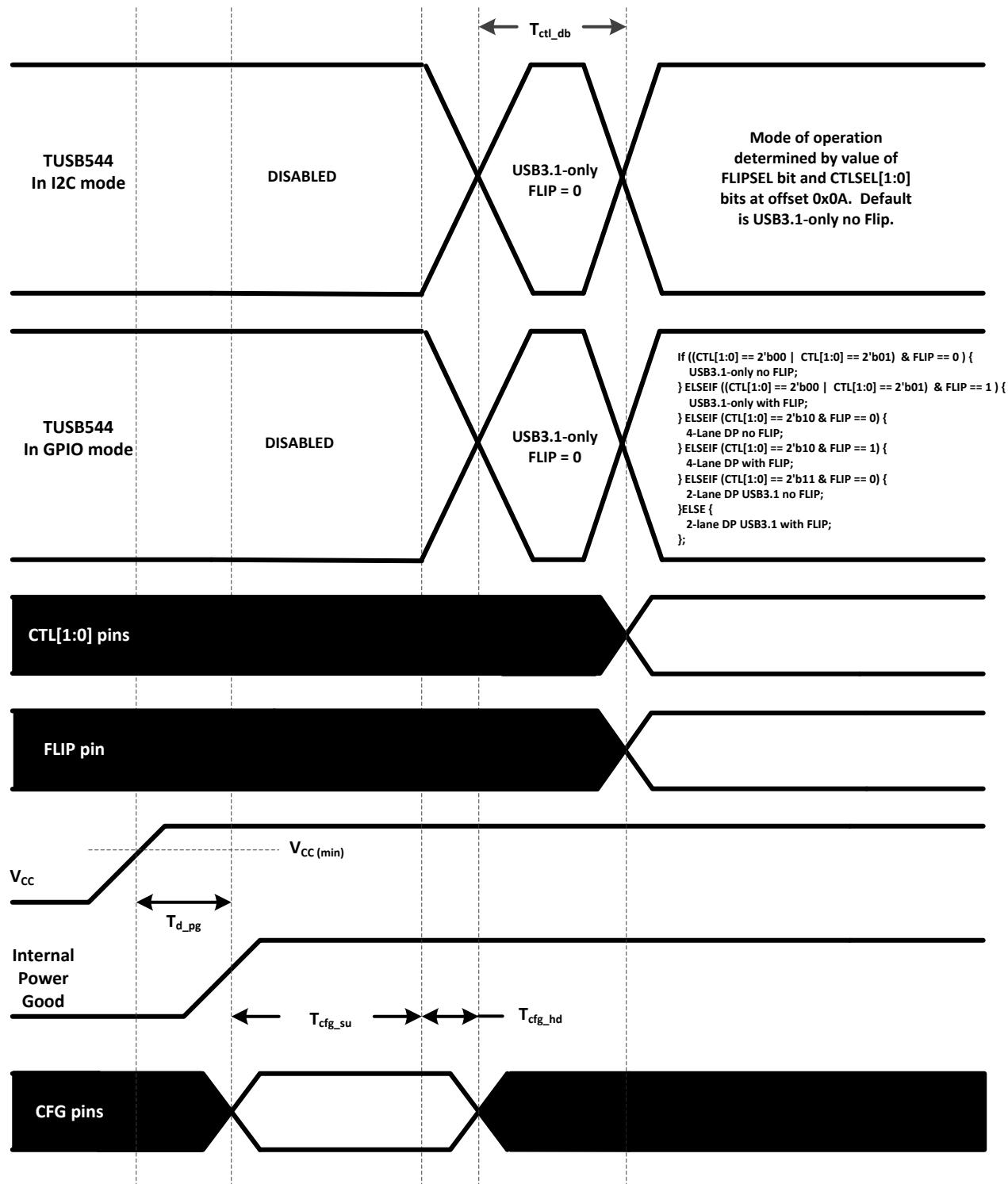


Figure 21. Power-Up Timing

**Table 9. Power-Up Timing**

PARAMETER		MIN	MAX	UNIT
$T_{d\_pg}$	$V_{CC}$ (min) to Internal Power Good asserted high		500	$\mu s$
$T_{cfg\_su}$	CFG <sup>(1)</sup> pins setup <sup>(2)</sup>	350		ms
$T_{cfg\_hd}$	CFG <sup>(1)</sup> pins hold	10		$\mu s$
$T_{CTL\_DB}$	CTL[1:0] and FLIP pin debounce		16	ms
$T_{VCC\_RAMP}$	VCC supply ramp requirement		100	ms

(1) Following pins comprise CFG pins: I2C\_EN, UEQ[1:0], DEQ[1:0], CFG[1:0], DIR[1:0], VIO\_SEL, SLP\_S0#, and SWAP.  
(2) Recommend CFG pins are stable when VCC is at min.

## 7.5 Programming

For further programmability, the TUSB544 can be controlled using I<sup>2</sup>C. The SCL and SDA terminals are used for I<sup>2</sup>C clock and I<sup>2</sup>C data respectively.

**Table 10. I<sup>2</sup>C Slave Address**

TUSB544 I <sup>2</sup> C Slave Address									
UEQ1/A1 Pin Level	UEQ0/A0 Pin Level	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)
0	0	1	0	0	0	1	0	0	0/1
0	R	1	0	0	0	1	0	1	0/1
0	F	1	0	0	0	1	1	0	0/1
0	1	1	0	0	0	1	1	1	0/1
R	0	0	1	0	0	0	0	0	0/1
R	R	0	1	0	0	0	0	1	0/1
R	F	0	1	0	0	0	1	0	0/1
R	1	0	1	0	0	0	1	1	0/1
F	0	0	0	1	0	0	0	0	0/1
F	R	0	0	1	0	0	0	1	0/1
F	F	0	0	1	0	0	1	0	0/1
F	1	0	0	1	0	0	1	1	0/1
1	0	0	0	0	1	1	0	0	0/1
1	R	0	0	0	1	1	0	1	0/1
1	F	0	0	0	1	1	1	0	0/1
1	1	0	0	0	1	1	1	1	0/1

### 7.5.1 The Following Procedure Should be Followed to Write to TUSB544 I<sup>2</sup>C Registers:

1. The master initiates a write operation by generating a start condition (S), followed by the TUSB544 7-bit address and a zero-value “W/R” bit to indicate a write cycle .
2. The TUSB544 acknowledges the address cycle.
3. The master presents the sub-address (I<sup>2</sup>C register within TUSB544) to be written, consisting of one byte of data, MSB-first.
4. The TUSB544 acknowledges the sub-address cycle.
5. The master presents the first byte of data to be written to the I<sup>2</sup>C register.
6. The TUSB544 acknowledges the byte transfer.
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TUSB544.
8. The master terminates the write operation by generating a stop condition (P).

### 7.5.2 The Following Procedure Should be Followed to Read the TUSB544 I<sup>2</sup>C Registers:

1. The master initiates a read operation by generating a start condition (S), followed by the TUSB544 7-bit address and a one-value “W/R” bit to indicate a read cycle
2. The TUSB544 acknowledges the address cycle.
3. The TUSB544 transmit the contents of the memory registers MSB-first starting at register 00h or last read sub-address+1. If a write to the T I<sup>2</sup>C register occurred prior to the read, then the TUSB544 shall start at the sub-address specified in the write.
4. The TUSB544 shall wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I<sup>2</sup>C master acknowledges reception of each data byte transfer.
5. If an ACK is received, the TUSB544 transmits the next byte of data.
6. The master terminates the read operation by generating a stop condition (P).

### 7.5.3 The Following Procedure Should be Followed for Setting a Starting Sub-Address for I<sup>2</sup>C Reads:

1. The master initiates a write operation by generating a start condition (S), followed by the TUSB544 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB544 acknowledges the address cycle.
3. The master presents the sub-address (I<sup>2</sup>C register within TUSB544) to be written, consisting of one byte of data, MSB-first.
4. The TUSB544 acknowledges the sub-address cycle.
5. The master terminates the write operation by generating a stop condition (P).

#### NOTE

If no sub-addressing is included for the read procedure, and reads start at register offset 00h and continue byte by byte through the registers until the I<sup>2</sup>C master terminates the read operation. If a I<sup>2</sup>C address write occurred prior to the read, then the reads start at the sub-address specified by the address write.

## 7.6 Register Maps

### 7.6.1 TUSB544 Registers

Table 11 lists the memory-mapped registers for the TUSB544. All register offset addresses not listed in Table 11 should be considered as reserved locations and the register contents should not be modified.

**Table 11. TUSB544 Registers**

Offset	Acronym	Register Name	Section
Ah	GENERAL_4	General Registers 4	<a href="#">Go</a>
Bh	GENERAL_5	General Register 5	<a href="#">Go</a>
Ch	GENERAL_6	General Register 6	<a href="#">Go</a>
10h	DISPLAYPORT_1	DisplayPort Control/Status Registers 1	<a href="#">Go</a>
11h	DISPLAYPORT_2	DisplayPort Control/Status Registers 2	<a href="#">Go</a>
12h	DISPLAYPORT_3	DisplayPort Control/Status Registers 3	<a href="#">Go</a>
13h	DISPLAYPORT_4	DisplayPort Control/Status Registers 4	<a href="#">Go</a>
1Bh	DISPLAYPORT_5	DisplayPort Control/Status Registers 5	<a href="#">Go</a>
20h	USB3.1_1	USB3.1 Control/Status Registers 1	<a href="#">Go</a>
21h	USB3.1_2	USB3.1 Control/Status Registers 2	<a href="#">Go</a>
22h	USB3.1_3	USB3.1 Control/Status Registers 3	<a href="#">Go</a>
23h	USB3.1_4	USB3.1 Control/Status Registers 4	<a href="#">Go</a>

Complex bit access types are encoded to fit into small table cells. [Table 12](#) shows the codes that are used for access types in this section.

**Table 12. TUSB544 Access Type Codes**

Access Type	Code	Description
<b>Read Type</b>		
R	R	Read
RU	R	Read
<b>Write Type</b>		
W	W	Write
WU	W	Write
<b>Reset or Default Value</b>		
-n		Value after reset or the default value

#### 7.6.1.1 **GENERAL\_4 Register (Offset = Ah) [reset = 1h]**

GENERAL\_4 is shown in [Figure 22](#) and described in [Table 13](#).

Return to [Summary Table](#).

**Figure 22. GENERAL\_4 Register**

7	6	5	4	3	2	1	0
RESERVED	CABLE_MODE	SWAP_SEL	EQ_OVERRIDE	HPDIN_OVERRIDE	FLIPSEL	CTLSEL[1:0]	
R-0h	0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-1h

**Table 13. GENERAL\_4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	CABLE_MODE		0h	0 – Normal mode of operation 1 – Cable mode of operation. DP lane activation is performed through AUX snooping and HPDIN status. If AUX snooping is disabled, 2 DP lanes are activated by default. 4 DP lanes are activated if USB SS is not detected.
5	SWAP_SEL	R/W	0h	Setting of this field performs global direction swap on all the channels 0 – Channel directions and EQ settings are in normal mode (Default) 1 – Reverse all channel directions and EQ settings for the input ports
4	EQ_OVERRIDE	R/W	0h	Setting of this field will allow software to use EQ settings from registers instead of value sample from pins. 0 – EQ settings based on sampled state of the EQ pins. 1 – EQ settings based on programmed value of each of the EQ registers
3	HPDIN_OVERRIDE	R/W	0h	0 – HPD IN based on state of HPD_IN pin (Default) 1 – HPD_IN high.
2	FLIPSEL	R/W	0h	FLIPSEL. Refer to Table 5 and Table 6 for this field functionality.
1-0	CTLSEL[1:0]	R/W	1h	00 – Disabled. All RX and TX for USB3 and DisplayPort are disabled. 01 – USB3.1 only enabled. (Default) 10 – Four DisplayPort lanes enabled. 11 – Two DisplayPort lanes and one USB3.1

### 7.6.1.2 GENERAL\_5 Register (Offset = Bh) [reset = 0h]

GENERAL\_5 is shown in Figure 23 and described in Table 14.

Return to [Summary Table](#).

**Figure 23. GENERAL\_5 Register**

7	6	5	4	3	2	1	0
RESERVED		RESERVED		CH_SWAP_SEL			
R-0h		R-0h			R/W-0h		

**Table 14. GENERAL\_5 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-4	RESERVED	R	0h	Reserved
3-0	CH_SWAP_SEL	R/W	0h	Setting of this field swaps direction (TX to RX and RX to TX) and EQ settings of individual channels. Channels are numbered 0 to 3 from top to bottom (see block diagram on Figure 8.1). 0 – Channel direction and EQ setting are in normal mode (Default) 1 – Reverse channel direction and EQ setting for the input port. For example, setting 0x0B[3:0] to 4b1100 swaps directions and EQ settings only on channels 2 and 3

### 7.6.1.3 GENERAL\_6 Register (Offset = Ch) [reset = 0h]

GENERAL\_6 is shown in Figure 24 and described in Table 15.

Return to [Summary Table](#).

**Figure 24. GENERAL\_6 Register**

7	6	5	4	3	2	1	0
RESERVED	VOD_DCGAIN_OVERRIDE		VOD_DCGAIN_SEL			DIR_SEL[1:0]	
R-0h		R/WU-0h			R/W-0h		

**Table 15. GENERAL\_6 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	VOD_DCGAIN_OVERRIDE	R/W	0h	Setting of this field will allow software to use VOD linearity range and DC gain settings from registers instead of value sampled from pins. 0 – VOD linearity range and DC gain settings based on sampled state of CFG[2:1] pins. 1 – EQ settings based on programmed value of each of the VOD linearity range and DC gain registers
5-2	VOD_DCGAIN_SEL	R/WU	0h	Field selects VOD linearity range and DC gain for all the channels and in all directions. When VOD_DCGAIN_OVERRIDE = 1'b0, this field reflects the sampled state of CFG[1:0] pins. When VOD_DCGAIN_OVERRIDE = 1'b1, software can change the VOD linearity range and DC gain for all the channels and in all directions based on value written to this field. Refer to Table 8.8. Each CFG is a 2-bit value. The register-to-CFG1/0 mapping is: [5:2] = {CFG1[1:0], CFG0[1:0]} where CFGx[1:0] mapping is: 00 = 0 01 = R 10 = F 11 = 1
1-0	DIR_SEL[1:0]	R/W	0h	DIR_SEL[1:0]. Sets operation mode 00 – USB + DP Alt Mode (source) (Default) 01 – USB + DP Alt Mode (sink) 10 – USB + Custom Alt Mode (source) 11 – USB + Custom Alt Mode (sink)

#### 7.6.1.4 DISPLAYPORT\_1 Register (Offset = 10h) [reset = 0h]

DISPLAYPORT is shown in [Figure 25](#) and described in [Table 16](#).

Return to [Summary Table](#).

**Figure 25. DISPLAYPORT Register**

7	6	5	4	3	2	1	0
UTX2EQ_SEL				URX2EQ_SEL			
R/WU-0h				R/WU-0h			

**Table 16. DISPLAYPORT Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	UTX2EQ_SEL	RWU	0h	Field selects between 0 to 9.4 dB of EQ for UTX2P/N pins. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of UEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for UTX2P/N pins based on value written to this field.
3-0	URX2EQ_SEL	RWU	0h	Field selects between 0 to 9.4 dB of EQ for URX2P/N pins. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of UEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for URX2P/N pins based on value written to this field.

#### 7.6.1.5 DISPLAYPORT\_2 Register (Offset = 11h) [reset = 0h]

DISPLAYPORT\_2 is shown in [Figure 26](#) and described in [Table 17](#).

Return to [Summary Table](#).

**Figure 26. DISPLAYPORT\_2 Register**

7	6	5	4	3	2	1	0
UTX1EQ_SEL				URX1EQ_SEL			
R/WU-0h				R/WU-0h			

**Table 17. DISPLAYPORT\_2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	UTX1EQ_SEL	R/WU	0h	Field selects between 0 to 9.4 dB of EQ for UTX1P/N pins. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of UEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for UTX1P/N pins based on value written to this field.
3-0	URX1EQ_SEL	R/WU	0h	Field selects between 0 to 9.4 dB of EQ for URX1P/N pins. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of UEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for URX1P/N pins based on value written to this field.

### 7.6.1.6 DISPLAYPORT\_3 Register (Offset = 12h) [reset = 0h]

DISPLAYPORT\_3 is shown in [Figure 27](#) and described in [Table 18](#).

Return to [Summary Table](#).

**Figure 27. DISPLAYPORT\_3 Register**

7	6	5	4	3	2	1	0
RESERVED	SET_POWER_STATE			LANE_COUNT_SET			
R-0h	RU-0h			RU-0h			

**Table 18. DISPLAYPORT\_3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-5	SET_POWER_STATE	RU	0h	This field represents the snooped value of the AUX write to DPCD address 0x00600. When AUX_SNOOP_DISABLE = 1'b0, the TUSB544 will enable/disable DP lanes based on the snooped value. When AUX_SNOOP_DISABLE = 1'b1, then DP lane enable/disable are determined by state of DPx_DISABLE registers, where x = 0, 1, 2, or 3. This field is reset to 2'b00 by hardware when CTLSEL1 changes from a 1'b1 to a 1'b0.
4-0	LANE_COUNT_SET	RU	0h	This field represents the snooped value of AUX write to DPCD address 0x00101 register. When AUX_SNOOP_DISABLE = 1'b0, TUSB544 will enable DP lanes specified by the snoop value. Unused DP lanes will be disabled to save power. When AUX_SNOOP_DISABLE = 1'b1, then DP lanes enable/disable are determined by DPx_DISABLE registers, where x = 0, 1, 2, or 3. This field is reset to 0x0 by hardware when CTLSEL1 changes from a 1'b1 to a 1'b0.

### 7.6.1.7 DISPLAYPORT\_4 Register (Offset = 13h) [reset = 0h]

DISPLAYPORT\_4 is shown in [Figure 28](#) and described in [Table 19](#).

Return to [Summary Table](#).

**Figure 28. DISPLAYPORT\_4 Register**

7	6	5	4	3	2	1	0
AUX_SNOOP_DISABLE	RESERVED	AUX_SBU_OVR		DP3_DISABLE	DP2_DISABLE	DP1_DISABLE	DP0_DISABLE
R/W-0h	R-0h	R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h

**Table 19. DISPLAYPORT\_4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	AUX_SNOOP_DISABLE	R/W	0h	0 – AUX snoop enabled. (Default) 1 – AUX snoop disabled.
6	RESERVED	R	0h	Reserved
5-4	AUX_SBU_OVR	R/W	0h	This field overrides the AUXP/N to SBU1/2 connect and disconnect based on CTL1 and FLIP. Changing this field to 1'b1 will allow traffic to pass through AUX to SBU regardless of the state of CTLSEL1 and FLIPSEL register. 00 – AUX to SBU connect/disconnect determined by CTLSEL1 and FLIPSEL (Default) 01 – AUXP -> SBU1 and AUXN -> SBU2 connection always enabled. 10 – AUXP -> SBU2 and AUXN -> SBU1 connection always enabled. 1 1 = AUX to SBU open.
3	DP3_DISABLE	R/W	0h	When AUX_SNOOP_DISABLE = 1b1, this field can be used to enable or disable DP lane 3. When AUX_SNOOP_DISABLE = 1b0, changes to this field will have no effect on lane 3 functionality. 0 – DP Lane 3 Enabled (default) 1 – DP Lane 3 Disabled.
2	DP2_DISABLE	R/W	0h	When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 2. When AUX_SNOOP_DISABLE = 1'b0, changes to this field will have no effect on lane 2 functionality. 0 – DP Lane 2 Enabled (default) 1 – DP Lane 2 Disabled.
1	DP1_DISABLE	R/W	0h	When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 1. When AUX_SNOOP_DISABLE = 1'b0, changes to this field will have no effect on lane 1 functionality. 0 – DP Lane 1 Enabled (default) 1 – DP Lane 1 Disabled.
0	DP0_DISABLE	R/W	0h	When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 0. When AUX_SNOOP_DISABLE = 1'b0, changes to this field will have no effect on lane 0 functionality. 0 – DP Lane 0 Enabled (default) 1 – DP Lane 0 Disabled.

### 7.6.1.8 DISPLAYPORT\_5 Register (Offset = 1Bh) [reset = 0h]

DISPLAYPORT\_5 is shown in [Figure 29](#) and described in [Table 20](#).

Return to [Summary Table](#).

**Figure 29. DISPLAYPORT\_5 Register**

7	6	5	4	3	2	1	0
I2C_RST					DPCD_RST		
0h					0h		

**Table 20. DISPLAYPORT\_5 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	I2C_RST		0h	Resets I2C registers to default values. This field is self-clearing.
3-0	DPCD_RST		0h	Resets DPCD registers to default values. This field is self-clearing.

### 7.6.1.9 USB3.1\_1 Register (Offset = 20h) [reset = 0h]

USB3.1 is shown in [Figure 30](#) and described in [Table 21](#).

Return to [Summary Table](#).

**Figure 30. USB3.1 Register**

7	6	5	4	3	2	1	0
DTX2EQ_SEL					DRX2EQ_SEL		
R/WU-0h					R/WU-0h		

**Table 21. USB3.1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	DTX2EQ_SEL	R/WU	0h	Field selects between 0 to 11 dB of EQ for DTX2P/N pins. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DTX2P/N pins based on value written to this field.
3-0	DRX2EQ_SEL	R/WU	0h	Field selects between 0 to 11 dB of EQ for DRX2P/N pins. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DRX2P/N pins based on value written to this field.

### 7.6.1.10 USB3.1\_2 Register (Offset = 21h) [reset = 0h]

USB3.1\_2 is shown in [Figure 31](#) and described in [Table 22](#).

Return to [Summary Table](#).

**Figure 31. USB3.1\_2 Register**

7	6	5	4	3	2	1	0
DTX1EQ_SEL				DRX1EQ_SEL			
R/W-0h				R/WU-0h			

**Table 22. USB3.1\_2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	DTX1EQ_SEL	R/W	0h	Field selects between 0 to 11 dB of EQ for DTX1P/N pins. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DTX1P/N pins based on value written to this field.
3-0	DRX1EQ_SEL	R/WU	0h	Field selects between 0 to 11 dB of EQ for DRX1P/N pins. When EQ_OVERRIDE = 1'b0, this field reflects the sampled state of DEQ[1:0] pins. When EQ_OVERRIDE = 1'b1, software can change the EQ setting for DRX1P/N pins based on value written to this field.

### 7.6.1.11 USB3.1\_3 Register (Offset = 22h) [reset = 0h]

USB3.1\_3 is shown in [Figure 32](#) and described in [Table 23](#).

Return to [Summary Table](#).

**Figure 32. USB3.1\_3 Register**

7	6	5	4	3	2	1	0
CM_ACTIVE		LFPS_EQ	U2U3_LFPS_D	DISABLE_U2U3_RXDET		DFP_RXDET_INTERVAL	USB3_COMPLIANCE_CTRL
R/WU-0h		R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h

**Table 23. USB3.1\_3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	CM_ACTIVE	R/WU	0h	0 - device not in USB 3.1 compliance mode. (Default) 1 - device in USB 3.1 compliance mode
6	LFPS_EQ	R/W	0h	Controls whether settings of EQ based on URX[2:1]EQ_SEL, UTX[2:1]EQ_SEL, DRX[2:1]EQ_SEL, and DTX[2:1]EQ_SEL applies to received LFPS signal. 0 - EQ set to zero when receiving LFPS (default) 1 - EQ set by the related registers when receiving LFPS.
5	U2U3_LFPS_DEBOUNCE	R/W	0h	0 - No debounce of LFPS before U2/U3 exit. (Default) 1 - 200us debounce of LFPS before U2/U3 exit.
4	DISABLE_U2U3_RXDET	R/W	0h	0 - Rx.Detect in U2/U3 enabled. (Default) 1 - Rx.Detect in U2/U3 disabled.
3-2	DFP_RXDET_INTERVAL	R/W	0h	This field controls the Rx.Detect interval for the Downstream facing port (TX1P/N and TX2P/N). 00 - 8 ms 01 - 12 ms (default) 10 - Reserved 11 - Reserved
1-0	USB3_COMPLIANCE_CTRL	R/W	0h	00 - FSM determined compliance mode. (Default) 01 - Compliance Mode enabled in DFP direction (UTX1/UTX2 DTX1/DTX2) 10 - Compliance Mode enabled in UFP direction (DRX1/DRX2 URX1/URX2) 11 - Compliance Mode Disabled.

### 7.6.1.12 USB3.1\_4 Register (Offset = 23h) [reset = 0h]

USB3.1\_4 is shown in [Figure 33](#) and described in [Table 24](#).

Return to [Summary Table](#).

**Figure 33. USB3.1\_4 Register**

7	6	5	4	3	2	1	0
RESERVED		CFG_LOS_HYST			CFG_LOS_VTH		
R-0h			R/W-0h			R/W-0h	

**Table 24. USB3.1\_4 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-3	CFG_LOS_HYST	R/W	0h	Controls LOS hysteresis defined as 20 log (LOS de-assert threshold/LOS assert threshold). 000 - 0.15 dB 001 - 0.85 dB 010 - 1.45 dB 011 - 2.00 dB 100 - 2.70 dB (default) 101 - 3.00 dB 110 - 3.40 dB 111 - 3.80 dB
2-0	CFG_LOS_VTH	R/W	0h	Controls LOS assert threshold voltage 000 - 67 mV 001 - 72 mV 010 - 79 mV 011 - 85 mV (default) 100 - 91 mV 101 - 97 mV 110 - 105 mV 111 - 112 mV

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TUSB544 is a linear redriver designed specifically to compensate for intersymbol interference (ISI) jitter caused by signal attenuation through a passive medium like PCB traces and cables. Because the TUSB544 has four independent inputs, it can be optimized to correct ISI on all those seven inputs through 16 different equalization choices. Placing the TUSB544 between a USB3.1 Host/DisplayPort 1.4 GPU and a USB3.1 Type-C receptacle can correct signal integrity issues resulting in a more robust system.

### 8.2 Typical Application

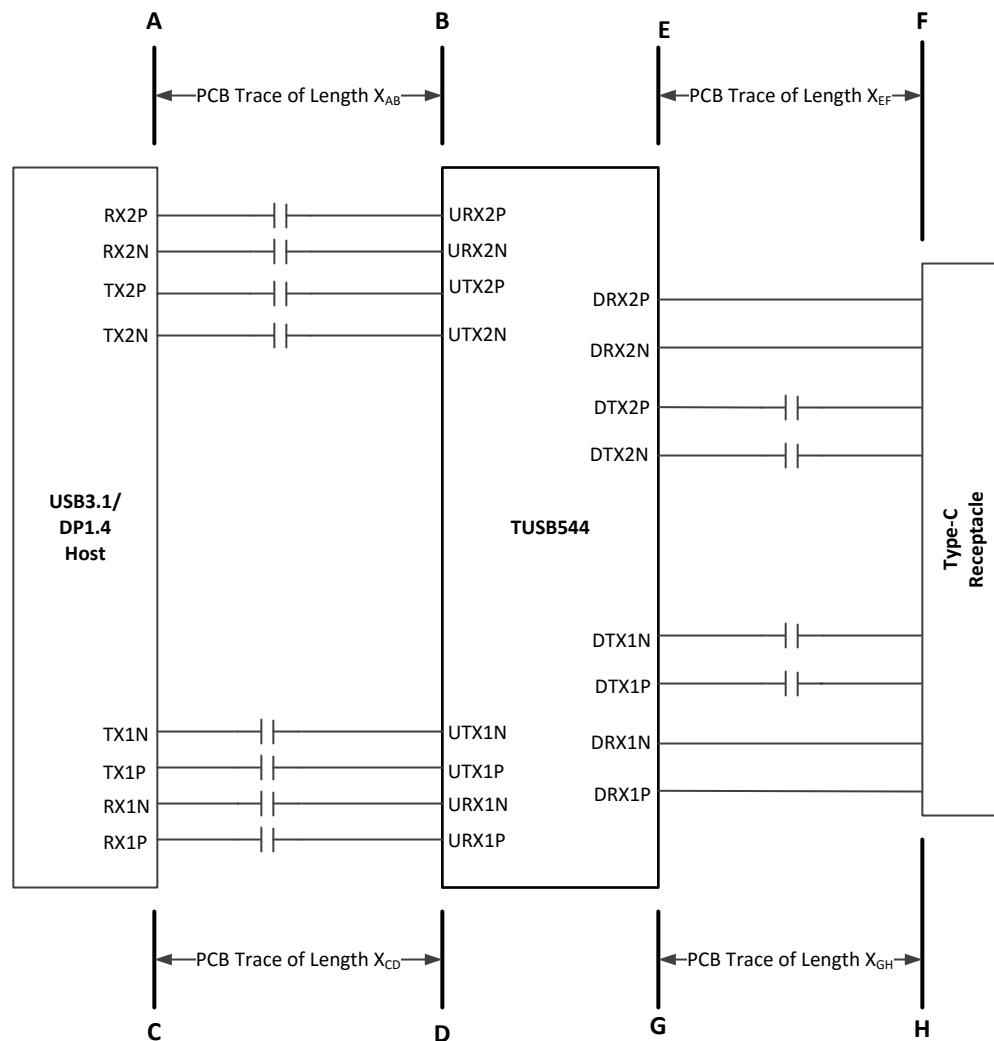


Figure 34. TUSB544 in a Host Application

## Typical Application (continued)

### 8.2.1 Design Requirements

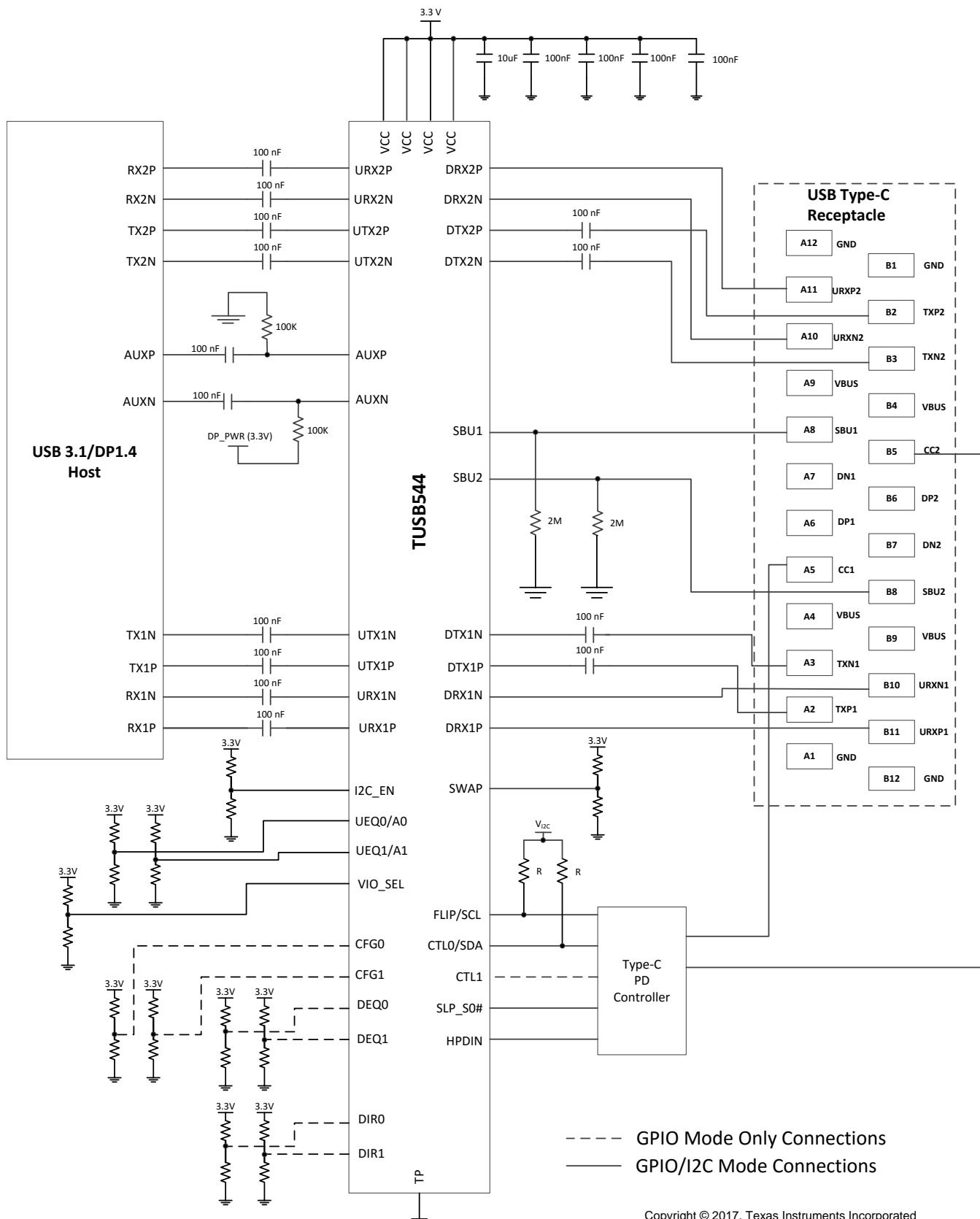
For this design example, use the parameters shown in [Table 25](#).

**Table 25. Design Parameters**

PARAMETER	VALUE
A to B PCB trace length, X <sub>AB</sub>	12 inches
C to D PCB trace length, X <sub>CD</sub>	12 inches
E to F PCB trace length, X <sub>EF</sub>	2 inches
G to H PCB trace length, X <sub>GH</sub>	2 inches
PCB trace width	4 mils
AC-coupling capacitor (75 nF to 265 nF)	100 nF
VCC supply (3 V to 3.6 V)	3.3 V
I <sup>2</sup> C Mode or GPIO Mode	I <sup>2</sup> C Mode. (I <sup>2</sup> C_EN pin != "0")
1.8V or 3.3V I <sup>2</sup> C Interface	3.3V I <sup>2</sup> C. Pull-up the I <sup>2</sup> C_EN pin to 3.3V with a 1K ohm resistor.

### 8.2.2 Detailed Design Procedure

A typical usage of the TUSB544 device is shown in [Figure 35](#). The device can be controlled either through its GPIO pins or through its I<sup>2</sup>C interface. In the example shown below, a Type-C PD controller is used to configure the device through the I<sup>2</sup>C interface. In I<sup>2</sup>C mode, the equalization settings for each receiver can be independently controlled through I<sup>2</sup>C registers. For this reason, all of the equalization pins (UEQ[1:0] and DEQ[1:0]) can be left unconnected. If these pins are left unconnected, the TUSB544 7-bit I<sup>2</sup>C slave address will be 0x12 because both UEQ1/A1 and UEQ0/A0 will be at pin level "F". If a different I<sup>2</sup>C slave address is desired, UEQ1/A1 and UEQ0/A0 pins should be set to a level which produces the desired I<sup>2</sup>C slave address.



Copyright © 2017, Texas Instruments Incorporated

### 8.2.3 Application Curve

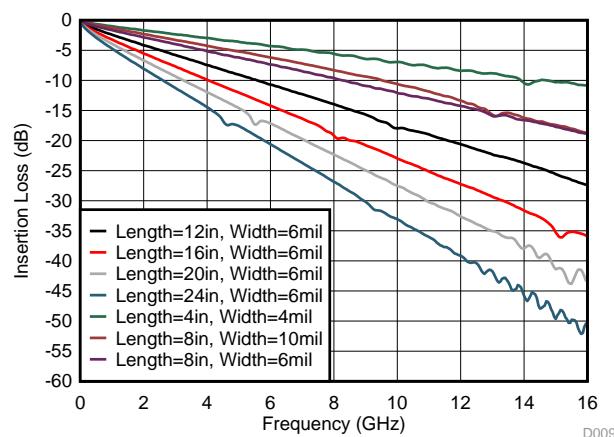
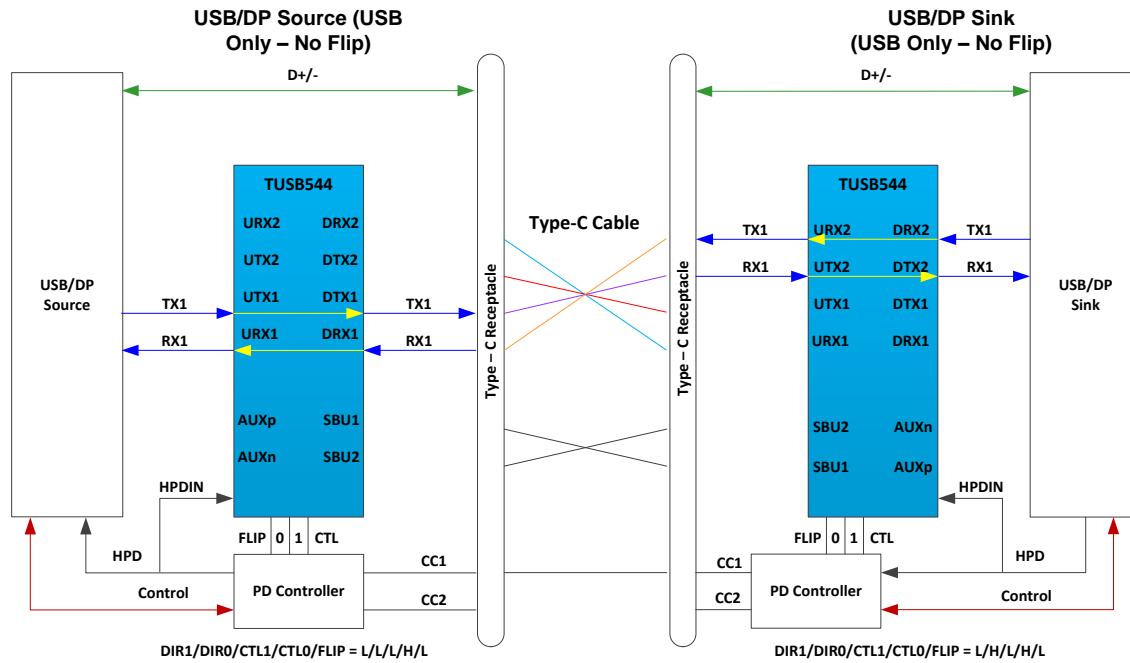


Figure 36. Insertion Loss of FR4 PCB Traces

## 8.3 System Examples

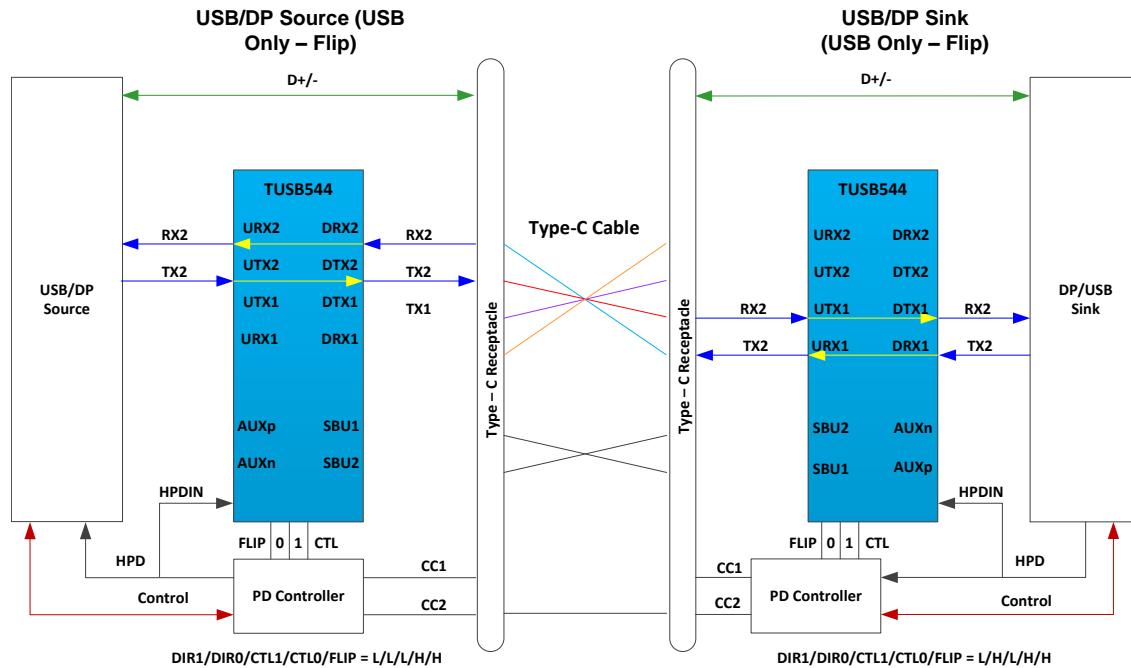
### 8.3.1 USB 3.1 only (USB/DP Alternate Mode)

The TUSB544 will be in USB3.1 only when the CTL1 pin is low and CTL0 pin is high.



Copyright © 2017, Texas Instruments Incorporated

**Figure 37. USB3.1 Only – No Flip**

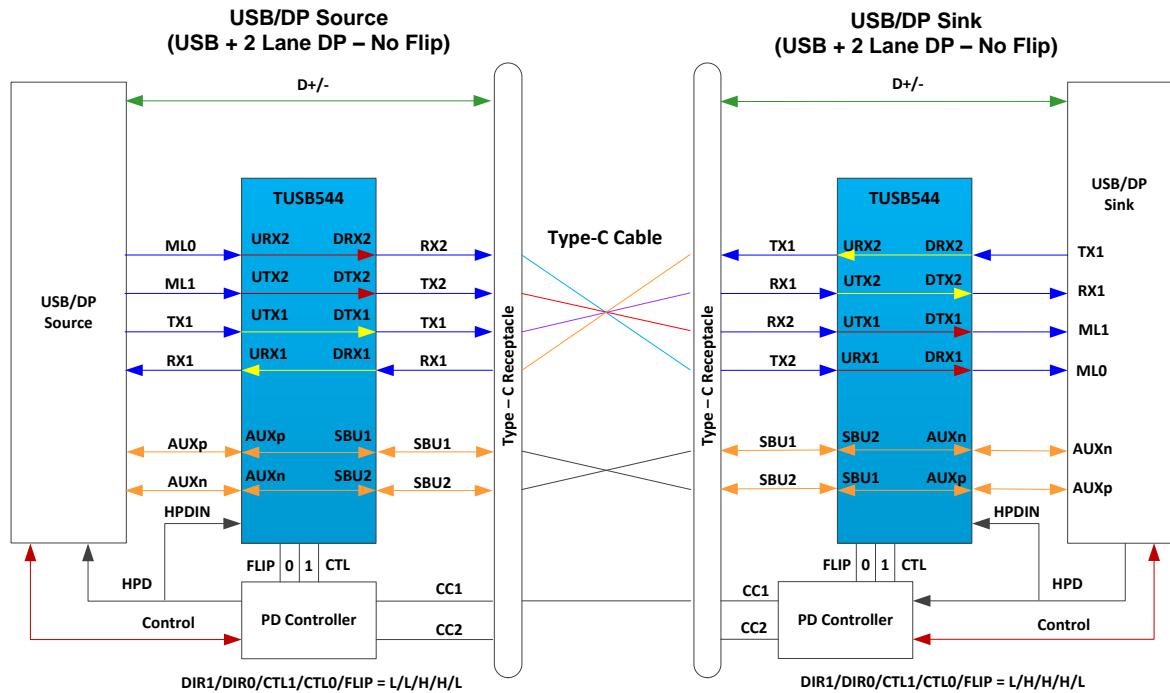


Copyright © 2017, Texas Instruments Incorporated

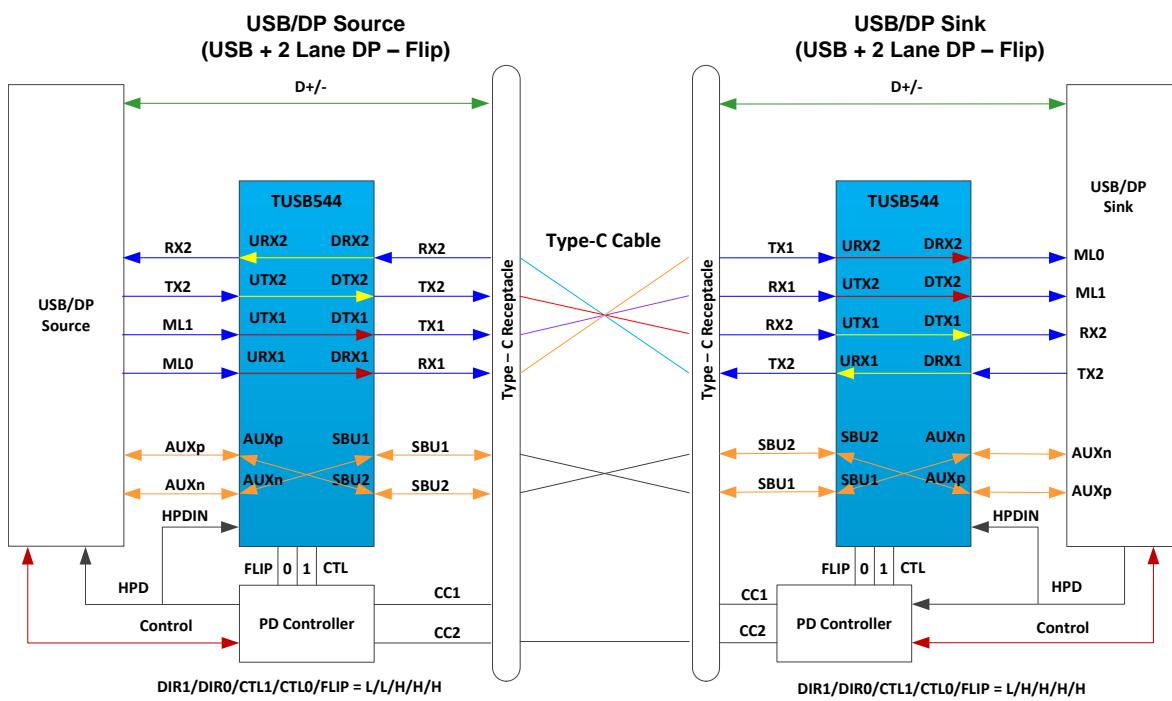
**Figure 38. USB3.1 Only – With Flip**

## System Examples (continued)

### 8.3.2 USB3.1 and 2 lanes of DisplayPort



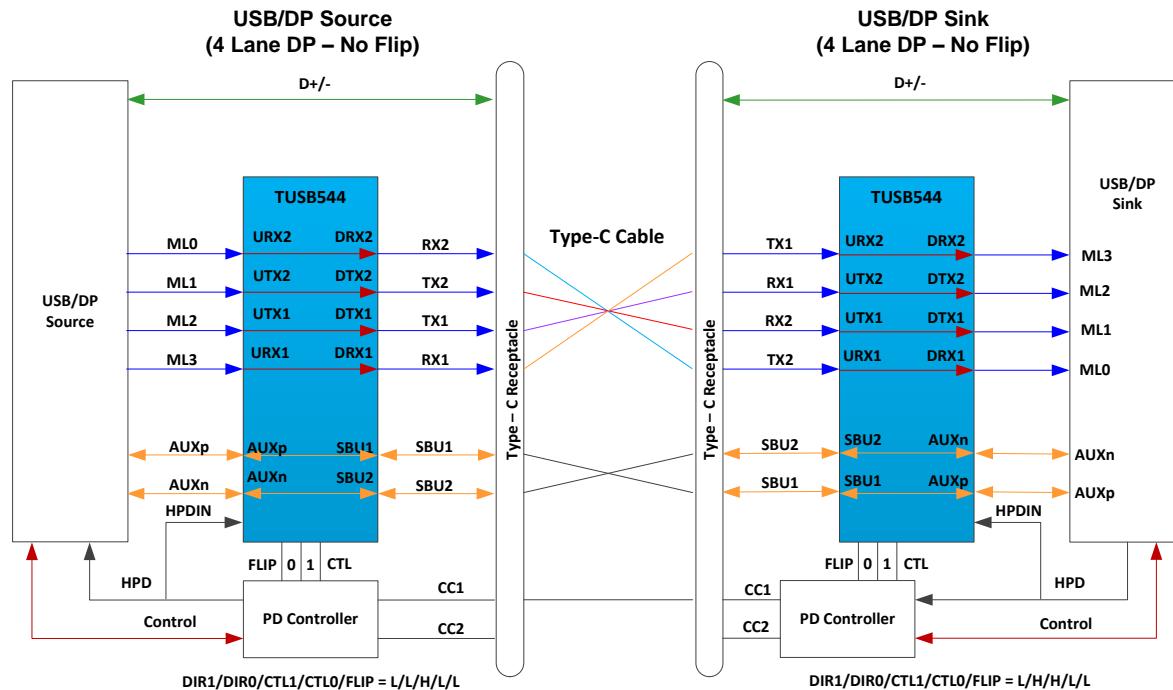
**Figure 39. USB3.1 + 2 Lane DP – No Flip**



**Figure 40. USB 3.1 + 2 Lane DP – Flip**

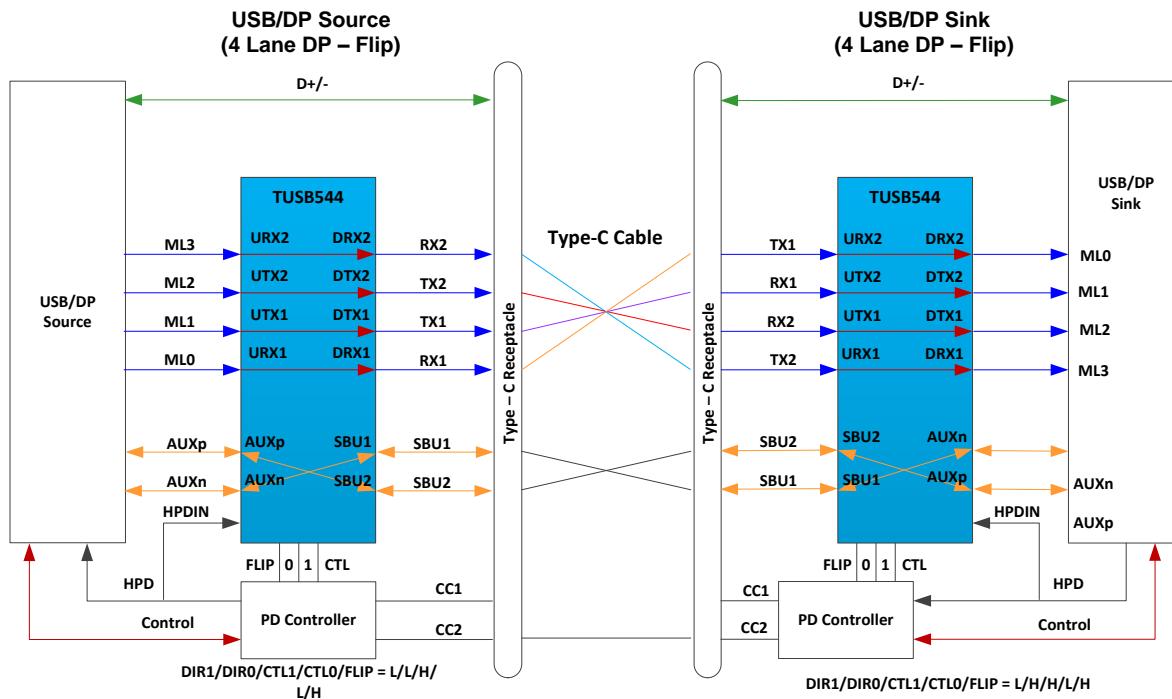
## System Examples (continued)

### 8.3.3 DisplayPort Only



Copyright © 2017, Texas Instruments Incorporated

**Figure 41. Four Lane DP – No Flip**

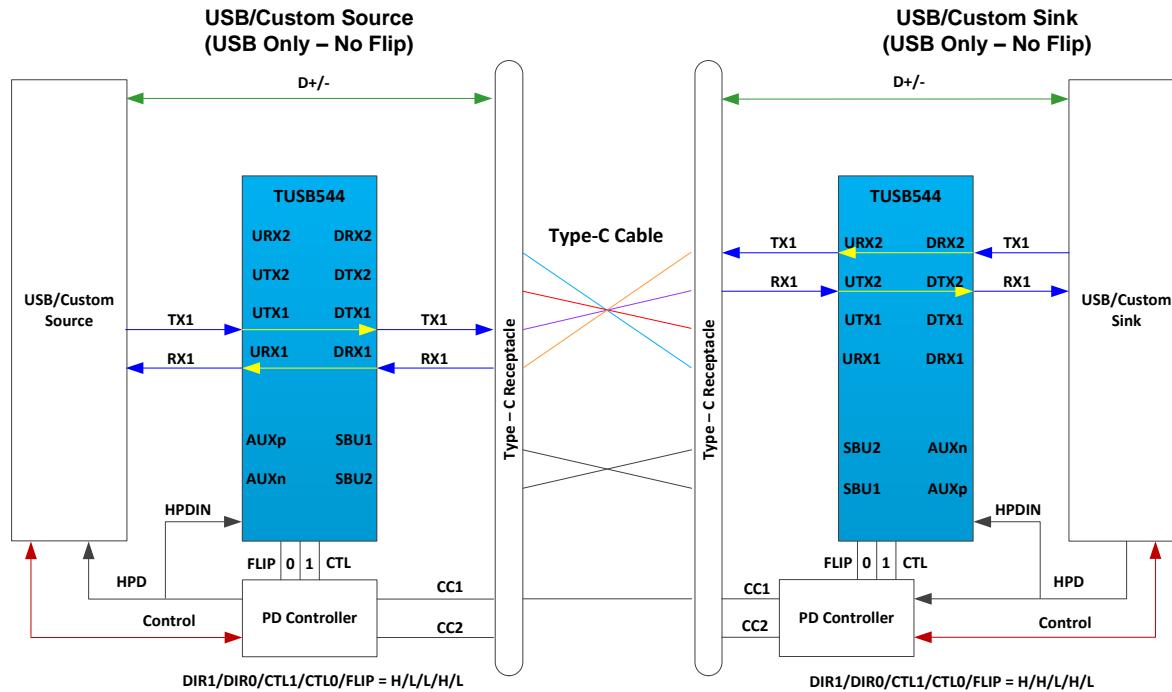


Copyright © 2017, Texas Instruments Incorporated

**Figure 42. Four Lane DP – With Flip**

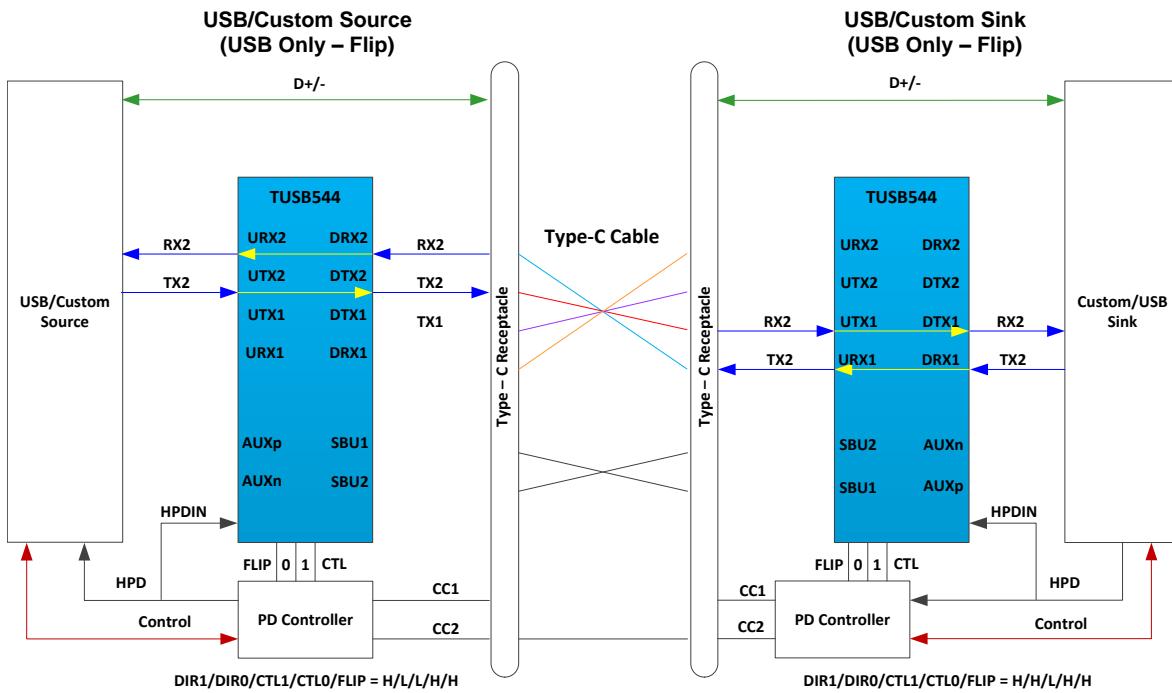
## System Examples (continued)

### 8.3.4 USB 3.1 only (USB/Custom Alternate Mode)



Copyright © 2017, Texas Instruments Incorporated

**Figure 43. USB3.1 Only – No Flip**

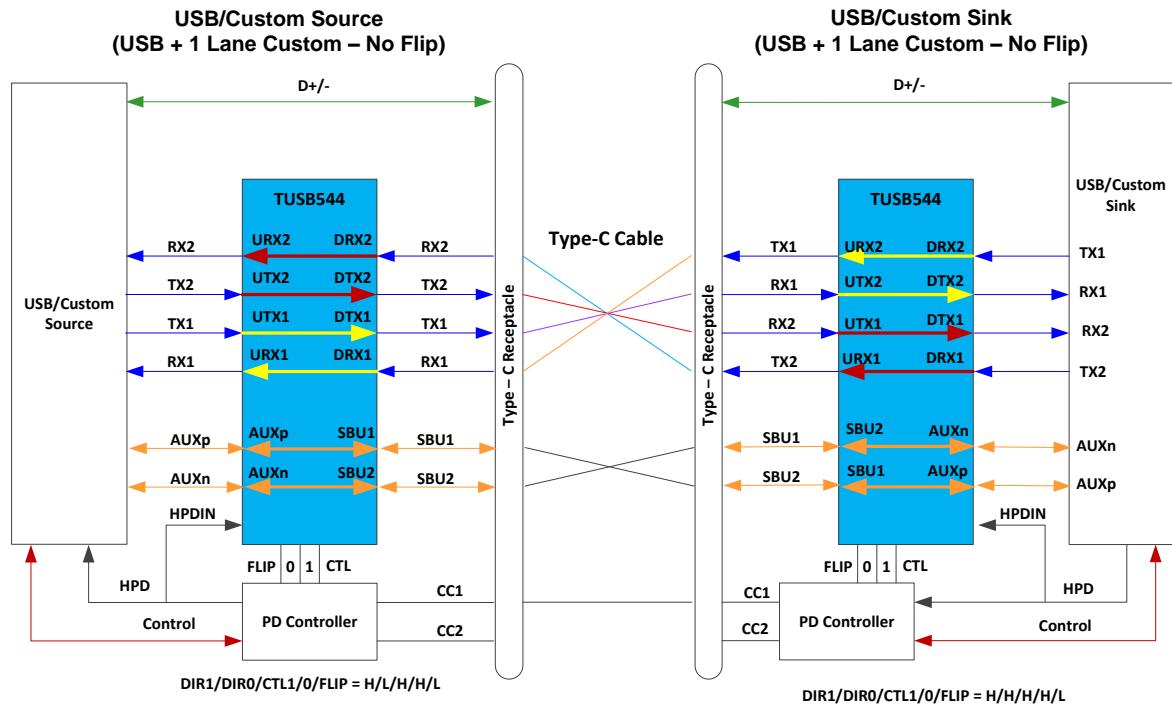


Copyright © 2017, Texas Instruments Incorporated

**Figure 44. USB3.1 Only – With Flip**

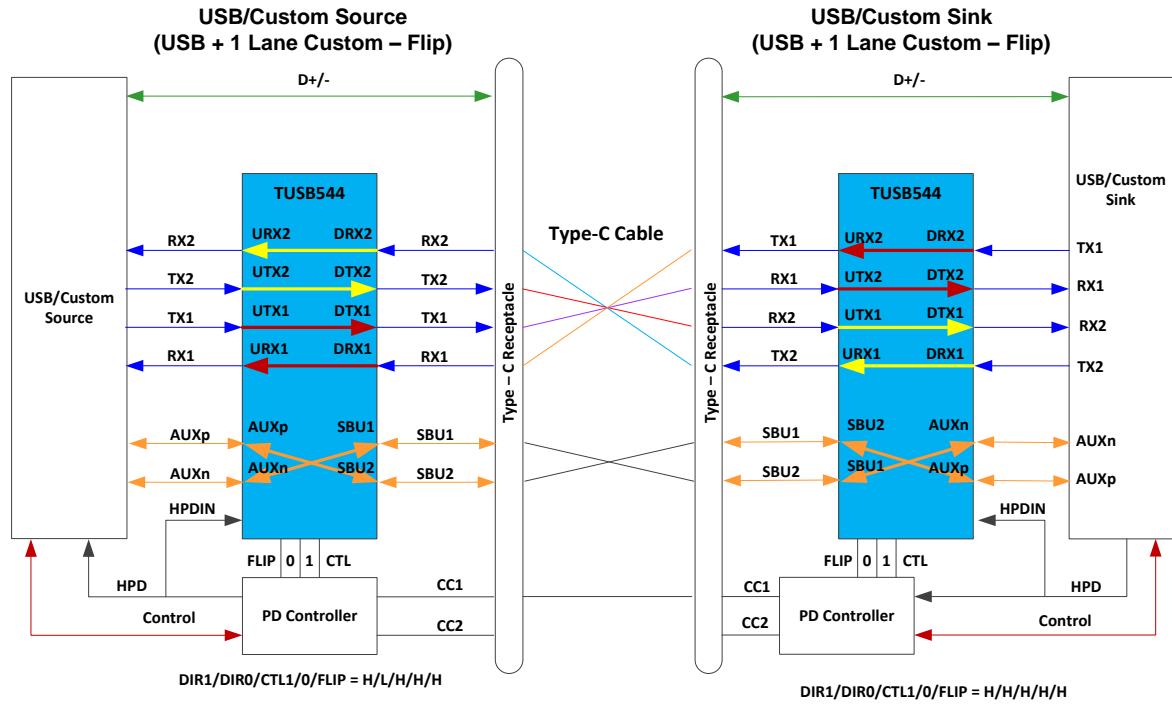
## System Examples (continued)

### 8.3.5 USB3.1 and 1 Lane of Custom Alt Mode



Copyright © 2017, Texas Instruments Incorporated

**Figure 45. USB3.1 + 1 Lane Custom Alt Mode – No Flip**



Copyright © 2017, Texas Instruments Incorporated

**Figure 46. USB 3.1 + 1 Lane Custom Alt. Mode – Flip**

## System Examples (continued)

### 8.3.6 USB3.1 and 2 Lane of Custom Alt Mode

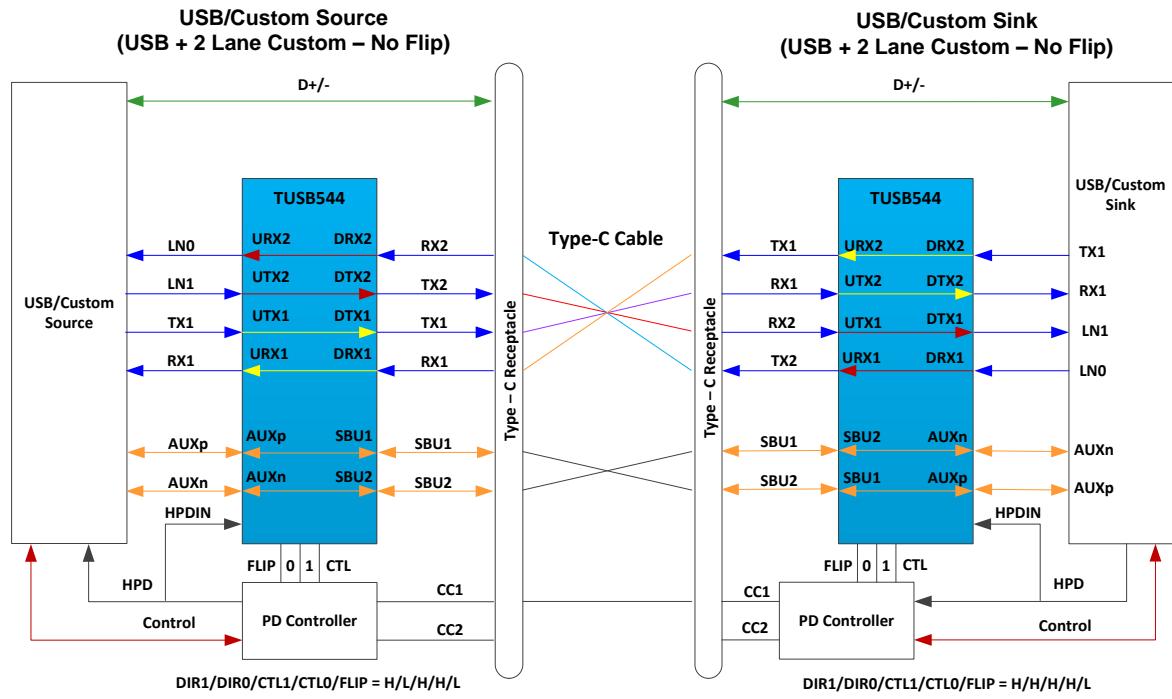


Figure 47. Two Lane Custom Alternate Mode – No Flip

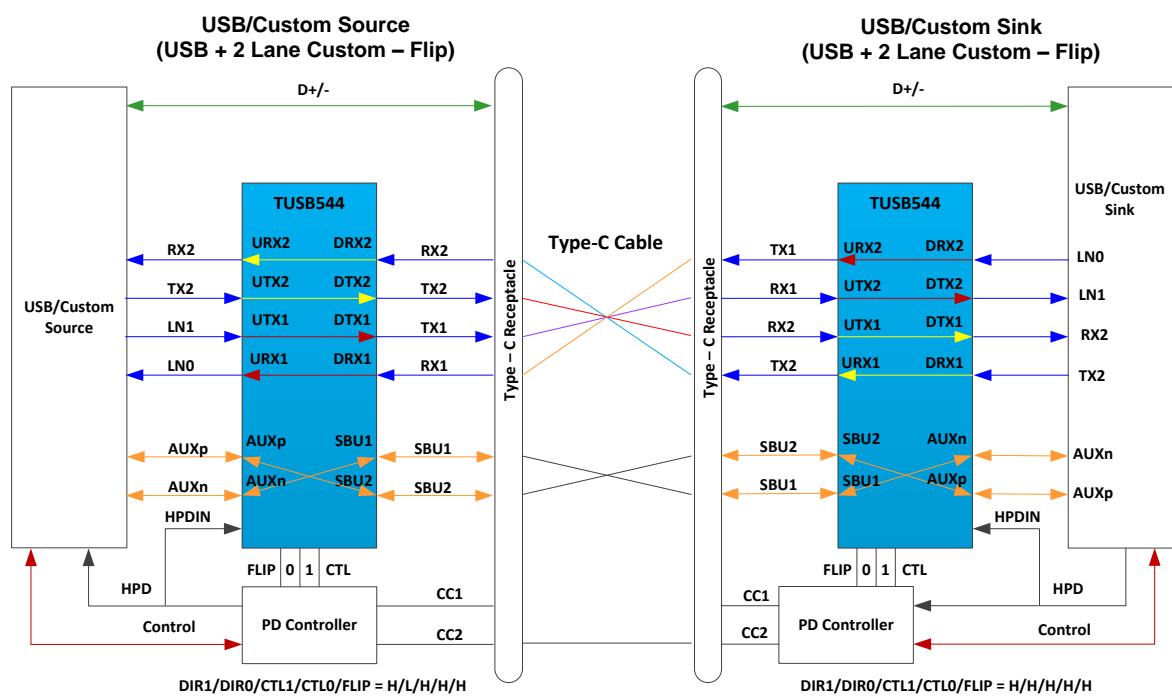
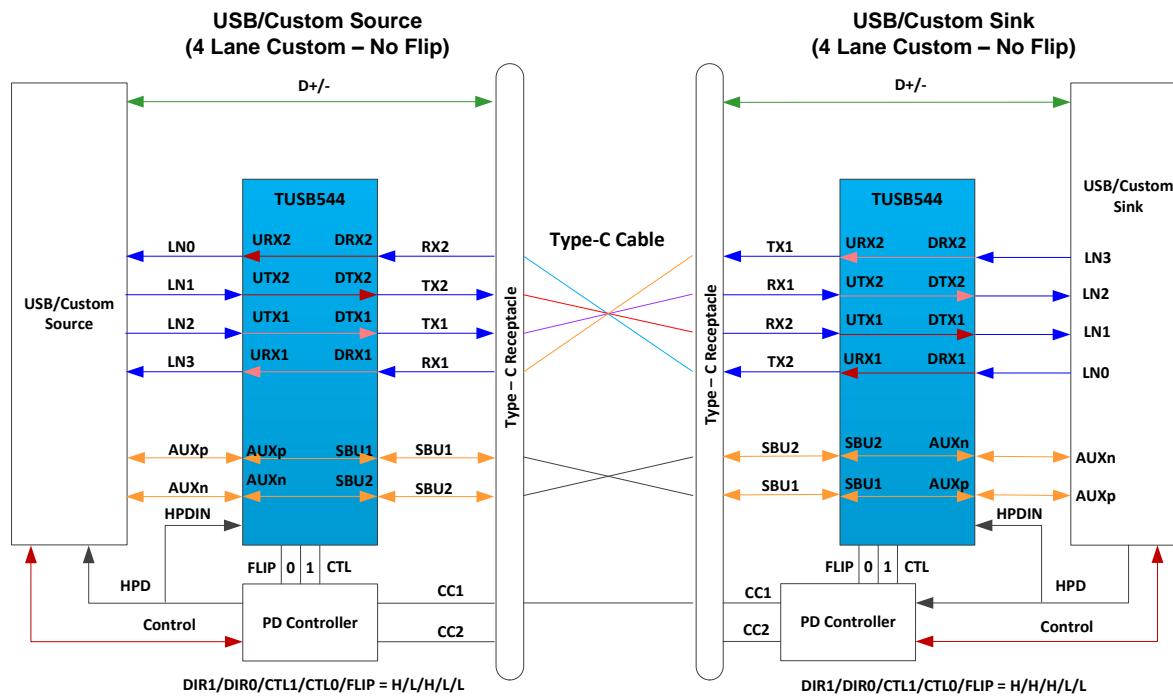


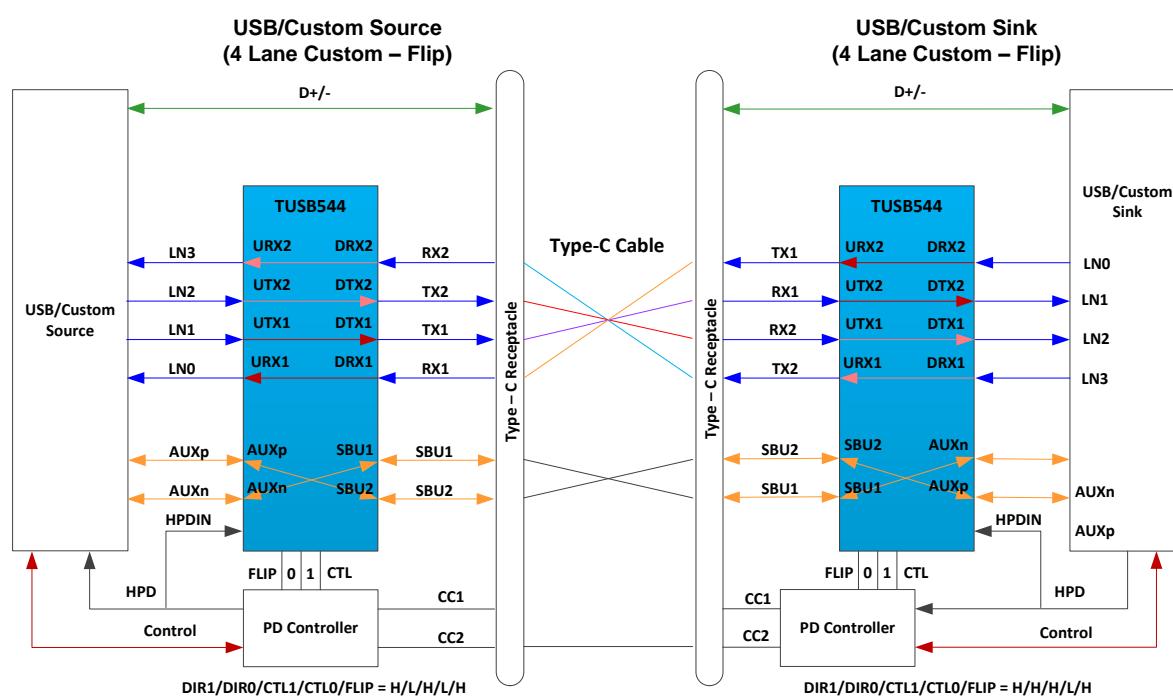
Figure 48. Two Lane Custom Alternate Mode – With Flip

## System Examples (continued)

### 8.3.7 USB3.1 and 4 Lane of Custom Alt Mode



**Figure 49. Four Lane Custom Alternate Mode – No Flip**



**Figure 50. Four Lane Custom Alternate Mode – With Flip**

## 9 Power Supply Recommendations

The TUSB544 is designed to operate with a 3.3 V power supply. Levels above those listed in the *Absolute Maximum Ratings* table should not be used. If using a higher voltage system power supply, a voltage regulator can be used to step down to 3.3 V. Decoupling capacitors should be used to reduce noise and improve power supply integrity. A 0.1- $\mu$ F capacitor should be used on each power pin.

## 10 Layout

### 10.1 Layout Guidelines

1. RXP/N and TXP/N pairs should be routed with controlled 90-Ohm differential impedance (+/- 15%).
2. Keep away from other high speed signals.
3. Intra-pair routing should be kept to within 2 mils.
4. Length matching should be near the location of mismatch.
5. Each pair should be separated at least by 3 times the signal trace width.
6. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be  $\geq 135$  degrees. This will minimize any length mismatch causes by the bends and therefore minimize the impact bends have on EMI.
7. Route all differential pairs on the same of layer.
8. The number of VIAS should be kept to a minimum. It is recommended to keep the VIAS count to 2 or less.
9. Keep traces on layers adjacent to ground plane.
10. Do NOT route differential pairs over any plane split.
11. Adding Test points will cause impedance discontinuity; and therefore, negatively impacts signal performance. If test points are used, the test points should be placed in series and symmetrically. The test points must not be placed in a manner that causes a stub on the differential pair.

### 10.2 Layout Example

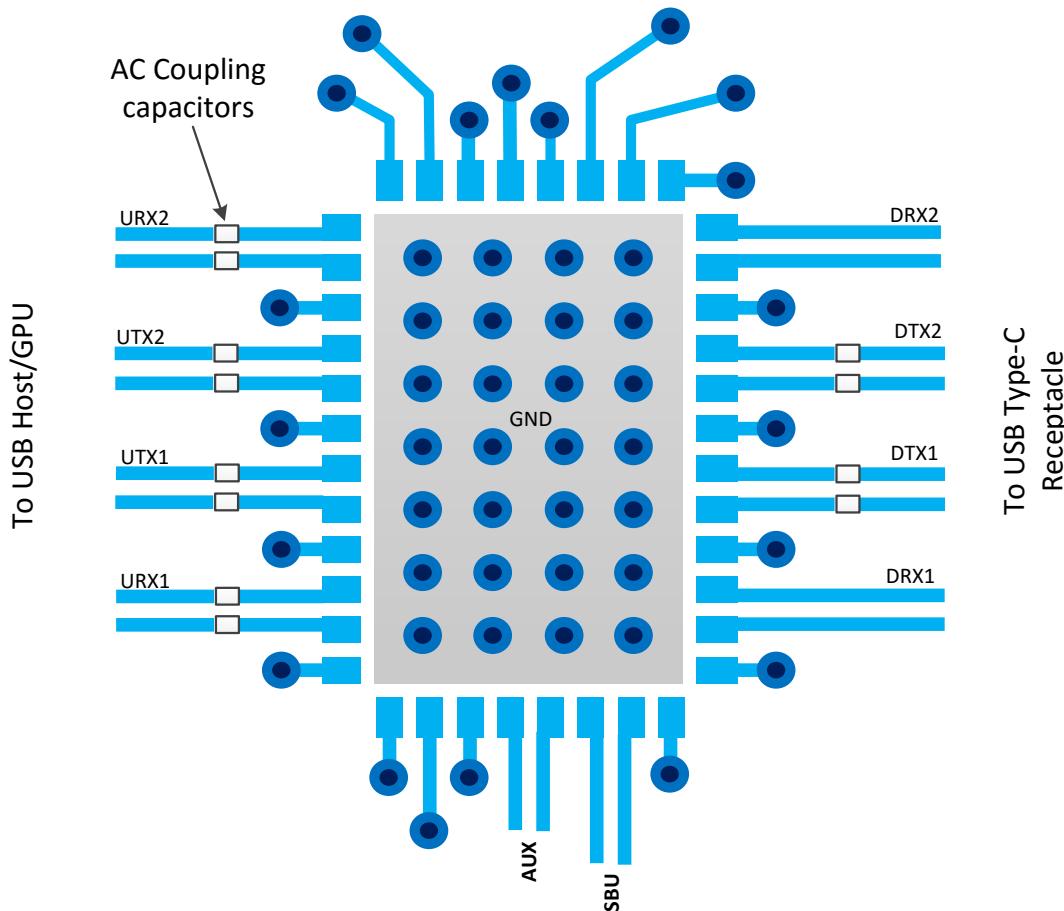


Figure 51.

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

The documents identified in this section are referenced within this specification. Most references with the text will use a document tag, identified as [Document Tag], instead of the complete document title to simplify the text.

For related documentation see the following:

- [USB31] Universal Serial Bus 3.1 Specification.
- [TYPEC] Universal Serial Bus Type C Cable and Connector Specification

### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** **TI's Engineer-to-Engineer (E2E) Community.** Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** **TI's Design Support** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 11.5 Electrostatic Discharge Caution

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

 ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.6 Glossary

[SLYZ022](#) — **TI Glossary.**

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB544IRNQR	ACTIVE	WQFN	RNQ	40	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		TUSB544	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TUSB544IRNQT	ACTIVE	WQFN	RNQ	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		TUSB544	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
TUSB544RNQR	PREVIEW	WQFN	RNQ	40	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	TUSB544	
TUSB544RNQT	PREVIEW	WQFN	RNQ	40	300	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	TUSB544	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and



www.ti.com

## PACKAGE OPTION ADDENDUM

1-Jul-2017

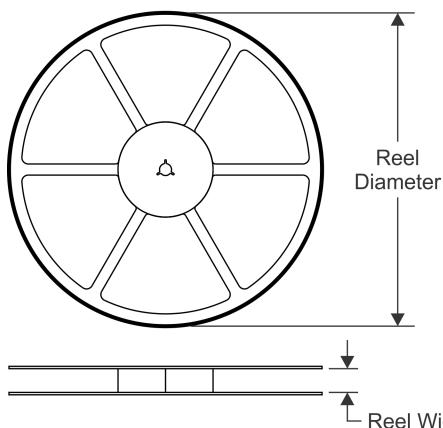
---

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

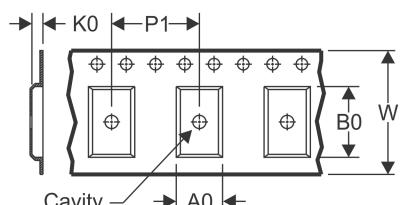
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

## REEL DIMENSIONS

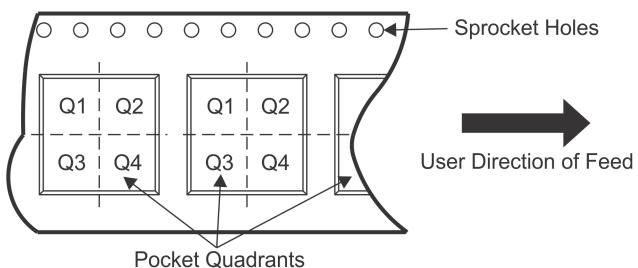


## TAPE DIMENSIONS



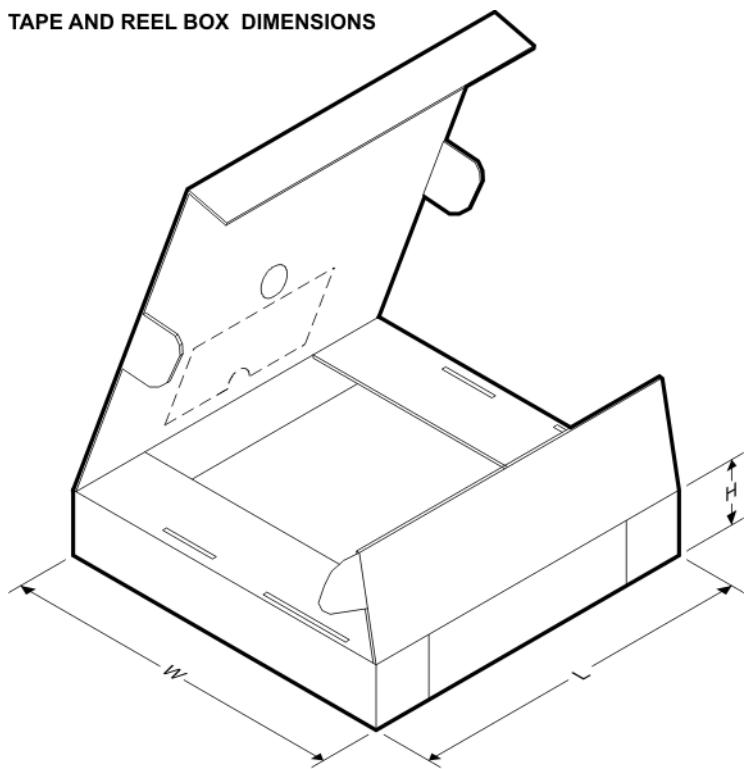
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

All dimensions are nominal													
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant	
TUSB544IRNQR	WQFN	RNQ	40	3000	330.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2	
TUSB544IRNQT	WQFN	RNQ	40	250	180.0	12.4	4.3	6.3	1.1	8.0	12.0	Q2	

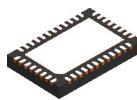
**TAPE AND REEL BOX DIMENSIONS**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB544IRNQR	WQFN	RNQ	40	3000	367.0	367.0	35.0
TUSB544IRNQT	WQFN	RNQ	40	250	210.0	185.0	35.0

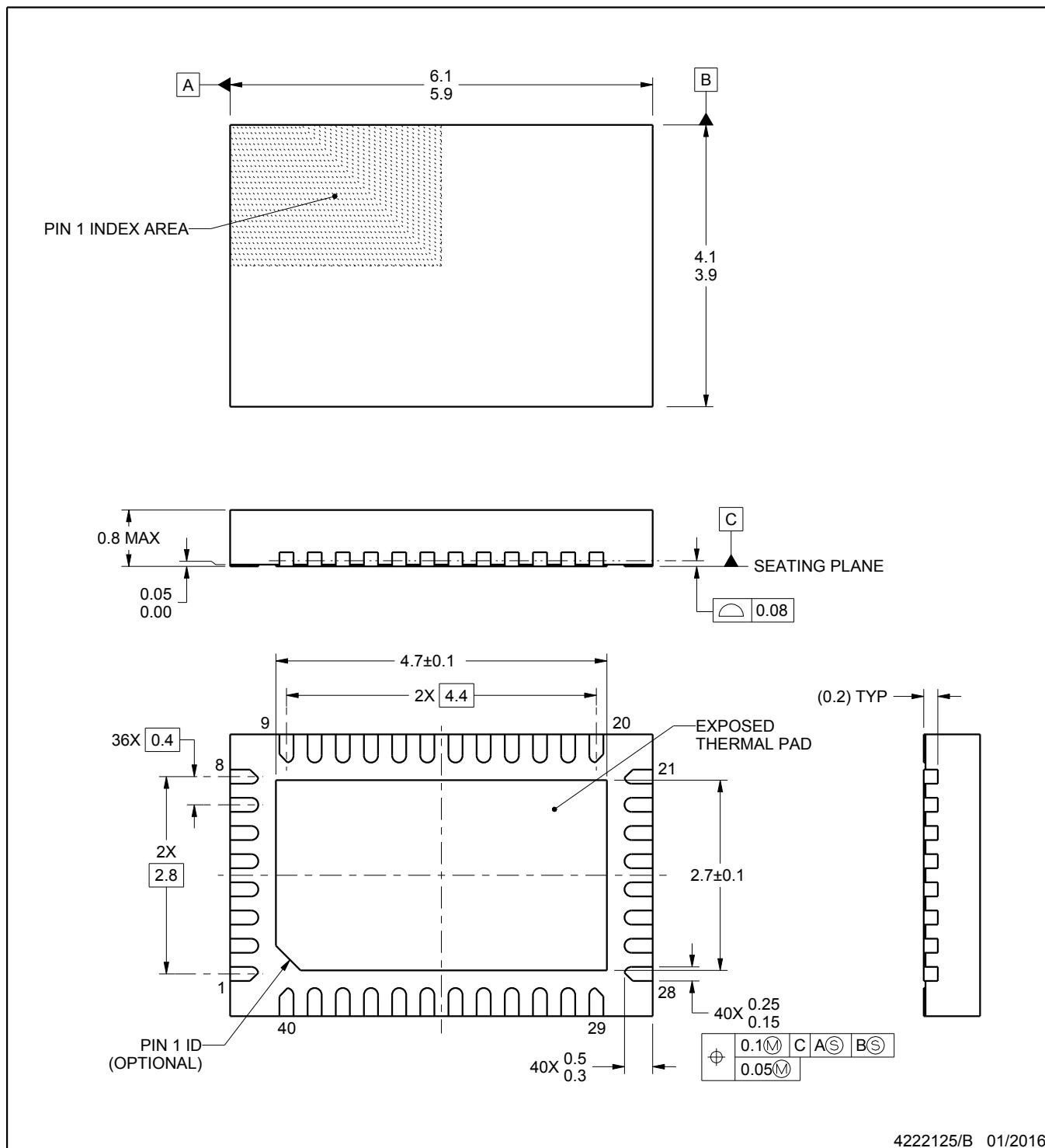
# PACKAGE OUTLINE

RNQ0040A



WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4222125/B 01/2016

## NOTES:

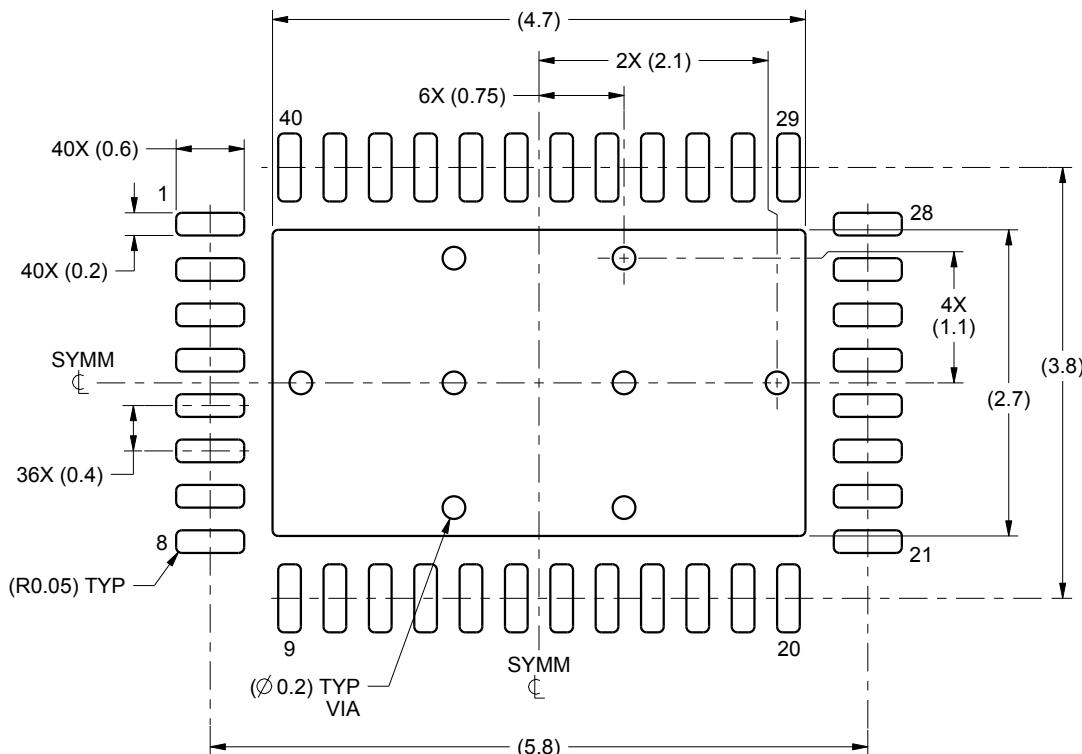
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

## EXAMPLE BOARD LAYOUT

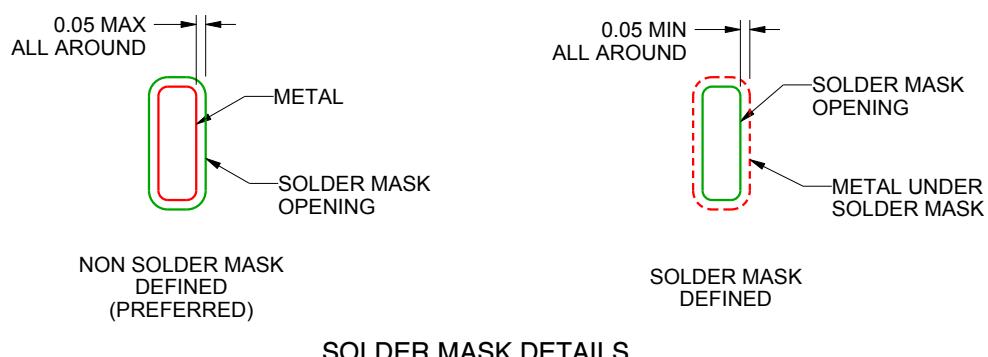
**RNQ0040A**

## **WQFN - 0.8 mm max height**

#### PLASTIC QUAD FLATPACK - NO LEAD



## LAND PATTERN EXAMPLE



4222125/B 01/2016

#### NOTES: (continued)

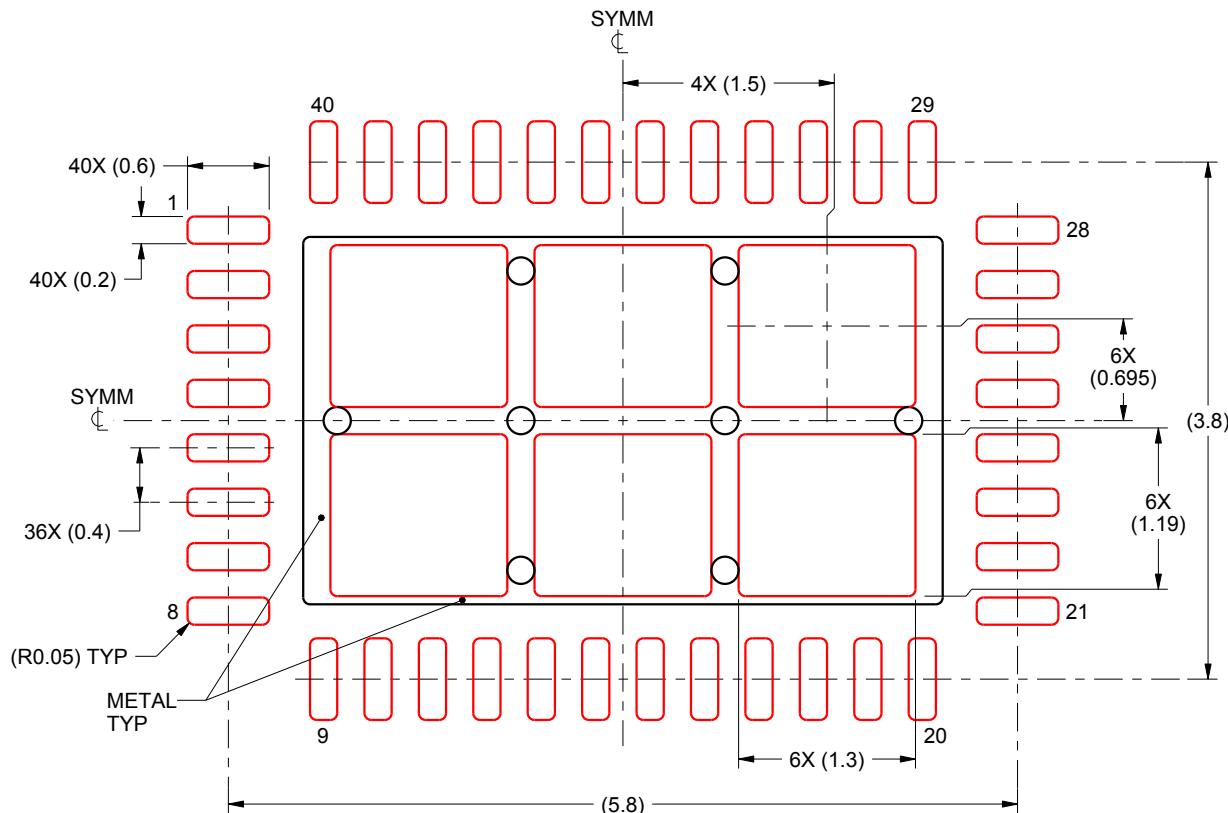
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number [SLU271](http://www.ti.com/lit/slu271) ([www.ti.com/lit/slu271](http://www.ti.com/lit/slu271))

## EXAMPLE STENCIL DESIGN

**RNQ0040A**

## **WQFN - 0.8 mm max height**

#### PLASTIC QUAD FLATPACK - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD  
73% PRINTED SOLDER COVERAGE BY AREA  
SCALE:18X

4222125/B 01/2016

#### NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.