TEXAS INSTRUMENTS

DRV10983, DRV10983Z

SLVSCP6E – JULY 2014 – REVISED MAY 2017

DRV10983 12- to 24-V, Three-Phase, Sensorless BLDC Motor Driver

1 Features

- Input Voltage Range: 8 to 28 V
- Total Driver H + L $r_{DS(on)}$: 250 mΩ
- Drive Current: 2-A Continuous (3-A Peak)
- Sensorless Proprietary Back Electromotive Force (BEMF) Control Scheme
- Continuous Sinusoidal 180° Commutation
- No External Sense Resistor Required
- For Flexibility User May Include External Sense Resistor to Monitor Power Delivered to Motor
- Flexible User Interface Options:
  - I^2C Interface: Access Registers for Command and Feedback
  - Dedicated SPEED Pin: Accepts Either Analog or PWM Input
  - Dedicated FG Pin: Provides TACH Feedback
  - Spin-Up Profile Customized With EEPROM
  - Forward-Reverse Control With DIR Pin
- Integrated Buck/Linear Converter to Efficiently Provide Voltage (5 V or 3.3 V) for Internal and External Circuits
- Supply Current 3 mA With Standby Version (DRV10983)
- Supply Current 180 μA With Sleep Version (DRV10983Z)
- Overcurrent Protection
- Lock Detection
- Voltage Surge Protection
- UVLO Protection
- Thermal Shutdown Protection
- Thermally-Enhanced 24-Pin HTSSOP

2 Applications

- Appliance Fan
- HVAC

3 Description

The DRV10983 is a three-phase sensorless motor driver with integrated power MOSFETs, which can provide continuous drive current up to 2 A. The device is specifically designed for cost-sensitive, low-noise, low-external-component-count applications.

The DRV10983 uses a proprietary sensorless control scheme to provide continuous sinusoidal drive, which significantly reduces the pure tone acoustics that typically occur as a result of commutation. The interface to the device is designed to be simple and flexible. The motor can be controlled directly through PWM, analog, or I^2C inputs. Motor speed feedback is available through either the FG pin or I^2C.

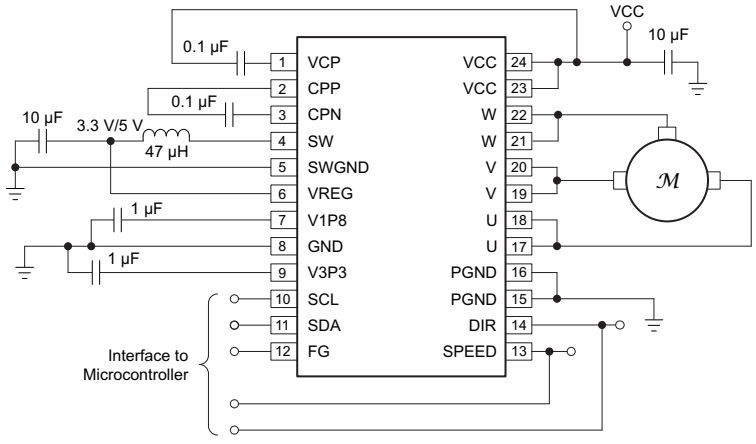
The DRV10983 features an integrated buck/linear regulator to efficiently step down the supply voltage to either 5 or 3.3 V for powering both internal and external circuits. The device is available in either a sleep mode or a standby mode version to conserve power when the motor is not running. The standby mode (3-mA) version leaves the regulator running and the sleep mode (180-μA) version shuts it off. Use the standby mode version in applications where the regulator is used to power an external microcontroller.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV10983	HTSSOP (24)	7.80 mm × 6.40 mm
DRV10983Z		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 2017) to Revision E — **Page**

- Changed pin numbering in the *Pin Functions* table ... 4

Changes from Revision C (May 2016) to Revision D — **Page**

- Added the DRV10983Z part number to the data sheet header and to the *Device Information* table ... 1
- Added DRV10983Z part number ... 6
- Corrected the link to the *DRV10983 and DRV10975 Tuning Guide* ... 15
- Added text to the *PWM Output* section ... 33
- Changed Figure 37 ... 35
- Changed "FGOLSet[1:0]" to "FGOLsel[1:0]" in *Register Map* address 0x2B ... 39
- Added recommended minimum dead tiime to SysOpt7 register ... 44
- Added *External Components* table ... 46
- Changed the link to the *DRV10983 and DRV10975 Tuning Guide* ... 46
- Changed the layout example ... 48

Changes from Revision B (February 2015) to Revision C — **Page**

- Added "phase to phase" clarification for overcurrent protection ... 8
- Added more accurate description to clarify overcurrent protection operation ... 12

Changes from Revision A (October 2014) to Revision B — **Page**

- Updated data sheet with the DRV10983Z sleep version ... 1

Changes from Original (July 2014) to Revision A **Page**

- Updated the input voltage range: 8 to 28 V ... 1
- Removed DRV10983Z sleep version part and updated standby mode supply current ... 1
- Updated pin information for SW, SWGND, VREG, SDA, FG, and VCC pins ... 4
- Added DIR, SW, and VREG pins to *Absolute Maximum Ratings* ... 9
- Updated max supply voltage and voltage range ratings for VCC and U, V, W in *Recommended Operating Conditions* ... 9
- Updated *Functional Block Diagram* ... 11
- Changed "hardware current limit" to "lock detection current limit" and "software current" to "acceleration current limit" throughout data sheet ... 12
- Updated max value for open to closed loop threshold ... 23
- Corrected description to "velocity constant of the motor" for Equation 1 ... 24
- Corrected register name in *Start-Up Current Setting* ... 24
- Updated Equation 2 ... 24
- Updated Figure 18 ... 24
- Updated caption name for Figure 22 ... 26
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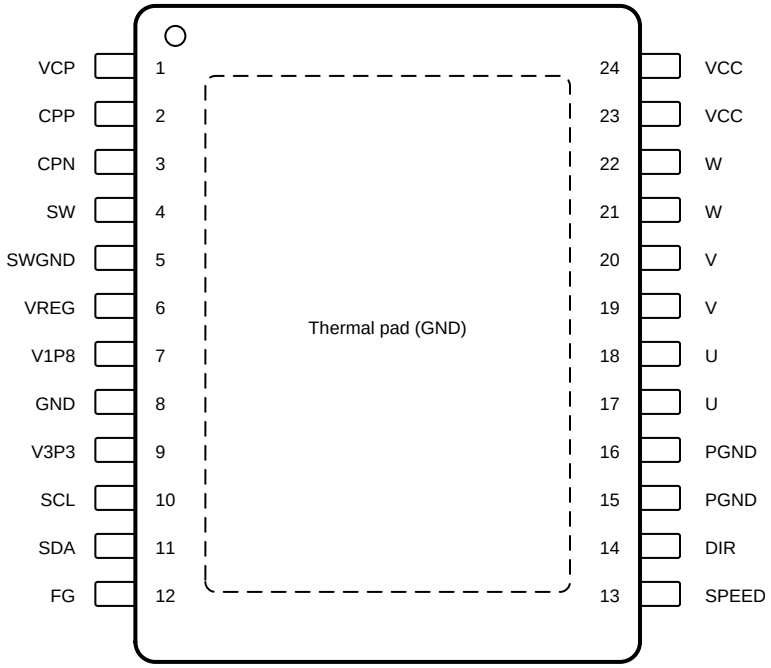
- Updated register description for status register. ... 39
- Updated the data in the examples for MotorSpeed1 and MotorPeriod1 ... 41
- Updated IPDPosition description in *Register Map* ... 41
- Increased max motor voltage for Recommended Application Range ... 45
- Updated graph callout for Figure 41 ... 46

5 Description (continued)

An I^2C interface allows the user to reprogram specific motor parameters in registers and program the EEPROM to help optimize the performance for a given application. The DRV10983 is available in a thermally efficient HTSSOP, 24-pin package with an exposed thermal pad. The operating temperature is specified from –40°C to +125°C.

6 Pin Configuration and Functions

PWP Package
24-Pin HTSSOP
Top View



Not to scale

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VCP	1	P	Charge pump output.
CPP	2	P	Charge pump pin 2, use a ceramic capacitor between CPN and CPP.
CPN	3	P	Charge pump pin 1, use a ceramic capacitor between CPN and CPP.
SW	4	O	Step-down regulator switching node output.
SWGND	5	P	Step-down regulator ground.
VREG	6	P	Step-down regulator output and feedback point.
V1P8	7	P	Internal 1.8-V digital core voltage. V1P8 capacitor must connect to GND. This is an output, but not specified to drive external loads.
GND	8	—	Digital and analog ground.
V3P3	9	P	Internal 3.3-V supply voltage. V3P3 capacitor must connect to GND. This is an output and may drive external loads not to exceed I_{V3P3_MAX}.
SCL	10	I	I^2C clock signal.
SDA	11	I/O	I^2C data signal.
FG	12	O	FG signal output.
SPEED	13	I	Speed control signal for PWM or analog input speed command.
DIR	14	I	Direction.

(1) I = input, O = output, I/O = input/output, P = power

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
PGND	15, 16	P	Power ground.
U	17, 18	O	Motor U phase
V	19, 20	O	Motor V phase
W	21, 22	O	Motor W phase
VCC	23, 24	P	Device power supply
Thermal pad (GND)	—	—	The exposed thermal pad must be electrically connected to ground plane through soldering to PCB for proper operation and connected to bottom side of PCB through vias for better thermal spreading.

7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage(2)	VCC	–0.3	30	V
	SPEED	–0.3	4	
	GND	–0.3	0.3	
	SCL, SDA	–0.3	4	
	DIR	–0.3	4	
Output voltage(2)	U, V, W	–1	30	V
	SW	–1	30	
	VREG	–0.3	7	
	FG	–0.3	4	
	VCP	–0.3	$V_{(VCC)}$ + 6	
	CPN	–0.3	30	
	CPP	–0.3	$V_{(VCC)}$ + 6	
	V3P3	–0.3	4	
	V1P8	–0.3	2.5	
T_{J_MAX}	Maximum junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	VCC	8	24	28	V
Voltage	U, V, W	–0.7		29	V
	SCL, SDA, FG, SPEED, DIR	–0.1	3.3	3.6	
	PGND, GND	–0.1		0.1	
Current	Step-down regulator output current (buck mode)			100	mA
	Step-down regulator output current (linear mode)			0	
	V3P3 LDO output current			5	
Operating junction temperature, T_J		–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		DRV10983, DRV10983Z PWP (HTSSOP) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT (DRV10983)						
I_{Vcc}	Supply current	T_A = 25°C; sleepDis = 1; SPEED = 0 V; $V_{(VCC)}$ = 24 V; buck regulator		3.5	5	mA
		T_A = 25°C; sleepDis = 1; SPEED = 0 V; $V_{(VCC)}$ = 24 V; linear regulator		11		
$I_{VccSTBY}$	Standby current	T_A = 25°C; SPEED = 0 V; $V_{(VCC)}$ = 24 V; standby mode device; buck regulator		3	4	mA
		T_A = 25°C; SPEED = 0 V; $V_{(VCC)}$ = 24 V; standby mode device; linear regulator		9		
SUPPLY CURRENT (DRV10983Z)						
I_{Vcc}	Supply current	T_A = 25°C; sleepDis = 1; SPEED = 0 V; $V_{(VCC)}$ = 24 V; buck regulator		3.5	5	mA
		T_A = 25°C; sleepDis = 1; SPEED = 0 V; $V_{(VCC)}$ = 24 V; linear regulator		11		
$I_{VccSLEEP}$	Sleep current	T_A = 25°C; SPEED = 0 V; $V_{(VCC)}$ = 24 V; sleep mode device; buck regulator		160	200	µA
UVLO						
V_{UVLO_R}	UVLO threshold voltage	Rise threshold, T_A = 25°C	7	7.4	8	V
V_{UVLO_F}	UVLO threshold voltage	Fall threshold, T_A = 25°C	6.7	7.1	7.5	V
V_{UVLO_HYS}	UVLO threshold voltage hysteresis	T_A = 25°C	200	300	400	mV
LDO OUTPUT						
V3P3		$V_{(VCC)}$ = 24 V, T_A = 25°C, VregSel = 0, 5-mA load	3	3.3	3.6	V
		$V_{(VCC)}$ = 24 V, T_A = 25°C, VregSel = 1, $V_{(VREG)}$ < 3.3 V, 5-mA load	$V_{(VREG)}$ – 0.3	$V_{(VREG)}$ – 0.1	$V_{(VREG)}$	
		$V_{(VCC)}$ = 24 V, T_A = 25°C, VregSel = 1, $V_{(VREG)}$ ≥ 3.3 V, 5-mA load	3	3.3	3.6	
I_{V3P3_MAX}	Maximum load from V3P3	$V_{(VCC)}$ = 24 V, T_A = 25°C		5		mA
V1P8		$V_{(VCC)}$ = 24 V, T_A = 25°C, VregSel = 0	1.6	1.78	2	V
		$V_{(VCC)}$ = 24 V, T_A = 25°C, VregSel = 1	1.6	1.78	2	
STEP-DOWN REGULATOR						
V_{REG}	Regulator output voltage	T_A = 25˚C; VregSel = 0, L_{SW} = 47 µH, C_{SW} = 10 µF, I_{load} = 50 mA	4.5	5	5.5	V
		T_A = 25˚C; VregSel = 1, L_{SW} = 47 µH, C_{SW} = 10 µF, I_{load} = 50 mA	3.06	3.4	3.6	
V_{REG_L}	Regulator output voltage (linear mode)	T_A = 25°C, VregSel = 0, R_{SW} = 39 Ω, C_{SW} = 10 µF		5		V
		T_A = 25°C, VregSel = 1, R_{SW} = 39 Ω, C_{SW} = 10 µF		3.4		
I_{REG_MAX}	Maximum load from V_{REG}	T_A = 25°C, L_{SW} = 47 µH, C_{SW} = 10 µF		100		mA
INTEGRATED MOSFET						
$r_{DS(on)}$	Series resistance (H + L)	T_A = 25˚C; $V_{(VCC)}$ = 24 V; $V_{(VCP)}$ = 29 V; Iout = 1 A		0.25	0.4	Ω
		T_A = 85˚C; $V_{(VCC)}$ = 24 V; $V_{(VCP)}$ = 29 V; Iout = 1 A		0.325		Ω
SPEED – ANALOG MODE						
V_{AN/A_FS}	Analog full speed voltage			$V_{(V3P3)}$ × 0.9		V
V_{AN/A_ZS}	Analog zero speed voltage			100		mV
t_{SAM}	Analog speed sample period			320		µs
V_{AN/A_RES}	Analog voltage resolution			5.8		mV
SPEED – PWM DIGITAL MODE						

Electrical Characteristics (continued)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DIG_IH}	PWM input high voltage		2.2			V
V_{DIG_IL}	PWM input low voltage				0.6	V
f_{PWM}	PWM input frequency		1		100	kHz
SLEEP OR STANDBY CONDITION						
$V_{EN\_SL\_SB}$	Analog voltage-to-enter sleep or standby	SpdCtrlMd = 0 (analog mode)	30			mV
V_{EX_SL}	Analog voltage-to-exit sleep	SpdCtrlMd = 0 (analog mode)	2.2	3.3		V
V_{EX_SB}	Analog voltage-to-exit standby	SpdCtrlMd = 0 (analog mode)		120		mV
t_{EX_SL}	Time-to-exit from sleep mode	SpdCtrlMd = 0 (analog mode) SPEED > V_{DIG_IH}		1		µs
t_{EX_SB}	Time-to-exit from standby mode	SpdCtrlMd = 0 (analog mode) SPEED > V_{EX_SB}		700		ms
$t_{EX\_SL\_SB}$	Time-to-exit from sleep or standby condition	SpdCtrlMd = 1 (PWM mode) SPEED > V_{DIG_IH}		1		µs
$t_{EN\_SL\_SB}$	Time-to-enter sleep or standby condition	SpdCtrlMd = 1 (PMW mode) SPEED < V_{DIG_IL}		5		ms
DIGITAL I/O (DIR INPUT AND FG OUTPUT)						
V_{DIR_H}	Input high		2.2			V
V_{DIR_L}	Input low				0.6	V
I_{FG_SINK}	Output sink current	Vout = 0.3 V	5			mA
I^2C SERIAL INTERFACE						
V_{I2C_H}	Input high		2.2			V
V_{I2C_L}	Input low				0.6	V
LOCK DETECTION RELEASE TIME						
t_{LOCK_OFF}	Lock release time			5		s
t_{LCK_ETR}	Lock enter time			0.3		s
OVERCURRENT PROTECTION						
I_{OC_limit}	Overcurrent protection	T_A = 25˚C; phase to phase	3	4		A
THERMAL SHUTDOWN						
T_{SDN}	Shutdown temperature threshold	Shutdown temperature		150		°C
T_{SDN_HYS}	Shutdown temperature threshold	Hysteresis		10		°C

7.6 Typical Characteristics

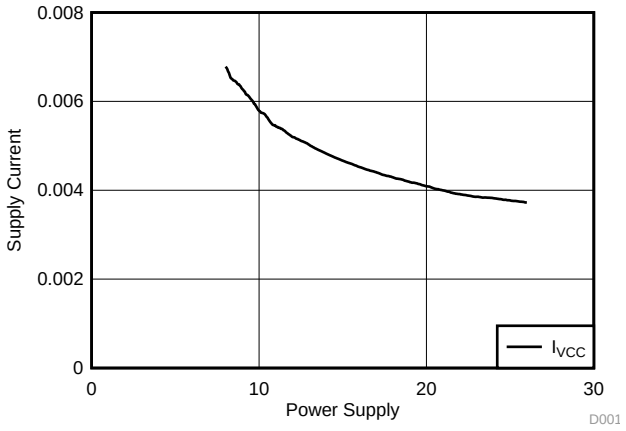


Figure 1. Supply Current vs Power Supply

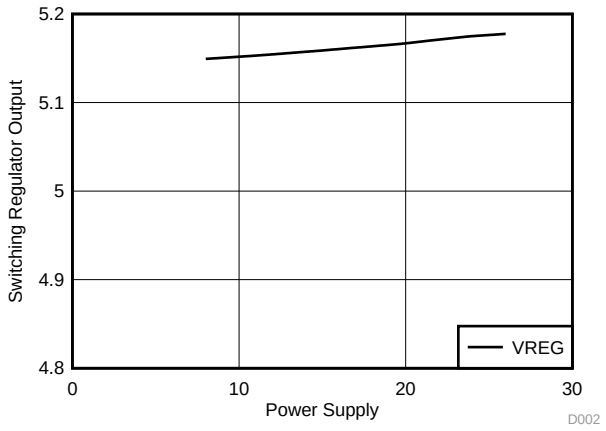


Figure 2. Switching Regulator Output vs Power Supply (VregSel = 0)

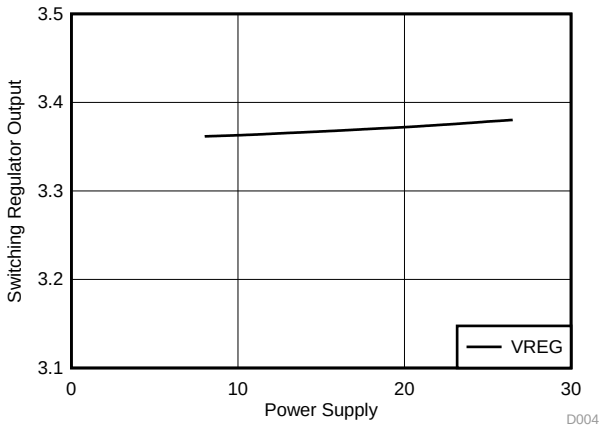


Figure 3. Switching Regulator Output vs Power Supply (VregSel = 1)

8 Detailed Description

8.1 Overview

The DRV10983 is a three-phase sensorless motor driver with integrated power MOSFETs, which provide drive current capability up to 2 A continuous. The device is specifically designed for low-noise, low external component count, 12- to 24-V motor drive applications. The device is configurable through a simple I^2C interface to accommodate different motor parameters and spin-up profiles for different customer applications.

A 180° sensorless control scheme provides continuous sinusoidal output voltages to the motor phases to enable ultra-quiet motor operation by keeping the electrically induced torque ripple small.

The DRV10983 features extensive protection and fault detect mechanisms to ensure reliable operation. Voltage surge protection prevents the input Vcc capacitor from overcharging, which is typical during motor deceleration. The devices provides phase to phase overcurrent protection without the need for an external current sense resistor. Rotor lock detect is available through several methods. These methods can be configured with register settings to ensure reliable operation. The device provides additional protection for undervoltage lockout (UVLO) and for thermal shutdown.

The commutation control algorithm continuously measures the motor phase current and periodically measures the VCC supply voltage. The device uses this information for BEMF estimation, and the information is also provided through the I^2C register interface for debug and diagnostic use in the system, if desired.

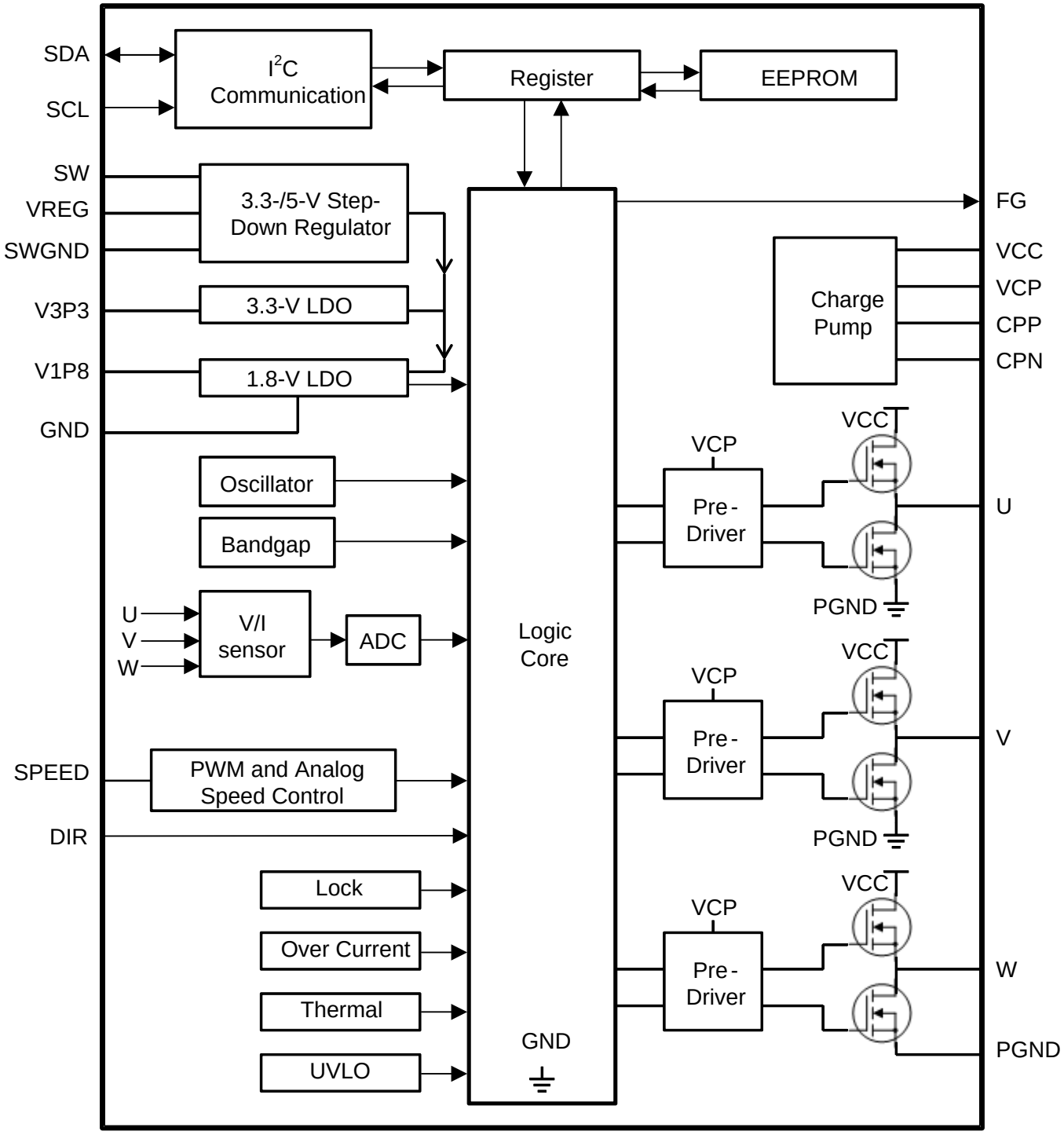
A buck switching regulator efficiently steps down the supply voltage. The output of this regulator provides power for the internal circuits and can also be used to provide power for an external circuit such as a microcontroller. If providing power for an external circuit is not necessary (and to reduce system cost), configure the buck switching regulator as a linear regulator by replacing the inductor with resistor.

TI designed the interfacing to the DRV10983 to be flexible. In addition to the I^2C interface, the system can use the discrete FG pin, DIR pin, and SPEED pin. SPEED is the speed command input pin. It controls the output voltage amplitude. DIR is the direction control input pin. FG is the speed indicator output, which shows the frequency of the motor commutation.

EEPROM is integrated in the DRV10983 as memory for the motor parameter and operation settings. EEPROM data transfers to the register after power on and exit from sleep mode.

The DRV10983 device can also operate in register mode. If the system includes a microcontroller communicating through the I^2C interface, the device can dynamically update the motor parameter and operation settings by writing to the registers. In this configuration, the EEPROM data is bypassed by the register settings.

8.2 Functional Block Diagram



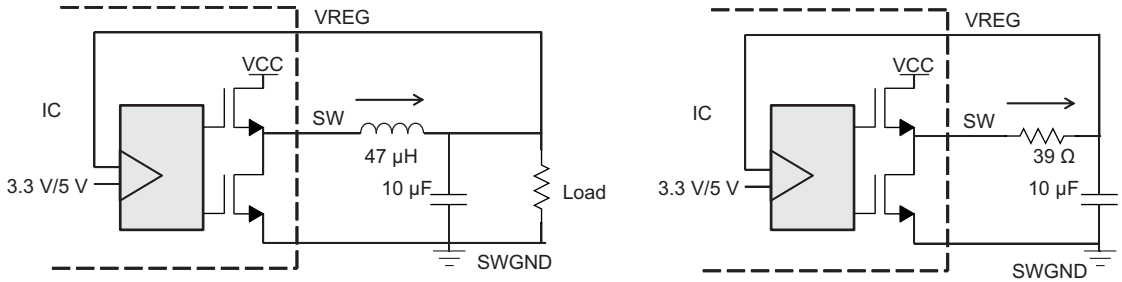
8.3 Feature Description

8.3.1 Regulators

8.3.1.1 Step-Down Regulator

The DRV10983 includes a step-down voltage regulator that can be operated as either a switching buck style regulator or as a linear regulator (see Figure 4). The regulator output voltage can be configured by register bit VregSel. When VregSel = 0, the regulator output voltage is 5 V, and when VregSel = 1, the regulator output voltage is 3.3 V.

If the step-down regulator is configured as buck style, see I_{REG_MAX} in the *Electrical Characteristics* to determine the amount of current provided for external load. If the step-down regulator is configured as linear mode, it is used for the device internal circuit only.



Buck Regulator Linear Regulator

Figure 4. Step-Down Regulator Configurations

8.3.1.2 3.3-V and 1.8-V LDO

The DRV10983 includes a 3.3-V LDO and an 1.8-V LDO. The 1.8-V LDO is for internal circuit only. The 3.3-V LDO is mainly for internal circuits, but can also drive external loads not to exceed I_{V3P3_MAX} listed in the *Electrical Characteristics*. For example, it can work as a pullup voltage for the FG, DIR, SDA, and SCL interface.

Both V1P8 and V3P3 capacitor must be connected to GND.

8.3.2 Protection Circuits

8.3.2.1 Thermal Shutdown

The DRV10983 has a built-in thermal shutdown function, which shuts down the device when junction temperature is more than T_{SDN} °C and recovers operating conditions when junction temperature falls to T_{SDN} – T_{SDN_HYS}°C.

The OverTemp status bit (address 0x10 bit 7) is set during thermal shutdown.

8.3.2.2 UVLO

The DRV10983 has a built-in UVLO function block. The hysteresis of UVLO threshold is $V_{UVLO-HYS}$. The device is locked out when VCC is down to V_{UVLO_F} and woke up at V_{UVLO_R}.

8.3.2.3 Current Protection

The overcurrent shutdown function acts to protect the device if the current, as measured from the FETs, exceeds the $I_{OC-limit}$ threshold. It protects the device from phase-to-phase short-circuit conditions; the DRV10983 places the output drivers into a high-impedance state and maintains this condition until the overcurrent is no longer present. The OverCurr status bit (address 0x10 bit 5) is set.

The DRV10983 also provides acceleration current limit and lock detection current limit functions to protect the device and motor (see *Current Limit* and *Lock Detect and Fault Handling*).

Feature Description (continued)

8.3.2.4 Lock

When the motor is blocked or stopped by an external force, the lock protection is triggered, and the device stops driving the motor immediately. After the lock release time t_{LOCK_OFF}, the DRV10983 resumes driving the motor again. If the lock condition is still present, it enters the next lock protection cycle until the lock condition is removed. With this lock protection, the motor and device does not get overheated or damaged due to the motor being locked (see *Lock Detect and Fault Handling*).

During lock condition, the MtrLck Status bit (address 0x10, bit 4) is set. To further diagnose, check the register FaultCode.

8.3.3 Motor Speed Control

The DRV10983 offers four methods for indirectly controlling the speed of the motor by adjusting the output voltage amplitude. This can be accomplished by varying the supply voltage (VCC) or by controlling the Speed Command. The Speed Command can be controlled in one of three ways. The user can set the Speed Command by adjusting either the PWM input (PWM) or the analog input (Analog) or by writing the Speed Command directly through the I^2C serial port (I^2C). The Speed Command is used to determine the PWM duty cycle output (PWM_DCO) (see Figure 5).

The Speed Command may not always be equal to the PWM_DCO because DRV10983 has implemented the AVS function (see *AVS Function*), the acceleration current limit function (see *Acceleration Current Limit*), and the closed loop accelerate function (see *Closed Loop Accelerate*) to optimize the control performance. These functions can limit the PWM_DCO, which affects the output amplitude.

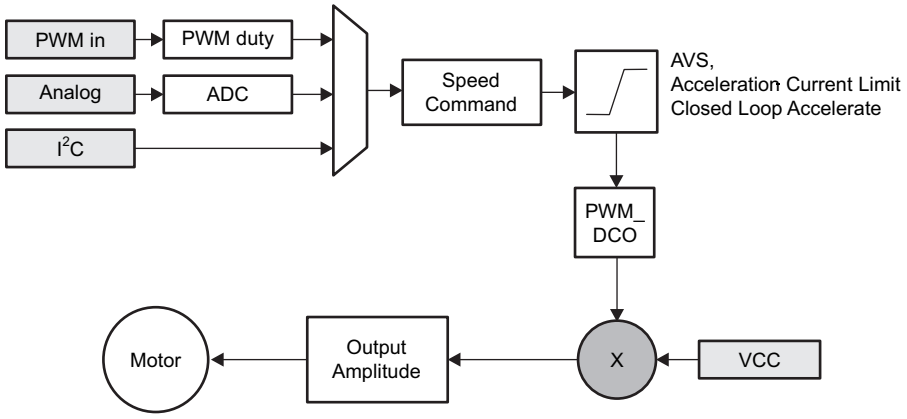


Figure 5. Multiplexing the Speed Command to the Output Amplitude Applied to the Motor

The output voltage amplitude applied to the motor is accomplished through sine wave modulation so that the phase-to-phase voltage is sinusoidal.

When any phase is measured with respect to ground, the waveform is sinusoidally coupled with third-order harmonics. This encoding technique permits one phase to be held at ground while the other two phases are pulse-width modulated. Figure 6 and Figure 7 show the sinusoidal encoding technique used in the DRV10983.

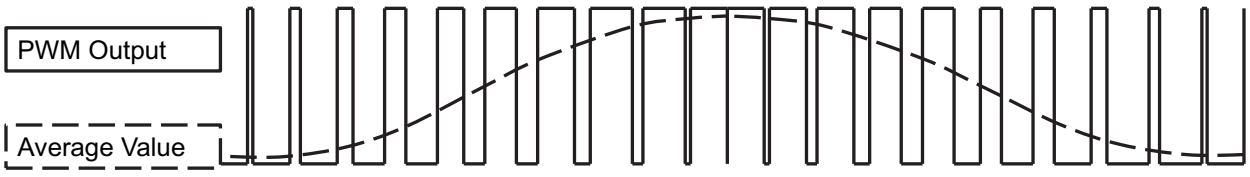
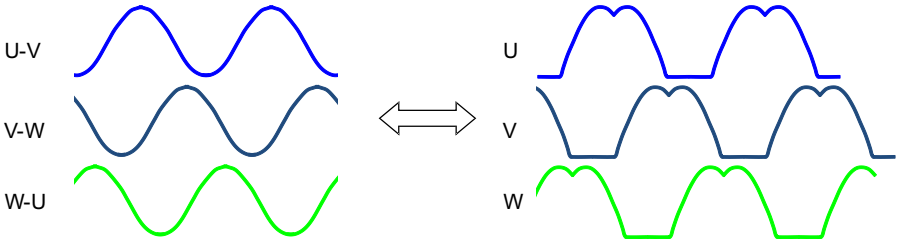


Figure 6. PWM Output and the Average Value

Feature Description (continued)



Sinusoidal voltage from phase to phase

Sinusoidal voltage with third order harmonics from phase to GND

Figure 7. Representing Sinusoidal Voltages With Third-Order Harmonic Output

The output amplitude is determined by the magnitude of VCC and the PWM duty cycle output (PWM_DCO). The PWM_DCO represents the peak duty cycle that is applied in one electrical cycle. The maximum amplitude is reached when PWM_DCO is at 100%. The peak output amplitude is VCC. When the PWM_DCO is at 50%, the peak amplitude is VCC / 2 (see Figure 8).

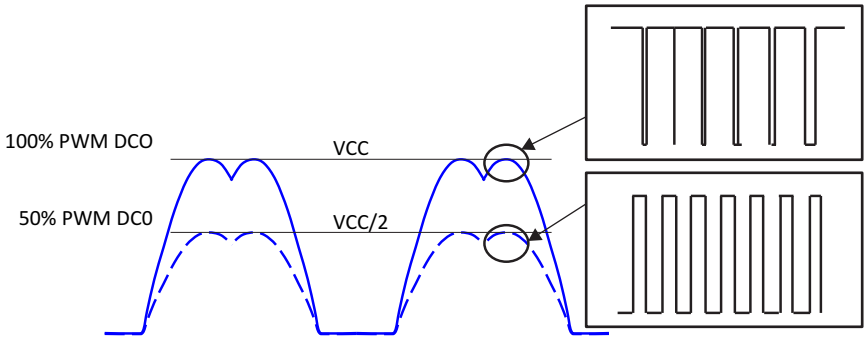


Figure 8. Output Voltage Amplitude Adjustment

8.3.4 Sleep or Standby Condition

The DRV10983 is available in either a sleep mode or standby mode version. The DRV10983 enters either sleep or standby to conserve energy. When the device enters either sleep or standby, the motor stops driving. The switching regulator is disabled in the sleep mode version to conserve more energy. The I^2C interface is disabled and any register data not stored in EEPROM will be reset. The switching regulator remains active in the standby mode version. The register data is maintained, and the I^2C interface remains active.

Setting sleepDis = 1 prevents the device from entering into the sleep or standby condition. If the device has already entered into sleep or standby condition, setting sleepDis = 1 will not take it out of the sleep or standby condition. During a sleep or standby condition, the Slp_Stdby status bit (address 0x10, bit 6) will be set.

For different speed command modes, Table 1 shows the timing and command to enter the sleep or standby condition.

Table 1. Conditions to Enter or Exit Sleep or Standby Condition

Speed Command Mode	Enter Sleep/Standby Condition	Exit from Standby Condition	Exit from Sleep Condition
Analog	SPEED pin voltage < $V_{EN\_SL\_SB}$ for $T_{EN\_SL\_SB}$	SPEED pin voltage > V_{EX_SB} for T_{EX_SB}	SPEED pin high (V > V_{DIG_IH}) for $T_{EX\_SL\_SB}$
PWM	SPEED pin low (V < V_{DIG_IL}) for $T_{EN\_SL\_SB}$	SPEED pin high (V > V_{DIG_IH}) for $T_{EX\_SL\_SB}$	SPEED pin high (V > V_{DIG_IH}) for $T_{EX\_SL\_SB}$

Feature Description (continued)

Table 1. Conditions to Enter or Exit Sleep or Standby Condition (continued)

Speed Command Mode	Enter Sleep/Standby Condition	Exit from Standby Condition	Exit from Sleep Condition
I^2C	SpdCtrl[8:0] is programmed as 0 for $T_{EN\_SL\_SB}$	SpdCtrl[8:0] is programmed as non-zero for $T_{EX\_SL\_SB}$	SPEED pin high (V > V_{DIG_IH}) for $T_{EX\_SL\_SB}$

Note that using the analog speed command, a higher voltage is required to exit from the sleep condition than the standby condition. The I^2C speed command cannot take the device out of the sleep condition because I^2C communication is disabled during the sleep condition.

8.3.5 Non-Volatile Memory

The DRV10983 has 96-bits of EEPROM data, which are used to program the motor parameters as described in the *I^2C Serial Interface*.

The procedure for programming the EEPROM is as follows. TI recommends to perform the EEPROM programming without the motor spinning, power cycle after the EEPROM write, and read back the EEPROM to verify the programming is successful.

1. Set SIdata = 1.
2. Write the desired motor parameters into the corresponding registers (address 0x20:0x2B) (see *I^2C Serial Interface*).
3. Write 1011 0110 (0xB6) to enProgKey in the DevCtrl register.
4. Ensure that VCC is at or above 22 V.
5. Write eeWrite = 1 in EECtrl register to start the EEPROM programming.

The programming time is about 24 ms, and eeWrite bit is reset to 0 when programming is done.

8.4 Device Functional Modes

This section includes the logic required to be able to reliably start and drive the motor. It describes the processes used in the logic core and provides the information needed to effectively configure the parameters to work over a wide range of applications.

8.4.1 Motor Parameters

For the motor parameter measurement, see the *DRV10983 and DRV10975 Tuning Guide*.

The motor resistance and motor velocity constant are two important parameters used to characterize a BLDC motor. The DRV10983 requires these parameters to be configured in the register. The motor resistance is programmed by writing the values for Rm[6:0] in the MotorParam1 register. The motor velocity constant is programmed by writing the values for Kt[6:0] in the MotorParam2 register.

8.4.1.1 Motor Resistance

The motor resistance (R_{PH_CT}) must be converted to a 7-bit digital register value Rm[6:0] to program the motor resistance value. The digital register value can be determined as follows:

1. Convert the motor resistance (R_{PH_CT}) to a digital value where the LSB is weighted to represent 9.67 mΩ: Rmdig = R_{PH_CT} / 0.00967.
2. Encode the digital value such that Rmdig = Rm[3:0] << Rm[6:4].

The maximum resistor value, R_{PH_CT}, that can be programmed for the DRV10983 is 18.5 Ω, which represents Rmdig = 1920 and an encoded Rm[6:0] value of 0x7Fh. The minimum resistor the DRV10983 supports is 0.029 Ω, R_{PH_CT}, which represents Rmdig = 3.

For convenience, the encoded value for Rm[6:0] can also be obtained from Table 2.

Device Functional Modes (continued)

Table 2. Motor Resistance Look-Up Table

R_{PH_CT} (Ω)	RM[6:0]	HEX	R_{PH_CT} (Ω)	RM[6:0]	HEX	R_{PH_CT} (Ω)	RM[6:0]	HEX
0.0000	0000000	00	0.348	0101001	29	3.09	1011010	5A
0.0097	0000001	01	0.387	0101010	2A	3.40	1011011	5B
0.0193	0000010	02	0.426	0101011	2B	3.71	1011100	5C
0.0290	0000011	03	0.464	0101100	2C	4.02	1011101	5D
0.0387	0000100	04	0.503	0101101	2D	4.33	1011110	5E
0.0484	0000101	05	0.542	0101110	2E	4.64	1011111	5F
0.0580	0000110	06	0.580	0101111	2F	4.95	1101000	68
0.0677	0000111	07	0.619	0111000	38	5.57	1101001	69
0.0774	001000	08	0.696	0111001	39	6.18	1101010	6A
0.0870	0001001	09	0.773	0111010	3A	6.80	1101011	6B
0.0967	0001010	0A	0.851	0111011	3B	7.42	1101100	6C
0.106	0001011	0B	0.928	0111100	3C	8.04	1101101	6D
0.116	0001100	0C	1.00	0111101	3D	8.66	1101110	6E
0.126	0001101	0D	1.08	0111110	3E	9.28	1101111	6F
0.135	0001110	0E	1.16	0111111	3F	9.90	1111000	78
0.145	0001111	0F	1.23	1001000	48	11.1	1111001	79
0.155	0011000	18	1.39	1001001	49	12.3	1111010	7A
0.174	0011001	19	1.54	1001010	4A	13.6	1111011	7B
0.193	0011010	1A	1.70	1001011	4B	14.8	1111100	7C
0.213	0011011	1B	1.85	1001100	4C	16.0	1111101	7D
0.232	0011100	1C	2.01	1001101	4D	17.3	1111110	7E
0.251	0011101	1D	2.16	1001110	4E	18.5	1111111	7F
0.271	0011110	1E	2.32	1001111	4F			
0.290	0011111	1F	2.47	1011000	58			
0.309	0101000	28	2.78	1011001	59			

8.4.1.2 Motor Velocity Constant

The motor velocity constant, Kt[6:0] describes the motors phase-to-phase BEMF voltage as a function of the motor velocity.

The measured motor velocity constant (Kt_{PH}) needs to be converted to a 7-bit digital register value Kt[6:0] to program the motor velocity constant value. The digital register value can be determined as follows:

1. Convert the measured Kt_{PH} to a weighted digital value: $Kt_{ph\_dig} = 1090 \times Kt_{PH}$
2. Encode the digital value such that Kt_{ph_dig} = Kt[3:0] << Kt[4:6].

The maximum Kt_{PH} that can be programmed is 1760 mV/Hz. This represents a digital value of 1920 and an encoded Kt[6:0] value of 0x7Fh. The minimum Kt_{PH} that can be programmed is 0.92 mV/Hz, which represents a digital value of 1 and an encoded Kt[6:0] value of 0x01h.

For convenience, the encoded value of Kt[6:0] may also be obtained from Table 3.

Table 3. Motor Velocity Constant Look-Up Table

Kt_{PH} (mV/Hz)	Kt[6:0]	HEX	Kt_{PH} (mV/Hz)	Kt [6:0]	HEX	Kt_{PH} (mV/Hz)	Kt [6:0]	HEX
0.00	0000000	00	33.0	0101001	29	293	1011010	5A
0.92	0000001	01	36.6	0101010	2A	322	1011011	5B
1.83	0000010	02	40.3	0101011	2B	352	1011100	5C
2.75	0000011	03	44.0	0101100	2C	381	1011101	5D
3.66	0000100	04	47.7	0101101	2D	411	1011110	5E
4.58	0000101	05	51.3	0101110	2E	440	1011111	5F

Table 3. Motor Velocity Constant Look-Up Table (continued)

Kt_{PH} (mV/Hz)	Kt[6:0]	HEX	Kt_{PH} (mV/Hz)	Kt [6:0]	HEX	Kt_{PH} (mV/Hz)	Kt [6:0]	HEX
5.5	0000110	06	55.0	0101111	2F	469	1101000	68
6.42	0000111	07	58.7	0111000	38	528	1101001	69
7.33	001000	08	66.0	0111001	39	587	1101010	6A
8.25	0001001	09	73.3	0111010	3A	645	1101011	6B
9.17	0001010	0A	80.7	0111011	3B	704	1101100	6C
10.0	0001011	0B	88.0	0111100	3C	763	1101101	6D
11.0	0001100	0C	95.4	0111101	3D	822	1101110	6E
11.9	0001101	0D	102	0111110	3E	880	1101111	6F
12.8	0001110	0E	110	0111111	3F	939	1111000	78
13.7	0001111	0F	117	1001000	48	1050	1111001	79
14.6	0011000	18	132	1001001	49	1170	1111010	7A
16.5	0011001	19	146	1001010	4A	1290	1111011	7B
18.3	0011010	1A	161	1001011	4B	1400	1111100	7C
20.1	0011011	1B	176	1001100	4C	1520	1111101	7D
22.0	0011100	1C	190	1001101	4D	1640	1111110	7E
23.8	0011101	1D	205	1001110	4E	1760	1111111	7F
25.6	0011110	1E	220	1001111	4F			
27.5	0011111	1F	234	1011000	58			
29.3	0101000	28	264	1011001	59			

8.4.2 Starting the Motor Under Different Initial Conditions

The motor can be in one of three states when the DRV10983 attempts to begin the start-up process. The motor may be stationary, or spinning in the forward or reverse directions. The DRV10983 includes a number of features to allow for reliable motor start under all of these conditions. Figure 9 shows the motor start-up flow for each of the three initial motor states.

8.4.2.1 Case 1 – Motor Is Stationary

If the motor is stationary, the commutation logic must be initialized to be in phase with the position of the motor. The DRV10983 provides for two options to initialize the commutation logic to the motor position. Initial position detect (IPD) determines the position of the motor based on the deterministic inductance variation, which is often present in BLDC motors. The Align and Go technique forces the motor into alignment by applying a voltage across a particular motor phase to force the motor to rotate in alignment with this phase. The following sections explain how to configure these techniques for use in the designer's system.

8.4.2.2 Case 2 – Motor Is Spinning in the Forward Direction

If the motor is spinning forward with enough velocity, the DRV10983 may be configured to go directly into closed loop. By resynchronizing to the spinning motor, the user achieves the fastest possible start-up time for this initial condition.

8.4.2.3 Case 3 – Motor Is Spinning in the Reverse Direction

If the motor is spinning in the reverse direction, the DRV10983 provides several methods to convert it back to forward direction.

One method, reverse drive, allows the motor to be driven so that it accelerates through zero velocity. The motor achieves the shortest possible spin-up time in systems where the motor is spinning in the reverse direction.

If this feature is not selected, then the DRV10983 may be configured to either wait for the motor to stop spinning or brake the motor. After the motor has stopped spinning, the motor start-up sequence proceeds as it would for a motor which is stationary.

Take care when using the feature reverse drive or brake to ensure that the current is limited to an acceptable level and that the supply voltage does not surge as a result of energy being returned to the power supply.

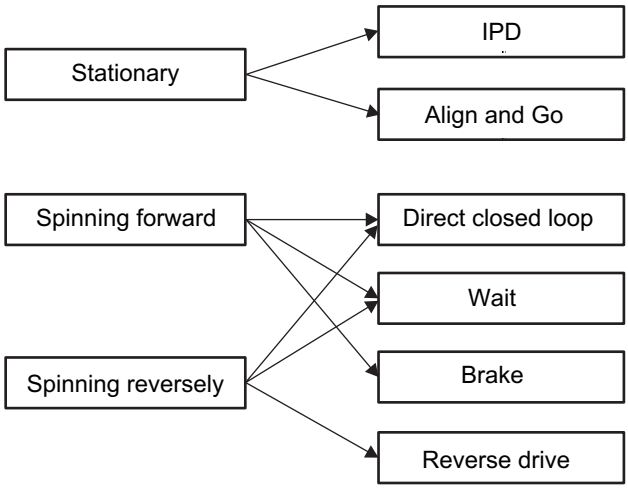


Figure 9. Start the Motor Under Different Initial Conditions

8.4.3 Motor Start Sequence

Figure 10 shows the motor start sequence implemented in the DRV10983.

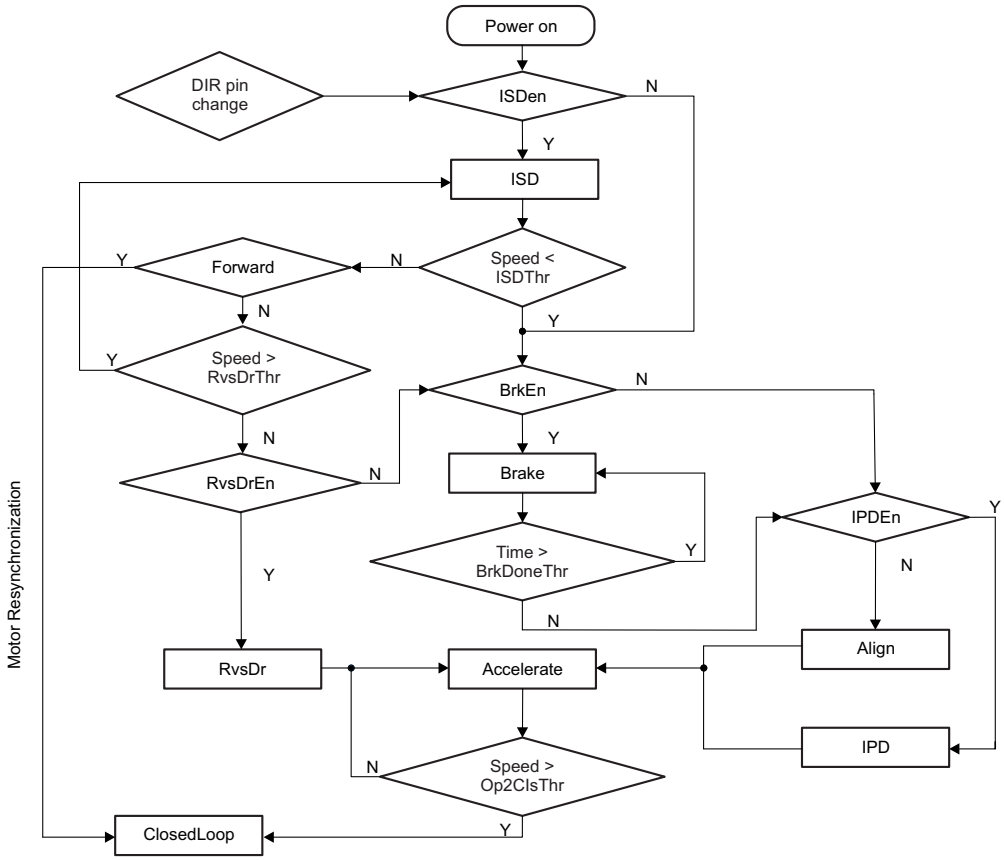


Figure 10. Motor Starting-Up Flow

Power-On State This is the initial power-on state of the motor start sequencer (MSS). The MSS starts in this state on initial power-up or whenever the DRV10983 comes out of either standby or sleep modes.

ISDen Judgment After power on, the DRV10983 MSS enters the ISDen Judgment where it checks to see if the Initial Speed Detect (ISD) function is enabled (ISDen = 1). If ISD is disabled, the MSS proceeds

directly to the BrkEn Judgment. If ISD is enabled, the motor start sequence advances to the ISD state.

ISD State The MSS determines the initial condition of the motor (see *ISD*).

Speed<ISDThr Judgment If the motor speed is lower than the threshold defined by ISDThr[1:0], then the motor is considered to be stationary and the MSS proceeds to the BrkEn judgment. If the speed is greater than the threshold defined by ISDThr[1:0], the start sequence proceeds to the Forward judgment.

Forward Judgment The MSS determines whether the motor is spinning in the forward or the reverse direction. If the motor is spinning in the forward direction, the DRV10983 executes the resynchronization (see *Motor Resynchronization*) process by transitioning directly into the ClosedLoop state. If the motor is spinning in the reverse direction, the MSS proceeds to the Speed>RvsDrThr.

Speed>RvsDrThr Judgment The motor start sequencer checks to see if the reverse speed is greater than the threshold defined by RvsDrThr[2:0]. If it is, then the MSS returns to the ISD state to allow the motor to decelerate. This prevents the DRV10983 from attempting to reverse drive or brake a motor that is spinning too quickly. If the reverse speed of the motor is less than the threshold defined by RvsDrThr[2:0], then the MSS advances to the RvsDrEn judgment.

RvsDrEn Judgment The MSS checks to see if the reverse drive function is enabled (RvsDrEn = 1). If it is, the MSS transitions into the RvsDr state. If the reverse drive function is not enabled, the MSS advances to the BrkEn judgment.

RvsDr State The DRV10983 drives the motor in the forward direction to force it to rapidly decelerate (see *Reverse Drive*). When it reaches zero velocity, the MSS transitions to the Accelerate state.

BrkEn Judgment The MSS checks to determine whether the brake function is enabled (BrkDoneThr[2:0] ≠ 000). If the brake function is enabled, the MSS advances to the Brake state.

Brake State The device performs the brake function (see *Motor Brake*).

Time>BrkDoneThr Judgment The MSS applies brake for time configured by BRKDontThr[2:0]. After brake state, the MSS advances to the IPDEn judgment.

IPDEn Judgment The MSS checks to see if IPD has been enabled (IPDCurrThr[3:0] ≠ 0000). If the IPD is enabled, the MSS transitions to the IPD state. Otherwise, it transitions to the align state.

Align State The DRV10983 performs align function (see *Align*). After the align completes, the MSS transitions to the Accelerate state.

IPD State The DRV10983 performs the IPD function. The IPD function is described in *IPD* . After the IPD completes, the MSS transitions to the Accelerate state.

Accelerate State The DRV10983 accelerates the motor according to the setting StAccel and StAccel2. After applying the accelerate settings, the MSS advances to the Speed > Op2ClsThr judgment.

Speed>Op2ClsThr Judgment The motor accelerates until the drive rate exceeds the threshold configured by the Op2ClsThr[4:0] settings. When this threshold is reached, the DRV10983 enters into the ClosedLoop state.

ClosedLoop State In this state, the DRV10983 drives the motor based on feedback from the commutation control algorithm.

DIR Pin Change Judgment If DIR pin get changed during any of above states, DRV10983 stops driving the motor and restarts from the beginning.

8.4.3.1 ISD

The ISD function is used to identify the initial condition of the motor. If the function is disabled, the DRV10983 does not perform the initial speed detect function and treats the motor as if it is stationary.

Phase-to-phase comparators are used to detect the zero crossings of the BEMF voltage of the motor while it is coasting (motor phase outputs are in high-impedance state). Figure 11 shows the configuration of the comparators.

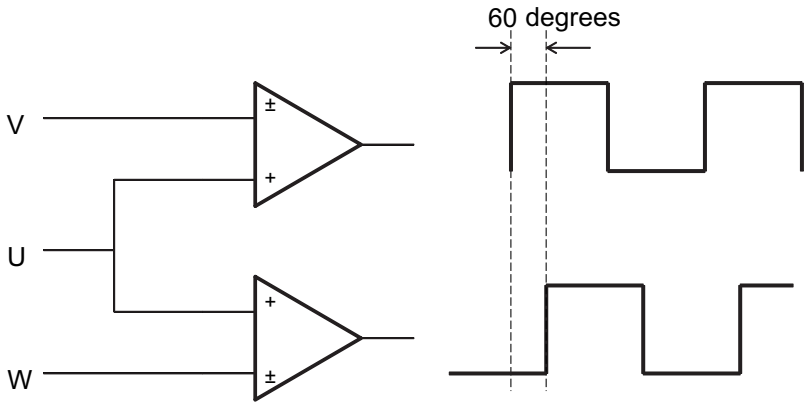


Figure 11. Initial Speed Detect Function

If the UW comparator output is lagging the UV comparator by 60°, the motor is spinning forward. If the UW comparator output is leading the UV comparator by 60°, the motor is spinning in reverse.

The motor speed is determined by measuring the time between two rising edges of either of the comparators.

If neither of the comparator outputs toggle for a given amount of time, the condition is defined as stationary. The amount of time can be programmed by setting the register bits ISDThr[1:0].

8.4.3.2 Motor Resynchronization

The resynchronize function works when the ISD function is enabled and determines that the initial state of the motor is spinning in the forward direction. The speed and position information measured during ISD are used to initialize the drive state of the DRV10983, which can transition directly into the closed loop running state without needing to stop the motor.

8.4.3.3 Reverse Drive

The ISD function measures the initial speed and the initial position; the DRV10983 reverse drive function acts to reverse accelerate the motor through zero speed and to continue accelerating until the closed loop threshold is reached (see Figure 12). If the reverse speed is greater than the threshold configured in RvsDrThr[1:0], then the DRV10983 waits until the motor coasts to a speed that is less than the threshold before driving the motor to reverse accelerate.

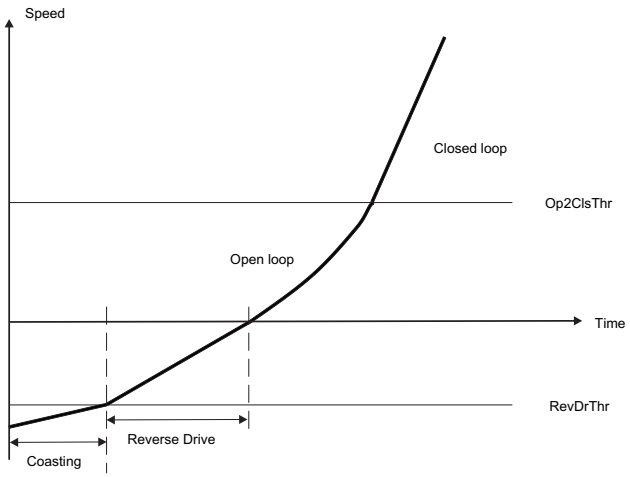


Figure 12. Reverse Drive Function

Reverse drive is suitable for applications where the load condition is light at low speed and relatively constant and where the reverse speed is low (that is, a fan motor with little friction). For other load conditions, the motor brake function provides a method for helping force a motor which is spinning in the reverse direction to stop spinning before a normal start-up sequence.

8.4.3.4 Motor Brake

The motor brake function can be used to stop the spinning motor before attempting to start the motor. The brake is applied by turning on all three of the low-side driver FETs.

Brake is enabled by configuring non zero value for BrkDoneThr[2:0]. Braking is applied for time configured by BrkDoneThr[2:0] (reverse or forward). After the motor is stopped, the motor position is unknown. To proceed with restarting in the correct direction, the IPD or Align and Go algorithm needs to be implemented. The motor start sequence is the same as it would be for a motor starting in the stationary condition.

The motor brake function can be disabled. The motor skips the brake state and attempts to spin the motor as if it were stationary. If this happens while the motor is spinning in either direction, the start-up sequence may not be successful.

8.4.3.5 Motor Initialization

8.4.3.5.1 Align

The DRV10983 aligns a motor by injecting dc current through a particular phase pattern which is current flowing into phase V, flowing out from phase W for a certain time (configured by AlignTime[2:0]). The current magnitude is determined by OpenLCurr[1:0]. The motor should be aligned at the known position.

The time of align affects the start-up timing (see *Start-Up Timing*). A bigger inertial motor requires longer align time.

8.4.3.5.2 IPD

The inductive sense method is used to determine the initial position of the motor when IPD is enabled. IPD is enabled by selecting IPDCurrThr[3:0] to any value other than 0000.

IPD can be used in applications where reverse rotation of the motor is unacceptable. Because IPD does not need to wait for the motor to align with the commutation, it can allow for a faster motor start sequence. IPD works well when the inductance of the motor varies as a function of position. Because it works by pulsing current to the motor, it can generate acoustics which must be taken into account when determining the best start method for a particular application.

8.4.3.5.2.1 IPD Operation

The IPD operates by sequentially applying voltage across two of the three motor phases according to the following sequence: VW WV UV VU WU UW (see Figure 13). When the current reaches the threshold configured in IPDCurrThr[3:0], the voltage across the motor is stopped. The DRV10983 measures the time it takes from when the voltage is applied until the current threshold is reached. The time varies as a function of the inductance in the motor windings. The state with the shortest time represents the state with the minimum inductance. The minimum inductance is because of the alignment of the north pole of the motor with this particular driving state.

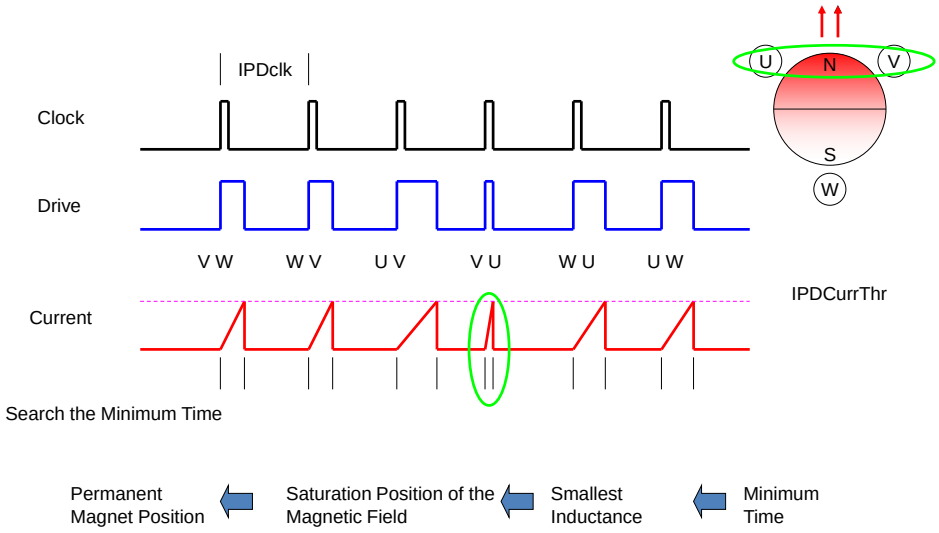


Figure 13. IPD Function

8.4.3.5.2.2 IPD Release Mode

Two options are available for stopping the voltage applied to the motor when the current threshold is reached. If IPDRlsMd = 0, the recirculate mode is selected. The low-side (S6) MOSFET remains on to allow the current to recirculate between the MOSFET (S6) and body diode (S2) (see Figure 14). If IPDRlsMd = 1, the tri-state mode is selected. Both the high-side (S1) and low-side (S6) MOSFETs are turned off and the current flies back across the body diodes into the power supply (see Figure 15).

The tri-state mode has a faster settle-down time, but could result in a surge on VCC. Manage this with appropriate selection of either a clamp circuit or by providing sufficient capacitance between VCC and GND. If the voltage surge cannot be contained and if it is unacceptable for the application, then select the recirculate mode. When selecting the recirculate mode, select the IPDClk[1:0] bits to give the current in the motor windings enough time to decay to 0.

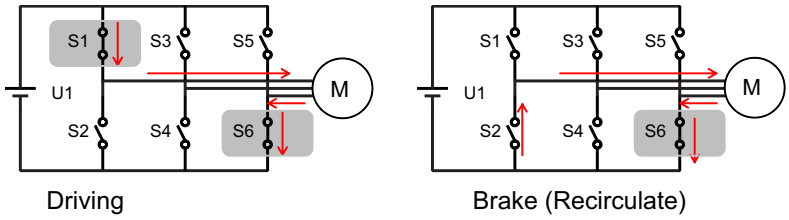


Figure 14. IPD Release Mode 0

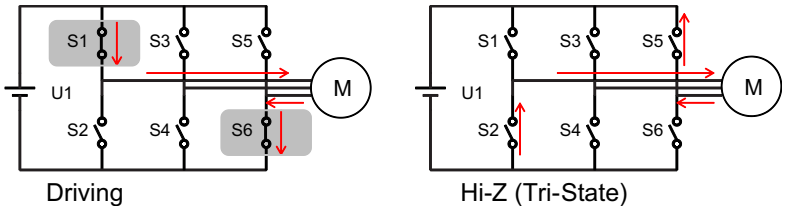


Figure 15. IPD Release Mode 1

8.4.3.5.2.3 IPD Advance Angle

After the initial position is detected, the DRV10983 begins driving the motor at an angle specified by IPDAdvcAgl[1:0].

Advancing the drive angle anywhere from 0° to 180° results in positive torque. Advancing the drive angle by 90° results in maximum initial torque. Applying maximum initial torque could result in uneven acceleration to the rotor. Select the IPDAdvcAgl[1:0] to allow for smooth acceleration in the application (see Figure 16).

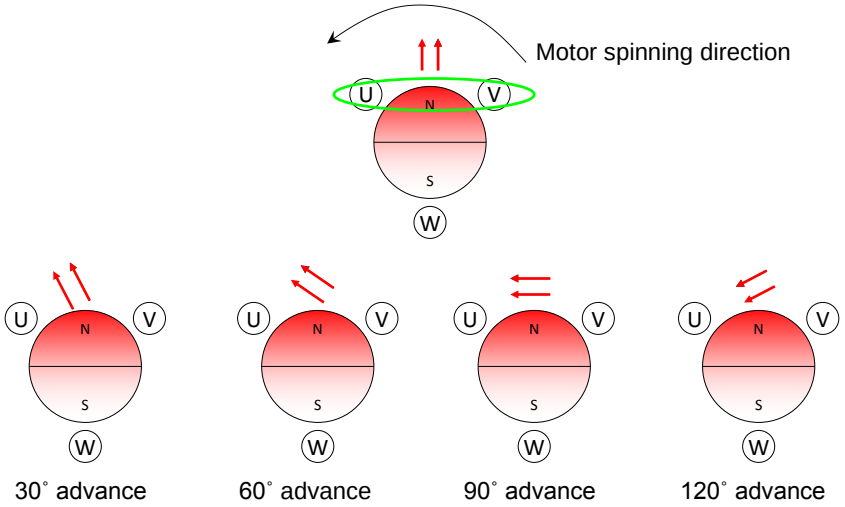


Figure 16. IPD Advance Angle

8.4.3.5.3 Motor Start

After it is determined that the motor is stationary and after completing the motor initialization with either align or IPD, the DRV10983 begins to accelerate the motor. This acceleration is accomplished by applying a voltage determined by the open loop current setting (OpenLCurr[1:0]) to the appropriate drive state and by increasing the rate of commutation without regard to the real position of the motor (referred to as open loop operation). The function of the open loop operation is to drive the motor to a minimum speed so that the motor generates sufficient BEMF to allow the commutation control logic to accurately drive the motor.

Table 4 lists the configuration options that can be set in register to optimize the initial motor acceleration stage for different applications.

Table 4. Configuration Options for Controlling Open Loop Motor Start

Description	Reg Name	ConfigBits	Min Value	Max Value
Open to closed loop threshold	SysOpt4	Op2ClsThr[4:0]	0.8 Hz	204.8 Hz
Align time	SysOpt4	AlignTime[2:0]	40 ms	5.3 s
First order accelerate	SysOpt3	StAccel[2:0]	0.3 Hz/s	76 Hz/s
Second order accelerate	SysOpt3	StAccel2[2:0]	0.22 Hz/s2	57 Hz/s2
Open loop current setting	SysOpt2	OpenLCurr[1:0]	200 mA	1.6 A
Open loop current ramping	SysOpt2	OpLCurrRt[2:0]	0.23 VCC/s	6 VCC/s

8.4.3.6 Start-Up Timing

Start-up timing is determined by the align and accelerate time. The align time can be set by AlignTime[2:0], as described in *Register Definition* . The accelerate time is defined by the open-to-closed loop threshold Op2ClsThr[4:0] along with the first order StAccel[2:0](A1) and second order StAccel2[2:0](A2) accelerate rates. Figure 17 shows the motor start-up process.

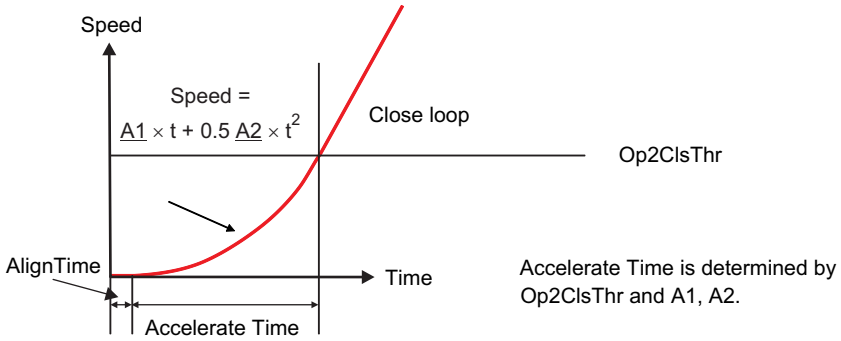


Figure 17. Motor Start-Up Process

Select the first order and second order accelerate rates to allow the motor to reliably accelerate from zero velocity up to the closed loop threshold in the shortest time possible. Using a slow accelerate rate during the first order accelerate stage can help improve reliability in applications where it is difficult to accurately initialize the motor with either align or IPD.

Select the open-to-closed loop threshold to allow the motor to accelerate to a speed that generates sufficient BEMF for closed loop control. This is determined by the velocity constant of the motor based on the relationship described in Equation 1.

$$BEMF = Kt_{PH} \times speed\ (Hz) \quad (1)$$

8.4.4 Start-Up Current Setting

The start-up current setting is to control the peak start-up during open loop. During open loop operation, it is desirable to control the magnitude of drive current applied to the motor. This is helpful in controlling and optimizing the rate of acceleration. The limit takes effect during reverse drive, align, and acceleration.

The start current is set by programming the OpenLCurr[1:0] bits. The current should be selected to allow the motor to reliably accelerate to the handoff threshold. Heavier loads may require a higher current setting, but it should be noted that the rate of acceleration will be limited by the acceleration rate (StAccel[2:0], StAccel2[2:0]). If the motor is started with more current than necessary to reliably reach the handoff threshold, it results in higher power consumption.

The start current is controlled based on the relationship shown in Equation 2 and Figure 18. The duty cycle applied to the motor is derived from the calculated value for U_{Limit} and the magnitude of the supply voltage, Vcc, as well as the drive state of the motor.

$$U_{Limit} = I_{Limit} \times Rm + Speed\,(Hz) \times Kt \quad (2)$$

where

- I_{Limit} is configured by OpenLCurr[1:0]
- Rm is configured by Rm[6:0]
- Speed is variable based open-loop acceleration profile of the motor
- Kt is configured by Kt[6:0]

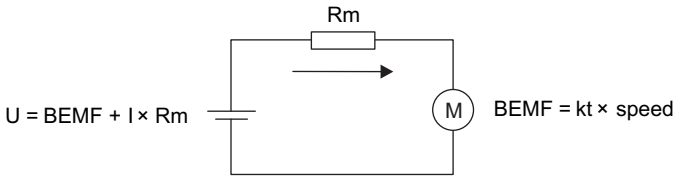


Figure 18. Motor Start-Up Current

8.4.4.1 Start-Up Current Ramp-Up

A fast change in the applied drive current may result in a sudden change in the driving torque. In some applications, this could result in acoustic noise. To avoid this, the DRV10983 allows the option of limiting the rate at which the current is applied to the motor. OpLCurrRt[2:0] sets the maximum voltage ramp up rate that will be applied to the motor. The waveforms in Figure 19 show how this feature can be used to gradually ramp the current applied to the motor.

Start driving with fast current ramp

Start driving with slow current ramp

Figure 19. Motor Startup Current Ramp

8.4.5 Closed Loop

In closed loop operation, the DRV10983 continuously samples the current in the U phase of the motor and uses this information to estimate the BEMF voltage that is present. The drive state of the motor is controlled based on the estimated BEMF voltage.

8.4.5.1 Half Cycle Control and Full Cycle Control

The estimated BEMF used to control the drive state of the motor has two zero-crosses every electrical cycle. The DRV10983 can be configured to update the drive state either once every electrical cycle or twice for every electrical cycle. When AdjMode is programmed to 1, half cycle adjustment is applied. The control logic is triggered at both rising edge and falling edge. When AdjMode is programmed to 0, full cycle adjustment is applied. The control logic is triggered only at the rising edge (see Figure 20).

Half cycle adjustment provides a faster response when compared with full cycle adjustment. Use half cycle adjustment whenever the application requires operation over large dynamic loading conditions. Use the full cycle adjustment for low current (<1 A) applications because it offers more tolerance for current measurement offset errors.

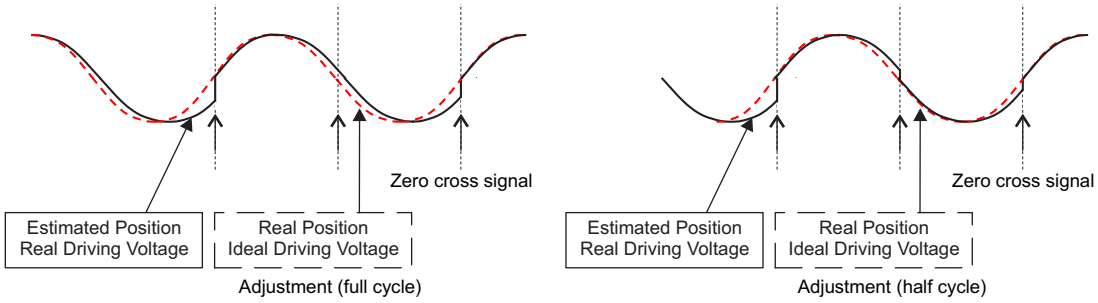


Figure 20. Closed Loop Control Commutation Adjustment Mode

8.4.5.2 Analog Mode Speed Control

The SPEED input pin can be configured to operate as an analog input (SpdCtrlMd = 0).

When configured for analog mode, the voltage range on the SPEED pin can be varied from 0 to V3P3. If SPEED > V_{ANA_FS}, the speed command is maximum. If V_{ANA_ZS} ≤ SPEED < V_{ANA_FS} the speed command changes linearly according to the magnitude of the voltage applied at the SPEED pin. If SPEED < V_{ANA_ZS} the speed command is to stop the motor. Figure 21 shows the speed command when operating in analog mode.

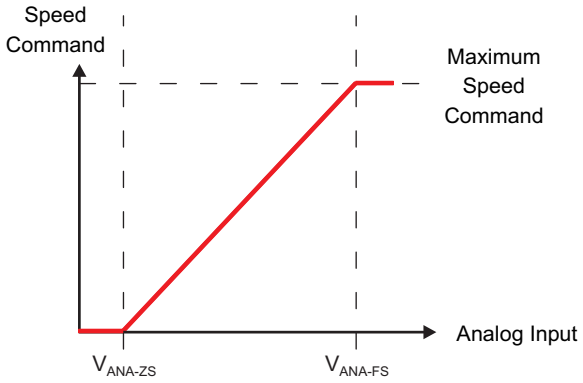


Figure 21. Analog Mode Speed Command

8.4.5.3 Digital PWM Input Mode Speed Control

If SpdCtrlMd = 1, the SPEED input pin is configured to operate as a PWM-encoded digital input. The PWM duty cycle applied to the SPEED pin can be varied from 0 to 100%. The speed command is proportional to the PWM input duty cycle. The speed command will be stopping the motor when the PWM input keeps at 0 for $t_{EN\_SL\_SB}$ (see Figure 22).

The frequency of the PWM input signal applied to the SPEED pin is defined as f_{PWM}. This is the frequency the device can accept to control motor speed. It does not correspond to the PWM output frequency that is applied to the motor phase. The PWM output frequency can be configured to be either 25 kHz when the DoubleFreq bit is set to 0 or to 50 kHz when DoubleFreq bit is set to 1.

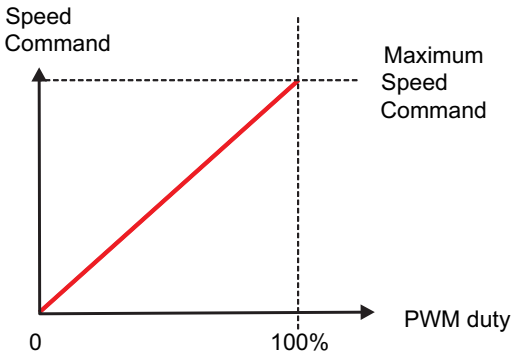


Figure 22. PWM Mode Speed Command

8.4.5.4 I^2C Mode Speed Control

The DRV10983 can also command the speed through the I^2C serial interface. To enable this feature, the OverRide bit is set to 1. When the DRV10983 is configured to operate in I^2C mode, it ignores the signal applied to the SPEED pin.

The speed command can be set by writing the SpdCtrl[8] and SpdCtrl[7:0] bits. The 9-bit SpdCtrl [8:0] located in the SpeedCtrl1 and SpeedCntrl2 registers are used to set the peak amplitude voltage applied to the motor. The maximum speed command is set when SpdCtrl [8:0] is set to 0x1FF (511).

When SpdCtrl [8] is written to the SpeedCtrl2 register, the data is stored, but the output is not changed. When SpdCtrl [7:0] is written to the SpeedCtrl1 register, the speed command is updated (see Figure 23).

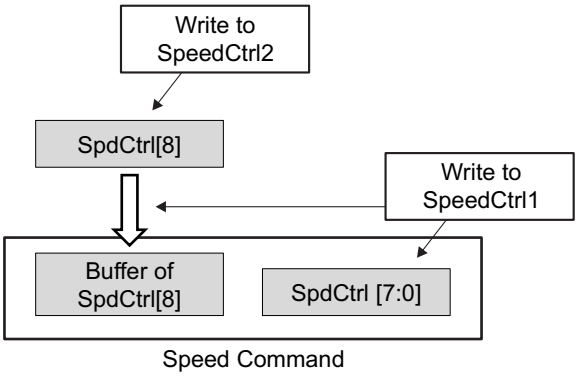


Figure 23. I²C Mode Speed Control

8.4.5.5 Closed Loop Accelerate

To prevent sudden changes in the torque applied to the motor which could result in acoustic noise, the DRV10983 provides the option of limiting the maximum rate at which the speed command changes. ClsLpAccel[2:0] can be programmed to set the maximum rate at which the speed command changes (shown in Figure 24).

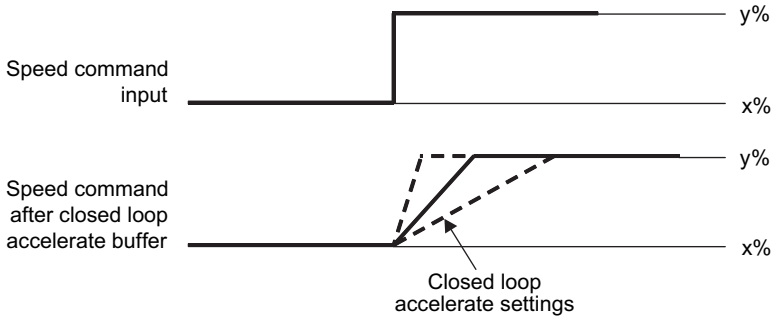


Figure 24. Closed-Loop Accelerate

8.4.5.6 Control Coefficient

The DRV10983 continuously measures the motor current and uses this information to control the drive state of the motor when operating in closed loop mode. In applications where noise makes it difficult to control the commutation optimally, the CtrlCoef[1:0] can be used to attenuate the feedback used for closed loop control. The loop will be less reactive to the noise on the feedback and provide for a smoother output.

8.4.5.7 Commutation Control Advance Angle

To achieve the best efficiency, it is often desirable to control the drive state of the motor so that the phase current of the motor is aligned with the BEMF voltage of the motor.

To align the phase current of the motor with the BEMF voltage of the motor, consider the inductive effect of the motor. The voltage applied to the motor should be applied in advance of the BEMF voltage of the motor (see Figure 25). The DRV10983 provides configuration bits for controlling the time (t_{adv}) between the driving voltage and BEMF.

For motors with salient pole structures, aligning the motor BEMF voltage with the motor current may not achieve the best efficiency. In these applications, the timing advance should be adjusted accordingly. Accomplish this by operating the system at constant speed and load conditions and by adjusting the t_{adv} until the minimum current is achieved.

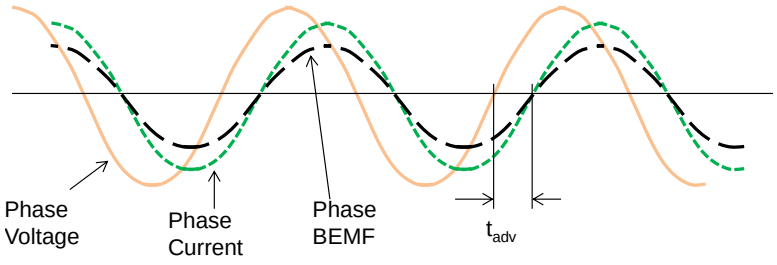


Figure 25. Advance Time (t_{adv}) Definition

The DRV10983 has two options for adjusting the motor commutate advance time. When CtrlAdvMd = 0, mode 0 is selected. When CtrlAdvMd = 1, mode 1 is selected.

Mode 0: t_{adv} is maintained to be a fixed time relative to the estimated BEMF zero cross as determined by Equation 3.

$$t_{adv} = t_{SETTING} \quad (3)$$

Mode 1: t_{adv} is maintained to be a variable time relative to the estimated BEMF zero cross as determined by Equation 4.

$$t_{adv} = t_{SETTING} \times (U\text{-}BEMF)/U. \quad (4)$$

where

- U is the phase voltage amplitude
- BEMF is phase BEMF amplitude

$t_{SETTING}$ (in µs) is determined by the configuration of the TCtrlAdv [6:4] and TCtrlAdv [3:0] bits as defined in Equation 5. For convenience, the available $t_{SETTING}$ values are provided in Table 5.

$$t_{SETTING} = 2.5\ \mu s \times [TCtrlAdv[3:0]] << TCtrlAdv[6:4] \quad (5)$$

Table 5. Configuring Commutation Advance Timing by Adjusting $t_{SETTING}$

$t_{SETTING}$ (µs)	TCtrlAdv [6:0]	HEX	$t_{SETTING}$ (µs)	TCtrlAdv [6:0]	HEX	$t_{SETTING}$ (µs)	TCtrlAdv [6:0]	HEX
0.0	0000000	00	90	0101001	29	800	1011010	5A
2.5	0000001	01	100	0101010	2A	880	1011011	5B
5	0000010	02	110	0101011	2B	960	1011100	5C
7.5	0000011	03	120	0101100	2C	1040	1011101	5D
10	0000100	04	130	0101101	2D	1120	1011110	5E
12.5	0000101	05	140	0101110	2E	1200	1011111	5F
15	0000110	06	150	0101111	2F	1280	1101000	68
17.5	0000111	07	160	0111000	38	1440	1101001	69
20	0001000	08	180	0111001	39	1600	1101010	6A
22.5	0001001	09	200	0111010	3A	1760	1101011	6B
25	0001010	0A	220	0111011	3B	1920	1101100	6C
27.5	0001011	0B	240	0111100	3C	2080	1101101	6D
30	0001100	0C	260	0111101	3D	2240	1101110	6E
32.5	0001101	0D	280	0111110	3E	2400	1101111	6F
35	0001110	0E	300	0111111	3F	2560	1111000	78
37.5	0001111	0F	320	1001000	48	2880	1111001	79
40	0011000	18	360	1001001	49	3200	1111010	7A
45	0011001	19	400	1001010	4A	3520	1111011	7B
50	0011010	1A	440	1001011	4B	3840	1111100	7C
55	0011011	1B	480	1001100	4C	4160	1111101	7D
60	0011100	1C	520	1001101	4D	4480	1111110	7E

Table 5. Configuring Commutation Advance Timing by Adjusting $t_{SETTING}$ (continued)

$t_{SETTING}$ (µs)	TCtrlAdv [6:0]	HEX	$t_{SETTING}$ (µs)	TCtrlAdv [6:0]	HEX	$t_{SETTING}$ (µs)	TCtrlAdv [6:0]	HEX
65	0011101	1D	560	1001110	4E	4800	1111111	7F
70	0011110	1E	600	1001111	4F			
75	0011111	1F	640	1011000	58			
80	0101000	28	720	1011001	59			

8.4.6 Current Limit

The DRV10983 has several current limit modes to help ensure optimal control of the motor and to ensure safe operation. The various current limit modes are listed in Table 6. Acceleration current limit is used to provide a means of controlling the amount of current delivered to the motor. This is useful when the system needs to limit the amount of current pulled from the power supply during motor start-up. The lock detection current limit is a configurable threshold that can be used to limit the current applied to the motor. Overcurrent protection is used to protect the device; therefore, it cannot be disabled or configured to a different threshold. The current limit modes are described in the following sections.

Table 6. DRV10983 Current Limit Modes

Current Limit Mode	Situation	Action	Fault Diagnose
Acceleration current limit	Motor start	Limit the output voltage amplitude	No fault
Lock detection current limit	Motor locked	Stop driving the motor and enter lock state	Mechanical rotation error
Overcurrent shutdown	Phase to phase	Stop driving and recover when OC signal disappeared	Circuit connection

8.4.6.1 Acceleration Current Limit

The acceleration current limit limits the voltage applied to the motor to prevent the current from exceeding the programmed threshold. The acceleration current limit threshold is configured by writing the SWiLimitThr[3:0] bits to select I_{LIMIT}. The acceleration current limit does not use a direct measurement of current. It uses the programmed motor resistance, Rm, and programmed motor velocity constant, Kt, to limit the voltage applied to the motor, U, as shown in Figure 26 and Equation 6.

When the acceleration current limit is active, it does not stop the motor from spinning nor does it trigger a fault. The acceleration current limit function is only available in closed loop control.

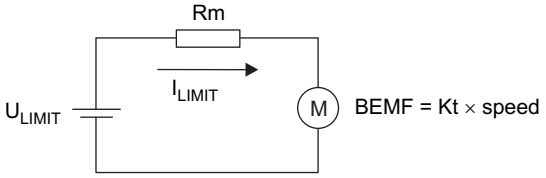


Figure 26. Acceleration Current Limit

$$U_{LIMIT} = I_{LIMIT} \times Rm + Speed \times Kt \quad (6)$$

8.4.7 Lock Detect and Fault Handling

The DRV10983 provides several options for determining if the motor becomes locked as a result of some external torque. Five lock detect schemes work together to ensure the lock condition is detected quickly and reliably. Figure 27 shows the logic which integrates the various lock detect schemes. When a lock condition is detected, the DRV10983 device takes action to prevent continuously driving the motor in order to prevent damage to the system or the motor.

In addition to detecting if there is a locked motor condition, the DRV10983 also identifies and takes action if there is no motor connected to the system.

Each of the five lock-detect schemes and the no motor detection can be disabled by respective register bits LockEn[5:0].

When a lock condition is detected, the MtrLck in the Status register is set. The FaultCode register provides an indication of which of the six different conditions was detected on Lock5 to Lock0. These bits are reset when the motor restarts. The bits in the FaultCode register are set even if the lock detect scheme is disabled.

The DRV10983 reacts to either locked rotor or no motor connected conditions by putting the output drivers into a high-impedance state. To prevent the energy in the motor from pumping the supply voltage, the DRV10983 incorporates an anti-voltage-surge (AVS) process whenever the output stages transition into the high-impedance state. The AVS function is described in *AVS Function*. After entering the high-impedance state as a result of a fault condition, the system tries to restart after t_{LOCK_OFF}.

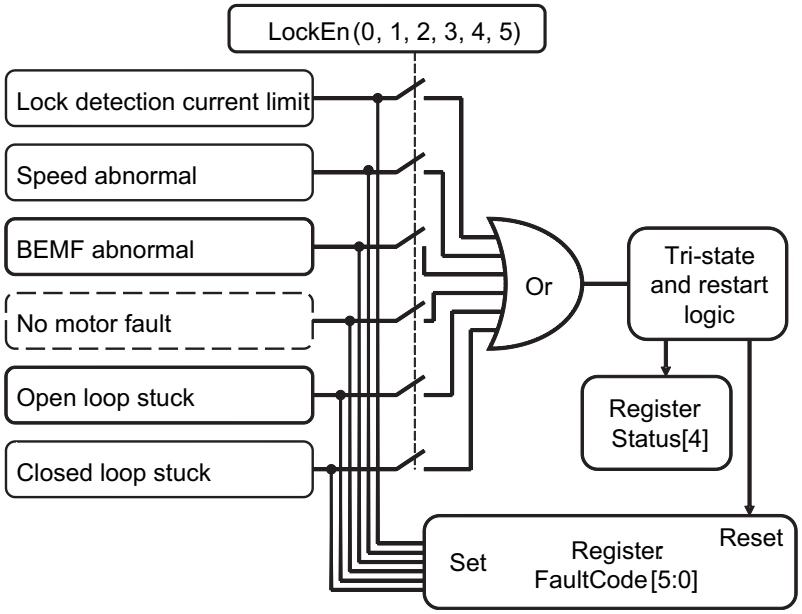


Figure 27. Lock Detect and Fault Diagnose

8.4.7.1 Lock0: Lock Detection Current Limit Triggered

The lock detection current limit function provides a configurable threshold for limiting the current to prevent damage to the system. This is often tripped in the event of a sudden locked rotor condition. The DRV10983 continuously monitors the current in the low-side drivers as shown in Figure 28. If the current goes higher than the threshold configured by the HWiLimitThr[2:0] bits, then the DRV10983 stops driving the motor by placing the output phases into a high-impedance state. The MtrLck bit is set and a lock condition is reported. It retries after t_{LOCK_OFF}.

Set the lock detection current limit to a higher value than the acceleration current limit.

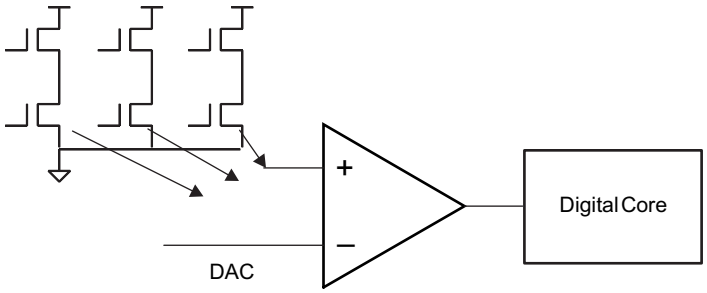


Figure 28. Lock Detection Current Limit

8.4.7.2 Lock1: Abnormal Speed

If motor is operating normally, the motor BEMF should always be less than output amplitude. The DRV10983 uses two methods of monitoring the BEMF in the system. The U phase current is monitored to maintain an estimate of BEMF based on the setting for Rm[6:0]. In addition, the BEMF is estimated based on the operation speed of the motor and the setting for Kt[6:0]. Figure 29 shows the method for using this information to detect a lock condition. If motor BEMF is much higher than output amplitude for a certain period of time, t_{LCK_ETR}, it means the estimated speed is wrong, and the motor has gotten out of phase.

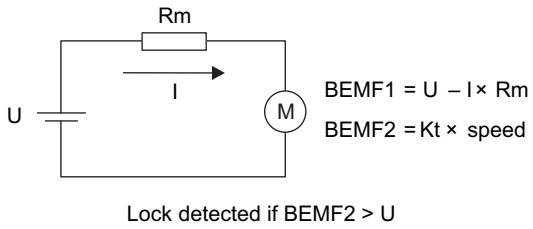


Figure 29. Lock Detection 1

8.4.7.3 Lock2: Abnormal Kt

For any given motor, the integrated value of BEMF during half of an electrical cycle is constant. It is determined by motor velocity constant (Kt_{PH}) (see Figure 30). It is true regardless of whether the motor is running fast or slow. This constant value is continuously monitored by calculation and used as criteria to determine the motor lock condition. It is referred to as Ktc.

Based on the Kt_{PH} value programmed, create a range from Kt_low to Kt_high, if the Ktc goes beyond the range for a certain period of time, t_{LCK_ETR}, lock is detected. Kt_low and Kt_high are determined by KtLckThr[1:0] (see Figure 31).

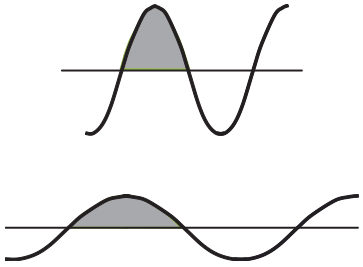


Figure 30. BEMF Integration

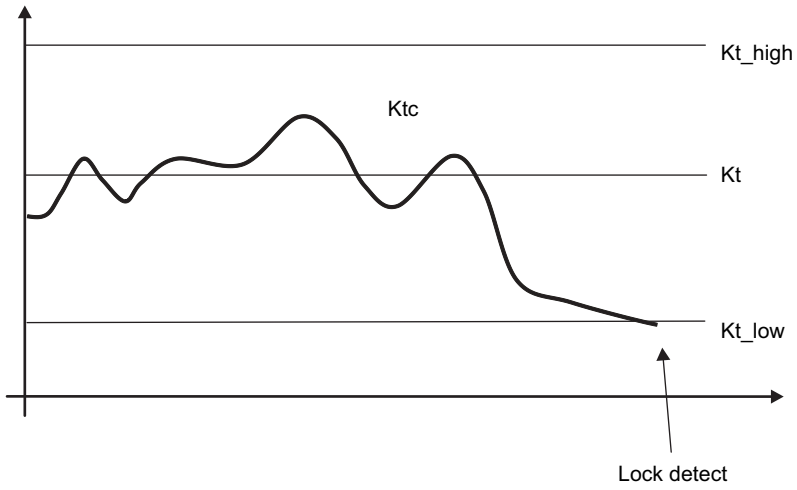


Figure 31. Abnormal Kt Lock Detect

8.4.7.4 Lock3 (Fault3): No Motor Fault

The phase U current is checked after transitioning from open loop to closed loop. If phase U current is not greater than 140 mA then the motor is not connected as shown in Figure 32. This condition is treated and reported as a fault.

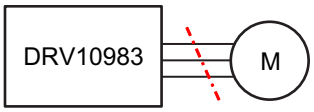


Figure 32. No Motor Error

8.4.7.5 Lock4: Open Loop Motor Stuck Lock

Lock4 is used to detect locked motor conditions while the motor start sequence is in open loop.

For a successful startup, motor speed should equal to open to closed loop handoff threshold when the motor is transitioning into closed loop. However, if the motor is locked, the motor speed is not able to match the open loop drive rate.

If the motor BEMF is not detected for one electrical cycle after the open loop drive rate exceeds the threshold, then the open loop was unsuccessful as a result of a locked rotor condition.

8.4.7.6 Lock5: Closed Loop Motor Stuck Lock

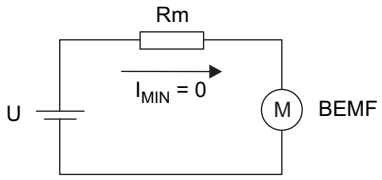
If the motor suddenly becomes locked, motor speed and Ktc are not able to be refreshed because motor BEMF zero cross may not appear after the lock. In this condition, lock can also be detected by the following scheme: if the current commutation period is 2× longer than the previous period.

8.4.8 AVS Function

When a motor is driven, energy is transferred from the power supply into it. Some of this energy is stored in the form of inductive energy or as mechanical energy. The DRV10983 includes circuits to prevent this energy from being returned to the power supply which could result in pumping up the VCC voltage. This function is referred to as the AVS and acts to protect the DRV10983 as well as other circuits that share the same VCC connection. Two forms of AVS protection are used to prevent both the mechanical energy or the inductive energy from being returned to the supply. Each of these modes can be independently disabled through the register configuration bits AVSMEn and AVSIndEn.

8.4.8.1 Mechanical AVS Function

If the speed command suddenly drops such that the BEMF voltage generated by the motor is greater than the voltage that is applied to the motor, then the mechanical energy of the motor is returned to the power supply and the VCC voltage surges. The mechanical AVS function works to prevent this from happening. The DRV10983 buffers the speed command value and limits the resulting output voltage, U_{MIN}, so that it is not less than the BEMF voltage of the motor. The BEMF voltage in the mechanical AVS function is determined using the programmed value for the Kt of the motor (Kt[6:0]) along with the speed. Figure 33 shows the criteria used by the mechanical AVS function.



U_{MIN} = BEMF + I_{MIN} × Rm = BEMF

Figure 33. Mechanical AVS

The mechanical AVS function can operate in one of two modes, which can be configured by the register bit AVSMMd:

AVSMMd = 0 – AVS mode is always active to prevent the applied voltage from being less than the BEMF voltage.

AVSMMd = 1 – AVS mode becomes active when VCC reaches 24 V. The motor acts as a generator and returns energy into the power supply until VCC reaches 24 V. This mode can be used to enable faster deceleration of the motor in applications where returning energy to the power supply is allowed.

8.4.8.2 Inductive AVS Function

When DRV10983 transitions from driving the motor into a high-impedance state, the inductive current in the motor windings continues to flow and the energy returns to the power supply through the intrinsic body diodes in the FET output stage (see Figure 34).

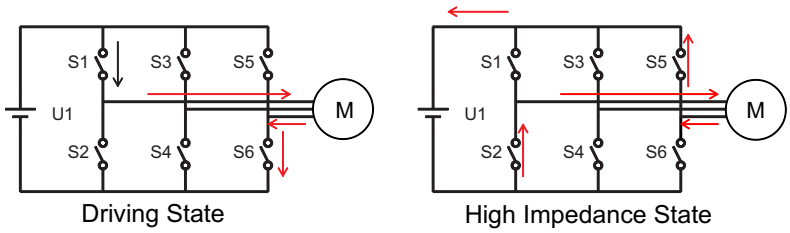


Figure 34. Inductive Mode Voltage Surge

To prevent the inductive energy from being returned to the power supply, the DRV10983 system transitions from driving to a high-impedance state by first turning off the active high-side drivers, and then after a fixed period of time, turning off the low-side drivers (see Figure 35).

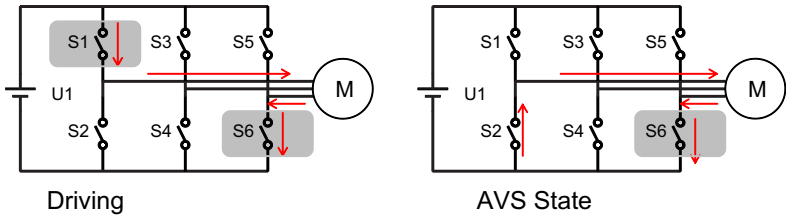


Figure 35. Inductive AVS

In this example, current is applied to the motor through the high-side driver on phase U (S1) and returned through the low-side driver on phase W (S6). The high-side driver on phase U is turned off and after a period of time (to allow the inductive energy in the resulting LR circuit to decay) the low-side driver on phase W is turned off.

8.4.9 PWM Output

The DRV10983 has 16 options for PWM dead time which can be used to configure the time between one of the bridge FETs turning off and the complementary FET turning on. Deadtime[3:0] can be used to configure dead times between 40 ns and 640 ns. Take care that the dead time is long enough to prevent the bridge FETs from shooting through. The recommend minimum dead time is 400 ns for 24-V VCC and 360 ns for 12-V VCC.

The DRV10983 offers two options for PWM switching frequency. When the configuration bit DoubleFreq is set to 0, the output PWM frequency will be 25 kHz and when DoubleFreq is set to 1, the output PWM frequency will be 50 kHz.

8.4.10 FG Customized Configuration

The DRV10983 provides information about the motor speed through the frequency generate (FG) pin. FG also provides information about the driving state of the DRV10983.

8.4.10.1 FG Output Frequency

The FG output frequency can be configured by FGcycle[1:0]. The default FG toggles once every electrical cycle (FGcycle = 00). Many applications configure the FG output so that it provides two pulses for every mechanical rotation of the motor. The configuration bits provided in DRV10983 can accomplish this for 4-pole, 6-pole, 8-pole, and 12-pole motors, as shown in Figure 36.

Figure 36 shows the DRV10983 has been configured to provide FG pulses once every electrical cycle (4 pole), twice every three electrical cycle (6 pole), once every two electrical cycles (8 pole), and once every three electrical cycles (12 pole).

Note that when it is set to 2 FG pulses every three electrical cycles, the FG output is not 50% duty cycle. Motor speed is able to be measured by monitoring the rising edge of the FG output.

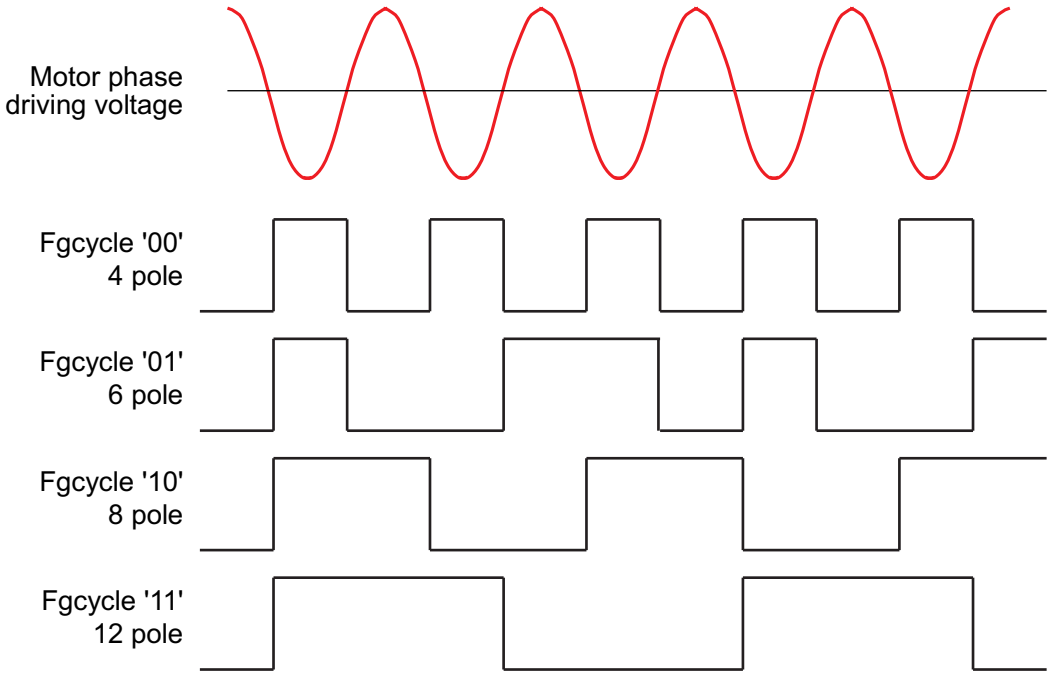


Figure 36. FG Frequency Divider

8.4.10.2 FG Open-Loop and Lock Behavior

Note that the FG output reflects the driving state of the motor. During normal closed loop behavior, the driving state and the actual state of the motor are synchronized. During open loop acceleration, however, this may not reflect the actual motor speed. During a locked motor condition, the FG output is driven high.

The DRV10983 provides three options for controlling the FG output during open loop as shown in Figure 37. The selection of these options is determined by the FGOLsel[1:0] setting.

- Option0: Open loop output FG based on driving frequency
- Option1: Open loop no FG output (keep high)
- Option2: FG output based on driving frequency at the first power-on start-up, and no FG output (keep high) for any subsequent restarts

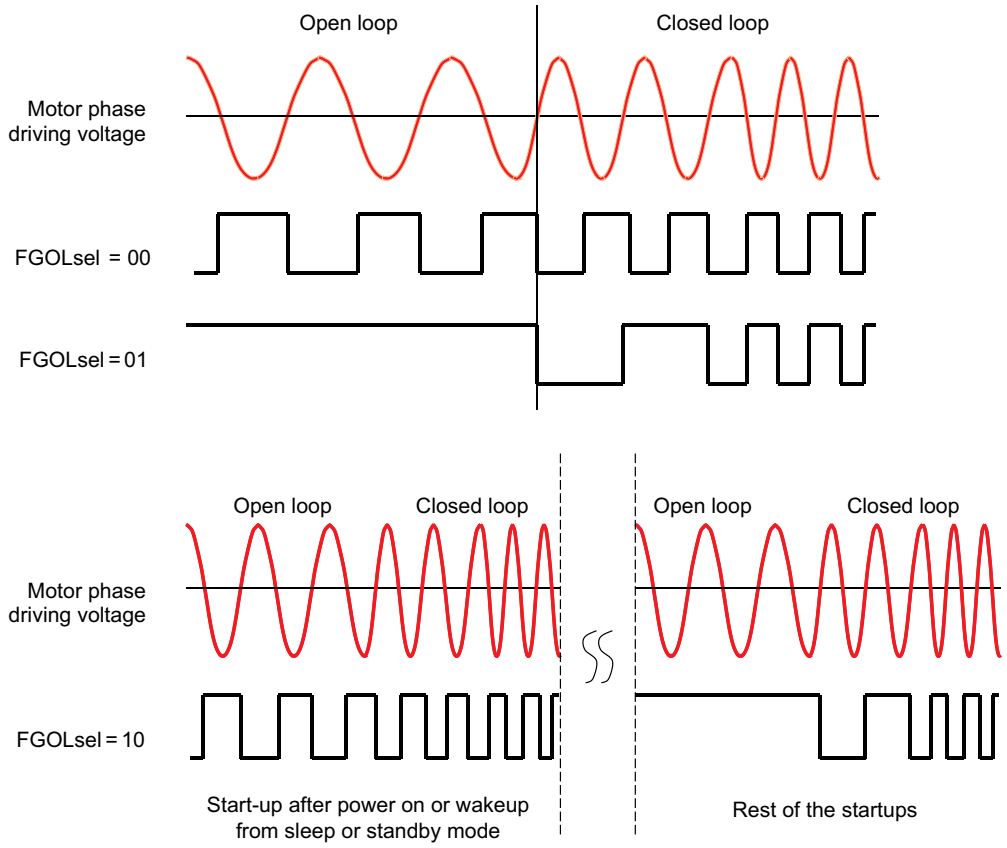


Figure 37. FG Behavior During Open Loop

8.4.11 Diagnostics and Visibility

The DRV10983 offers extensive visibility into the motor system operation conditions stored in internal registers. This information can be monitored through the I^2C interface. Information can be monitored relating to the device status, motor speed, supply voltage, speed command, motor phase voltage amplitude, fault status, and others. The data is updated on the fly.

8.4.11.1 Motor Status Readback

The motor status register provides information on overtemperature (OverTemp), sleep or standby state (Slp_Stdby), over current (OverCurr), and locked rotor (MtrLck).

8.4.11.2 Motor Speed Readback

The motor operation speed is automatically updated in register MotorSpeed1 and MotorSpeed2 while the motor is spinning. MotorSpeed1 contains the 8 most significant bits and MotorSpeed2 contains the 8 least significant bits. The value is determined by the period for calculated BEMF zero crossings on phase U. The electrical speed of the motor is denoted as *Velocity (Hz)* and is calculated as shown in Equation 7.

Velocity (Hz) = {MotorSpeed1:MotorSpeed2} / 10 (7)

As an example consider the following:

MotorSpeed1 = 0x01;
MotorSpeed2 = 0xFF;
Velocity = 512 (0x01FF) / 10 = 51 Hz

For a 4-pole motor, this translates to: $51 \frac{\text{ecycles}}{\text{second}} \times \frac{1}{2} \frac{\text{mechcycle}}{\text{ecycle}} \times 60 \frac{\text{second}}{\text{minute}} = 1530 \text{ RPM}$

8.4.11.2.1 Two-Byte Register Readback

Several of the registers such as MotorSpeed report data that is contained in two registers.

To make sure that the data does not change between the reading of the first and second register reads, the DRV10983 implements a special scheme to synchronize the reading of MSB and LSB data. To ensure valid data is read when reading a two register value, use the following sequence.

1. Read the MSB.
2. Read the LSB.

Figure 38 shows the two-register readback circuit. When the MSB is read, the controller takes a snapshot of the LSB. The LSB data is stored in one extra register byte, which is shown as MotorSpeedBuffer[7:0]. When the LSB is read, the value of MotorSpeedBuffer[7:0] is sent.

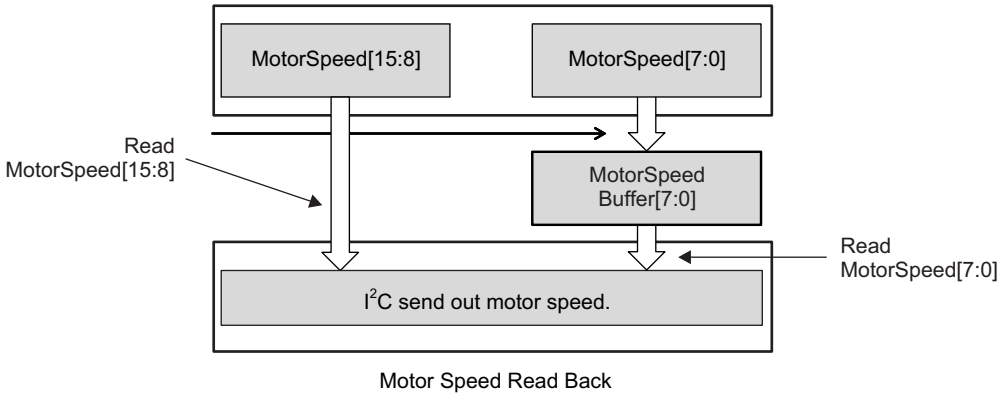


Figure 38. Two-Byte Register Readback

8.4.11.3 Motor Electrical Period Readback

The motor operation electrical period is automatically updated in register MotorPeriod1 and MotorPeriod2 while the motor is spinning. MotorPeriod1 is the MSB and MotorPeriod2 is the LSB. The electrical period is measured as the time between calculated BEMF zero crossings for phase U. The electrical period of the motor is denoted as d as t_{ELE_PERIOD} (µs) and is calculated as shown in Equation 8.

$$t_{ELE\_PERIOD}\ (\mu s) = \{MotorPeriod1:MotorPeriod2\} \times 10 \quad (8)$$

As an example consider the following:

MotorPeriod1 = 0x01;

MotorPeriod2 = 0xFF;

t_{ELE_PERIOD} = 512 (0x01FF) × 10 = 5120 µs

The motor electrical period and motor speed satisfies the condition of Equation 9.

$$t_{ELE\_PERIOD}\ (s) \times Velocity\ (Hz) = 1 \quad (9)$$

8.4.11.4 Motor Velocity Constant Readback

For any given motor, the integrated value of BEMF during half of an electronic cycle will be constant, Ktc (see *Lock2: Abnormal Kt*).

The integration of the motor BEMF is processed periodically (updated every electrical cycle) while the motor is spinning. The result is stored in register MotorKt1 and MotorKt2.

The relationship is shown in Equation 10.

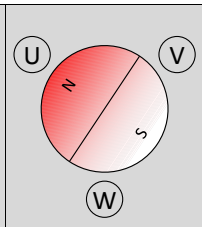
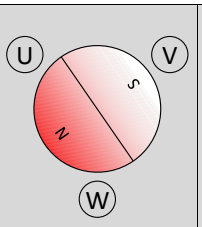
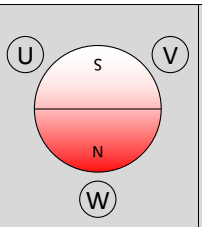
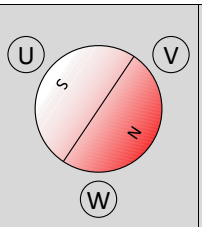
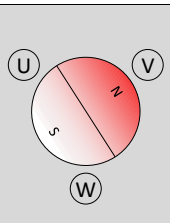
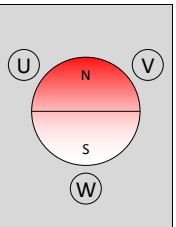
$$Ktc\ (V/Hz) = \{MotorKt1:MotorKt2\} / 2 / 1090 \quad (10)$$

8.4.11.5 Motor Estimated Position by IPD

After inductive sense is executed the rotor position is detected within 60 electrical degrees of resolution. The position is stored in register IPDPosition.

The value stored in IPD Position corresponds to one of the six motor positions plus the IPD Advance Angle as shown in Table 7. For more about information about IPD, see *IPD* .

Table 7. IPD Position Readback

						
Rotor position (°)	0	60	120	180	240	300
Data1	0	43	85	128	171	213
IPD Advance Angle	30	60	90	120		
Data2	22	44	63	85		
Register date	(Data1 + Data2) mod (256)					

8.4.11.6 Supply Voltage Readback

The power supply is monitored periodically during motor operation. This information is available in register SupplyVoltage. The power supply voltage is recorded as shown in Equation 11.

$$V_{POWERSUPPLY}\ (V) = \text{Supply Voltage} \times 30\ V / 256 \quad (11)$$

8.4.11.7 Speed Command Readback

The DRV10983 converts the various types of speed command into a speed command value (SpeedCmd) as shown in Figure 39. By reading SpeedCmd, the user can observe PWM input duty (PWM digital mode), analog voltage (analog mode), or I^2C data (I^2C mode). This value is calculated as shown in Equation 12.

Equation 12 shows how the speed command as a percentage can be calculated and set in SpeedCmd.

$$Duty_{SPEED}\ (\%) = SpeedCmd \times 100\% / 255$$

where

- $Duty_{SPEED}$ = Speed command as a percentage
- SpeedCmd = Register value

(12)

8.4.11.8 Speed Command Buffer Readback

If acceleration current limit and AVS are enabled, the PWM duty cycle output (read back at spdCmdBuffer) may not always match the input command (read back at SpeedCmd) shown in Figure 39. See *AVS Function* and *Current Limit* .

By reading the value of spdCmdBuffer, the user can observe buffered speed command (output PWM duty cycle) to the motor.

Equation 13 shows how the buffered speed is calculated.

$$Duty_{OUTPUT}\ (\%) = spdCmdBuffer \times 100\% / 255$$

where

- $Duty_{OUTPUT}$ = The maximum duty cycle of the output PWM, which represents the output amplitude in percentage.
- spdCmdBuffer = Register value

(13)

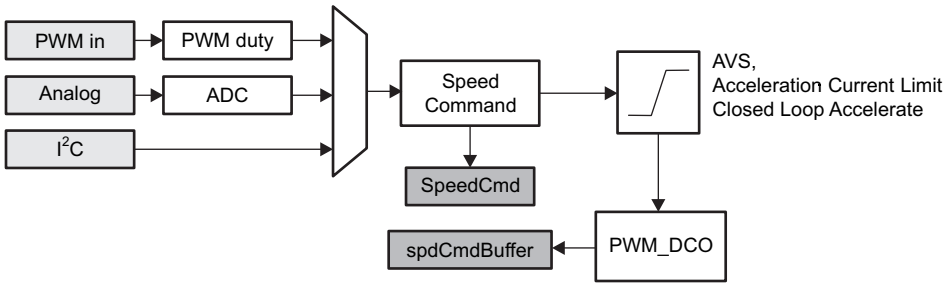


Figure 39. SpeedCmd and spdCmdBuffer Register

8.4.11.9 Fault Diagnostics

See *Lock Detect and Fault Handling*.

8.5 Register Maps

8.5.1 I²C Serial Interface

The DRV10983 provides an I²C slave interface with slave address 101 0010. TI recommends a pullup resistor 4.7 kΩ to 3.3 V for I²C interface port SCL and SDA.

Four read/write registers (0x00:0x03) are used to set motor speed and control device registers and EEPROM. Device operation status can be read back through 12 read-only registers (0x10:0x1E). Another 12 EEPROM registers (0x20:0x2B) can be accessed to program motor parameters and optimize the spin-up profile for the application.

8.5.2 Register Map

Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0
SpeedCtrl1 (1)	0x00	SpdCtrl[7:0]							
SpeedCtrl2 (1)	0x01	OverRide							SpdCtrl[8]
DevCtrl (1)	0x02	enProgKey[7:0]							
EECtrl (1)	0x03	sleepDis	SIdata	eeRefresh	eeWrite				
Status (2)	0x10	OverTemp	Slp_Stdby	OverCurr	MtrLck				
MotorSpeed1 (2)	0x11	MotorSpeed[15:8]							
MotorSpeed2 (2)	0x12	MotorSpeed[7:0]							
MotorPeriod1 (2)	0x13	MotorPeriod[15:8]							
MotorPeriod2 (2)	0x14	MotorPeriod[7:0]							
MotorKt1 (2)	0x15	MotorKt[15:8]							
MotorKt2 (2)	0x16	MotorKt[7:0]							
IPDPosition (2)	0x19	IPDPosition[7:0]							
SupplyVoltage (2)	0x1A	SupplyVoltage [7:0]							
SpeedCmd (2)	0x1B	SpeedCmd [7:0]							
spdCmdBuffer (2)	0x1C	spdCmdBuffer[7:0]							
FaultCode (2)	0x1E			Lock5	Lock4	Fault3	Lock2	Lock1	Lock0
MotorParam1 (3)	0x20	DoubleFreq	Rm[6:0]						
MotorParam2 (3)	0x21	AdjMode	Kt[6:0]						
MotorParam3 (3)	0x22	CtrlAdvMd	TCtrlAdv[6:0]						
SysOpt1 (3)	0x23	ISDThr[1:0]		IPDAdvcAgl[1:0]		ISDen	RvsDrEn	RvsDrThr[1:0]	
SysOpt2 (3)	0x24	OpenLCurr[1:0]		OpLCurrRt[2:0]			BrkDoneThr[2:0]		
SysOpt3 (3)	0x25	CtrlCoef[1:0]		StAccel2[2:0]			StAccel[2:0]		
SysOpt4 (3)	0x26	Op2ClsThr[4:0]					AlignTime[2:0]		
SysOpt5 (3)	0x27	LockEn[3:0]				AVSIndEn	AVSMEn	AVSMMd	IPDRlsMd
SysOpt6 (3)	0x28	SWiLimitThr[3:0]				HWiLimitThr[2:0]			
SysOpt7 (3)	0x29	LockEn5	ClsLpAccel[2:0]			Deadtime[3:0]			
SysOpt8 (3)	0x2A	IPDCurrThr[3:0]				LockEn4	VregSel	IPDClk[1:0]	
SysOpt9 (3)	0x2B	FGOLsel[1:0]		FGcycle[1:0]		KtLckThr[1:0]		SpdCtrlMd	CLoopDis

(1) R/W
(2) Read only
(3) EEPROM

Table 8. Default EEPROM Value

Address	Default Value
0x20	0x4A
0x21	0x4E
0x22	0x2A
0x23	0x00
0x24	0x98
0x25	0xE4
0x26	0x7A
0x27	0xFC
0x28	0x69
0x29	0xB7
0x2A	0xAD
0x2B	0x0C

8.5.3 Register Definition

Table 9. Register Description

Register			Data	Description
Name	Address	Bits		
SpeedCtrl1 (1)	0x00	7:0	SpdCtrl[7:0]	8 LSB of a 9-bit value used for the motor speed. If OverRide = 1, the user can directly control the motor speed by writing to the register through I^2C.
SpeedCtrl2 (1)	0x01	7	OverRide	Use to control the SpdCtrl [8:0] bits. If OverRide = 1, the user can write the speed command through I^2C.
		6:1	N/A	N/A
		0	SpdCtrl [8]	MSB of a 9-bit value used for the motor speed. If OverRide = 1, user can directly control the motor speed by writing to the register through I^2C. The MSB should be written first. Digital takes a snapshot of the MSB when LSB is written.
DevCtrl (1)	0x02	7:0	enProgKey[7:0]	8-bit byte use to enable programming in the EEPROM. To program the EEPROM, enProgKey = 1011 0110 (0xB6), followed immediately by eeWrite = 1. Otherwise, enProgKey value is reset.
EECtrl (1)	0x03	7	sleepDis	Set to 1 to disable entering into sleep or standby mode.
		6	SIdata	Set to 1 to enable the writing to the configuration registers.
		5	eeRefresh	Copy EEPROM data to register.
		4	eeWrite	Bit used to program (write) to the EEPROM.
		3:0	N/A	N/A
Status (2)	0x10	7	OverTemp	Bit to indicate device temperature is over its limits.
		6	Slp_Stdby	Bit to indicate that device went into sleep or standby mode.
		5	OverCurr	Bit to indicate that a phase to phase overcurrent event happened. This is a sticky bit, once written, it stays high even if overcurrent signal goes low. This bit is cleared on Read.
		4	MtrLck	Bit to indicate that the motor is locked.
		3	N/A	N/A
		2	N/A	N/A
		1	N/A	N/A
		0	N/A	N/A

(1) R/W
(2) Read only

Table 9. Register Description (continued)

Register			Data	Description
Name	Address	Bits		
Motor Speed1 (2)	0x11	7:0	MotorSpeed [15:8]	16-bit value indicating the motor speed. Always read the MotorSpeed1 first. Velocity (Hz) = {MotorSpeed1:MotorSpeed2} / 10 For example: MotorSpeed1 = 0x01, MotorSpeed2 = 0xFF, Motor Speed = 0x01FF (511) / 10 = 51 Hz
Motor Speed2 (2)	0x12	7:0	MotorSpeed [7:0]	
Motor Period1 (2)	0x13	7:0	MotorPeriod [15:8]	16-bit value indicating the motor period. Always read the MotorPeriod1 first. t_{ELE_PERIOD} (µs) = {MotorPeriod1:MotorPeriod2} × 10 For example: MotorPeriod1 = 0x01, MotorPeriod2 = 0xFF, Motor Period = 0x01FF (511) × 10 = 5.1 ms
Motor Period2 (2)	0x14	7:0	MotorPeriod [7:0]	
MotorKt1 (2)	0x15	7:0	MotorKt[15:8]	16-bit value indicating the motor measured velocity constant. Always read the MotorKt1 first. Ktc (V/Hz)= {MotorKt1:MotorKt2} / 2 /1090 {MotorKt1:MotorKt2} corresponding to 2 × Ktph_dig
MotorKt2 (2)	0x16	7:0	MotorKt[7:0]	
IPDPosition (2)	0x19	7:0	IPDPosition [7:0]	8-bit value indicating the estimated motor position during IPD plus the IPD advance angle (see Table 7)
Supply Voltage (2)	0x1A	7:0	SupplyVoltage [7:0]	8-bit value indicating the supply voltage $V_{POWERSUPPLY}$ (V) = SupplyVoltage[7:0] × 30 V /256 For example, SupplyVoltage[7:0] = 0x67, $V_{POWERSUPPLY}$ (V) = 0x67 (102) × 30 / 256 = 12 V
SpeedCmd (2)	0x1B	7:0	SpeedCmd[7:0]	8-bit value indicating the speed command based on analog or PWMin or I^2C. FF indicates 100% speed command.
spdCmd Buffer (2)	0x1C	7:0	spdCmdBuffer [8:1]	8-bit value indicating the speed command after buffer output. FF indicates 100% speed command.
FaultCode (2)	0x1E	7:6	N/A	N/A
		5	Lock5	Stuck in closed loop
		4	Lock4	Stuck in open loop
		3	Fault3	No motor
		2	Lock2	Kt abnormal
		1	Lock1	Speed abnormal
		0	Lock0	Lock detection current limit
Motor Param1 (3)	0x20	7	DoubleFreq	0 = Set driver output frequency to 25 kHz 1 = Set driver output frequency to 50 kHz
		6:0	Rm[6:0]	Rm[6:4] : Number of the Shift bits of the motor phase resistance Rm[3:0] : Significant value of the motor phase resistance Rmdig = R_(ph_ct) / 0.00967 Rmdig = Rm[3:0] ≪ Rm[6:4] See *Motor Resistance* and Table 2
Motor Param2 (3)	0x21	7	AdjMode	Closed loop adjustment mode setting 0 = Full cycle adjustment 1 = Half cycle adjustment
		6:0	Kt[6:0]	Kt[6:4] = Number of the Shift bits of motor velocity constant Kt[3:0] = Significant value of the motor velocity constant 〚Kt〛_(ph_dig) = 1090× 〚Kt〛_ph 〚Kt〛_(ph_dig) = Kt[3:0] ≪ Kt[4:6] See *Motor Velocity Constant* and Table 3.
Motor Param3 (3)	0x22	7	CtrlAdvMd	Motor commutate control advance 0 = Fixed time 1 = Variable time relative to the motor speed and VCC
		6:0	Tdelay[6:0]	t_{delay} [6:4] = Number of the Shift bits of LRTIME t_{delay} [3:0] = Significant value of LRTIME $t_{SETTING}$ = 2.5 µs × {TCtrlAdv[3:0] << TCtrlAdv[6:4]}

(3) EEPROM

Table 9. Register Description (continued)

Register			Data	Description
Name	Address	Bits		
SysOpt1 (3)	0x23	7:6	ISDThr[1:0]	ISD stationary judgment threshold 00 = 6 Hz (80 ms, no zero cross) 01 = 3 Hz (160 ms, no zero cross) 10 = 1.6 Hz (320 ms, no zero cross) 11 = 0.8 Hz (640 ms, no zero cross)
		5:4	IPDAdvcAgl [1:0]	Advancing angle after inductive sense 00 = 30° 01 = 60° 10 = 90° 11 = 120°
		3	ISDen	0 = Initial speed detect (ISD) disable 1 = ISD enable
		2	RvsDrEn	0 = Reverse drive disable 1 = Reverse drive enable
		1:0	RvsDrThr[1:0]	The threshold where device starts to process reverse drive (RvsDr) or brake. 00 = 6.3 Hz 01 = 13 Hz 10 = 26 Hz 11 = 51 Hz
SysOpt2 (3)	0x24	7:6	OpenLCurr[1:0]	Open loop current setting. 00 = 0.2 A 01 = 0.4 A 10 = 0.8 A 11 = 1.6 A
		5:3	OpLCurrRt:[2:0]	Open-loop current ramp-up rate setting 000 = 6 VCC/s 001 = 3 VCC/s 010 = 1.5 VCC/s 011 = 0.7 VCC/s 100 = 0.34 VCC/s 101 = 0.16 VCC/s 110 = 0.07 VCC/s 111 = 0.023 VCC/s
		2:0	BrkDoneThr [2:0]	Braking mode setting 000 = No brake (BrkEn = 0) 001 = 2.7 s 010 = 1.3 s 011 = 0.67 s 100 = 0.33 s 101 = 0.16 s 110 = 0.08 s 111 = 0.04 s

Table 9. Register Description (continued)

Register			Data	Description
Name	Address	Bits		
SysOpt3 (3)	0x25	7:6	CtrlCoef[1:0]	Control coefficient 00 = 0.25 01 = 0.5 10 = 0.75 11 = 1
		5:3	StAccel2[2:0]	Open loop start-up accelerate (second order) 000 = 57 Hz/s^2 001 = 29 Hz/s^2 010 = 14 Hz/s^2 011 = 6.9 Hz/s^2 100 = 3.3 Hz/s^2 101 = 1.6 Hz/s^2 110 = 0.66 Hz/s^2 111 = 0.22 Hz/s^2
		2:0	StAccel[2:0]	Open loop start-up accelerate (first order) 000 = 76 Hz/s 001 = 38 Hz/s 010 = 19 Hz/s 011 = 9.2 Hz/s 100 = 4.5 Hz/s 101 = 2.1 Hz/s 110 = 0.9 Hz/s 111 = 0.3 Hz/s
SysOpt4 (3)	0x26	7:3	Op2ClsThr[4:0]	Open to closed loop threshold 0xxxx = Range 0: n × 0.8 Hz 00000 = N/A 00001 = 0.8 Hz 00111 = 5.6 Hz 01111 = 12 Hz 1xxxx = Range 1: (n + 1) × 12.8 Hz 10000 = 12.8 Hz 10001 = 25.6 Hz 10111 = 192 Hz 11111 = 204.8 Hz
		2:0	AlignTime[2:0]	Align time. 000 = 5.3 s 001 = 2.7 s 010 = 1.3 s 011 = 0.67 s 100 = 0.33 s 101 = 0.16 s 110 = 0.08 s 111 = 0.04 s
SysOpt5 (3)	0x27	7	FaultEn3 (LockEn[3])	No motor fault. Enabled when high
		6	LockEn[2]	Abnormal Kt. Enabled when high
		5	LockEn[1]	Abnormal speed. Enabled when high
		4	LockEn[0]	Lock detection current limit. Enabled when high
		3	AVSIndEn	Inductive AVS enable. Enabled when high
		2	AVSMEn	Mechanical AVS enable. Enabled when high
		1	AVSMMd	Mechanical AVS mode 0 = AVS to VCC 1 = AVS to 24 V
		0	IPDRlsMd	IPD release mode 0 = Brake when inductive release 1 = Hi-z when inductive release

Table 9. Register Description (continued)

Register			Data	Description
Name	Address	Bits		
SysOpt6 (3)	0x28	7:4	SWiLimitThr [3:0]	Acceleration current limit threshold 0000 = No acceleration current limit 0001 = 0.2-A current limit xxxx = n × 0.2 A current limit
		3:1	HWiLimitThr [2:0]	Lock detection current limit threshold (n + 1) × 0.4 A
		0	N/A	N/A
SysOpt7 (3)	0x29	7	LockEn[5]	Stuck in closed loop (no zero cross detected). Enabled when high
		6:4	ClsLpAccel[2:0]	Closed loop accelerate 000 = Inf fast 001 = 48 VCC/s 010 = 48 VCC/s 011 = 0.77 VCC/s 100 = 0.37 VCC/s 101 = 0.19 VCC/s 110 = 0.091 VCC/s 111 = 0.045 VCC/s
		3:0	Deadtime[3:0]	Dead time between HS and LS gate drive for motor phases 0000 = 40 ns xxxx = (n + 1) × 40 ns. Recommended minimum dead time is 400 ns for 24-V VCC and 360 ns for 12-V VCC.
SysOpt8 (3)	0x2A	7:4	IPDCurrThr[3:0]	IPD (inductive sense) current threshold 0000 = No IPD function. Align and Go 0001 = 0.4-A current threshold. xxxx = 0.2 A × (n + 1) current threshold.
		3	LockEn[4]	Open loop stuck (no zero cross detected). Enabled when high
		2	VregSel	Buck regulator voltage select 0: Vreg = 5 V 1: Vreg = 3.3 V
		1:0	IPDClk[1:0]	Inductive sense clock 00 = 12 Hz; 01 = 24 Hz; 10 = 47 Hz; 11 = 95 Hz
SysOpt9 (3)	0x2B	7:6	FGOLsel[1:0]	FG open loop output select 00 = FG outputs in both open loop and closed loop 01 = FG outputs only in closed loop 10 = FG outputs closed loop and the first open loop 11 = Reserved
		5:4	FGcycle[1:0]	FG cycle select 00 = 1 pulse output per electrical cycle 01 = 2 pulses output per 3 electrical cycles 10 = 1 pulse output per 2 electrical cycles 11 = 1 pulse output per 3 electrical cycles
		3:2	KtLckThr[1:0]	Abnormal Kt lock detect threshold 00 = Kt_high = 3/2Kt. Kt_low = 3/4Kt 01 = Kt_high = 2Kt. Kt_low = 3/4Kt 10 = Kt_high = 3/2Kt. Kt_low = 1/2Kt 11 = Kt_high = 2Kt. Kt_low = 1/2Kt
		1	SpdCtrlMd	Speed input mode 0 = Analog input expected at SPEED pin 1 = PWM input expected at SPEED pin
		0	CLoopDis	0 = Transfer to closed loop at Op2ClsThr speed 1 = No transfer to closed loop. Keep in open loop

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV10983 is used in sensorless 3-phase BLDC motor control. The driver provides a high performance, high reliability, flexible and simple solution for appliance fan, pump, and HVAC applications. The following design shows a common application of the DRV10983.

9.2 Typical Application

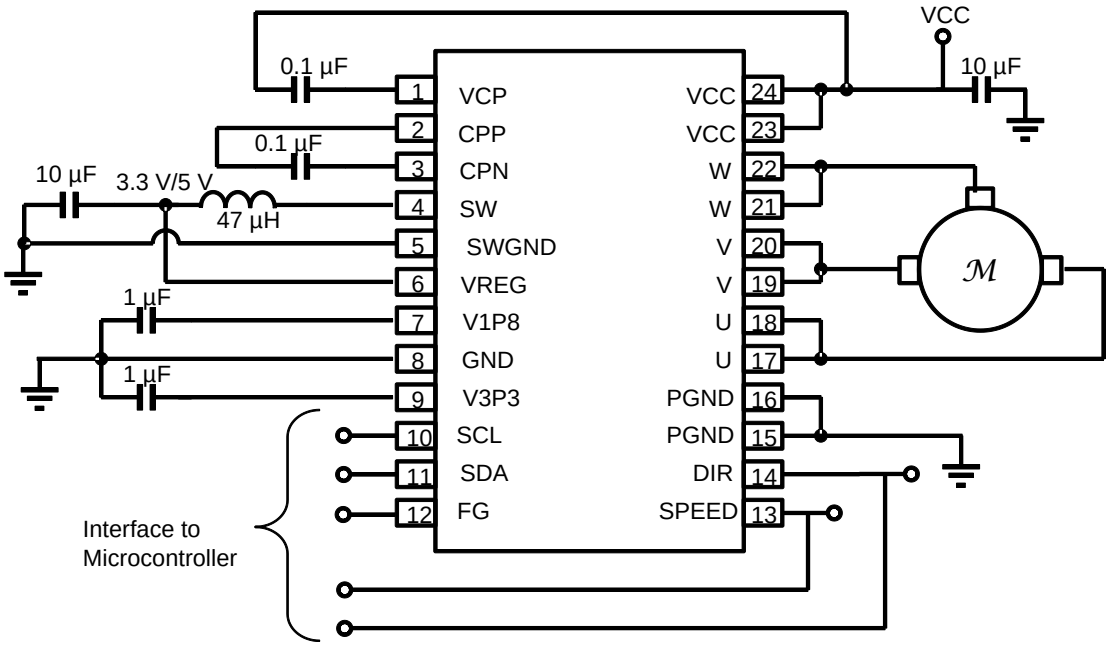


Figure 40. Typical Application Schematic

9.2.1 Design Requirements

Table 10 provides design input parameters and motor parameters for system design.

Table 10. Recommended Application Range

		MIN	TYP	MAX	UNIT
Motor voltage		8	24	28	V
Motor velocity constant	Phase to phase, measured while motor is coasting	0.001		1.8	V/Hz
Motor resistance	1 phase, measured ph-ph and divide by 2	0.3		19	Ω
Motor electrical constant	1 phase; inductance divided by resistance, measured ph-ph is equal to 1 ph	100		5000	µs
Operating closed loop speed	Electrical frequency	1		1000	Hz
Operating current	PGND, GND	0.1		2	A
Absolute maximum current	During start-up or lock condition			3	A

Table 11. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VCC}	VCC	GND	10-µF ceramic capacitor rated for VCC
C_{VCP}	VCP	VCC	0.1-µF ceramic capacitor rated for 10 V
C_{CP}	CPP	CPN	0.1-µF ceramic capacitor rated for VCC × 2
$L_{SW-VREG}$	SW	VREG	47-µH Ferrite rated for 1.15A (inductive mode)
$R_{SW-VREG}$	SW	VREG	39-Ω series resistor rated for ¼ W (resistor mode)
C_{VREG}	VREG	GND	10-µF ceramic capacitor rated for 10 V
C_{V1P8}	V1P8	GND	1-µF ceramic capacitor rated for 5 V
C_{V3P3}	V3P3	GND	1-µF ceramic capacitor rated for 5 V
R_{SCL}	SCL	V3P3	4.75-kΩ pullup to V3P3
R_{SDA}	SDA	V3P3	4.75-kΩ pullup to V3P3
R_{FG}	FG	V3P3	4.75-kΩ pullup to V3P3

9.2.2 Detailed Design Procedure

1. See the *Design Requirements* section and make sure your system meets the recommended application range.
2. See the *DRV10983 and DRV10975 Tuning Guide* and measure the motor parameters.
3. See the *DRV10983 and DRV10975 Tuning Guide*. Configure the parameters using DRV10983 GUI, and optimize the motor operation. The *Tuning Guide* takes the user through all the configurations step by step, including: start-up operation, closed-loop operation, current control, initial positioning, lock detection, and anti-voltage surge.
4. Build your hardware based on *Layout Guidelines*.
5. Connect the device into system and validate your system solution.

9.2.3 Application Curves

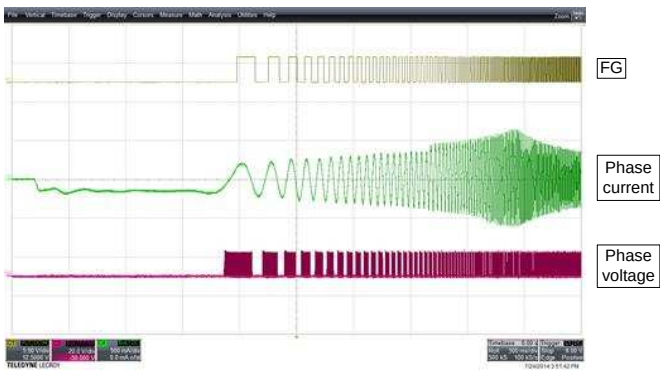


Figure 41. DRV10983 Start-Up Waveform

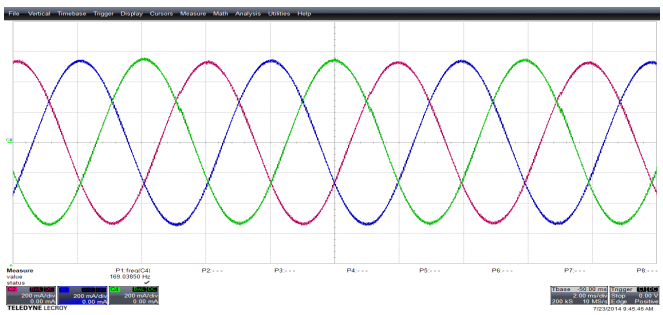


Figure 42. DRV10983 Operation Current Waveform

10 Power Supply Recommendations

The DRV10983 is designed to operate from an input voltage supply, $V_{(VCC)}$, range between 8 V and 28 V. The user must place a 10-µF ceramic capacitor rated for VCC as close as possible to the VCC and GND pin.

If the power supply ripple is more than 200 mV, in addition to the local decoupling capacitors, a bulk capacitance is required and must be sized according to the application requirements. If the bulk capacitance is implemented in the application, the user can reduce the value of the local ceramic capacitor to 1 µF.

11 Layout

11.1 Layout Guidelines

- Place VCC, GND, U, V, and W pins with thick traces because high current passes through these traces.
- Place the 10-µF capacitor between VCC and GND, and as close to the VCC and GND pins as possible.
- Place the capacitor between CPP and CPN, and as close to the CPP and CPN pins as possible.
- Connect the GND, PGND, and SWGND under the thermal pad.
- Keep the thermal pad connection as large as possible, both on the bottom side and top side. It should be one piece of copper without any gaps.

11.2 Layout Example

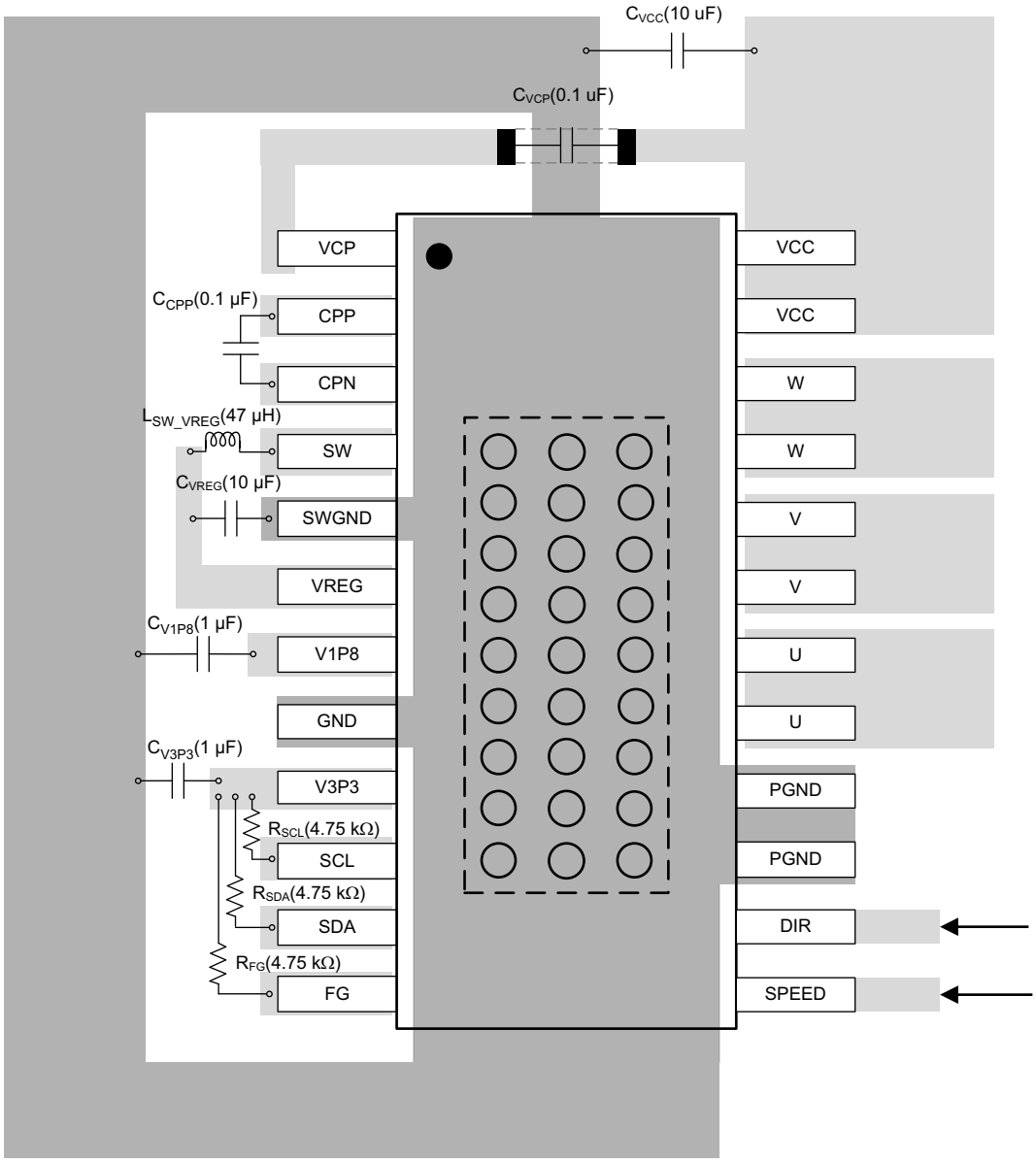


Figure 43. Layout Schematic

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *DRV10983 and DRV10975 Tuning Guide*

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 12. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DRV10983	Click here	Click here	Click here	Click here	Click here
DRV10983Z	Click here	Click here	Click here	Click here	Click here

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.7 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV10983PWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV10983	Samples
DRV10983PWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV10983	Samples
DRV10983ZPWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV10983Z	Samples
DRV10983ZPWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV10983Z	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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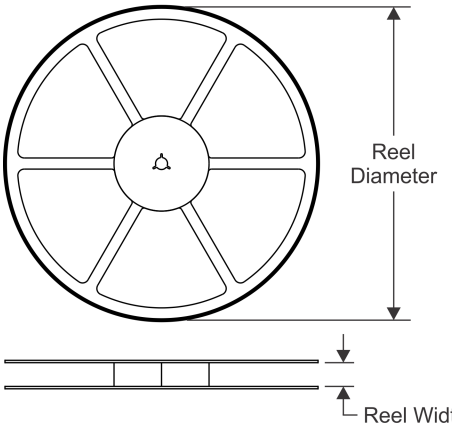
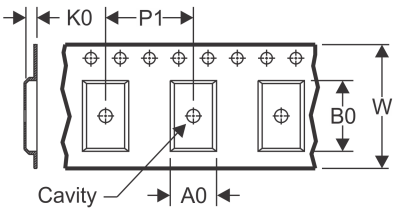
TAPE AND REEL INFORMATION

REEL DIMENSIONS

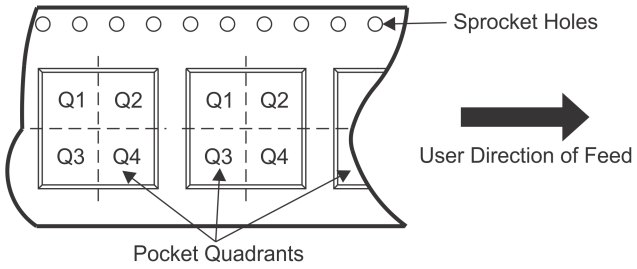


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

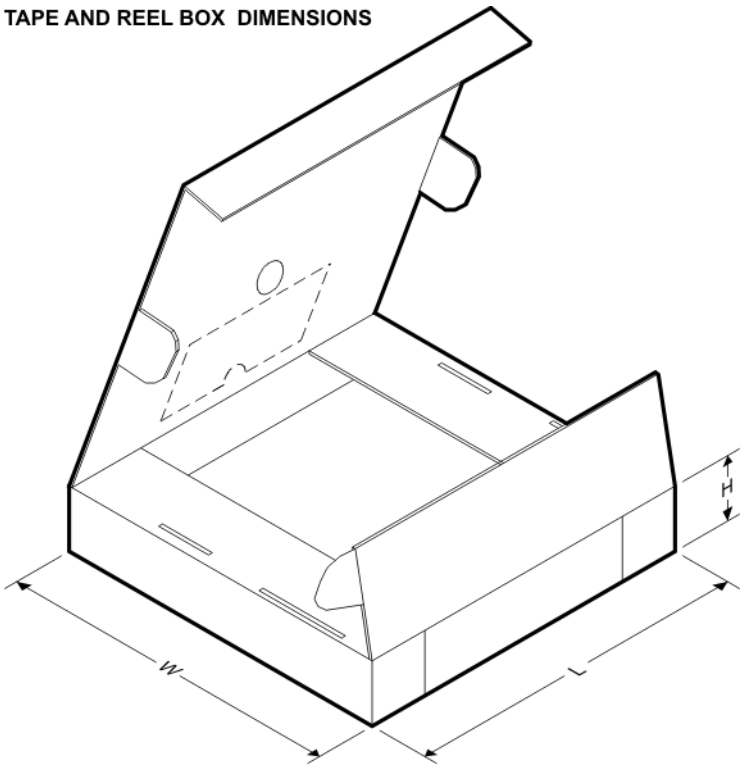
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV10983PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DRV10983ZPWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

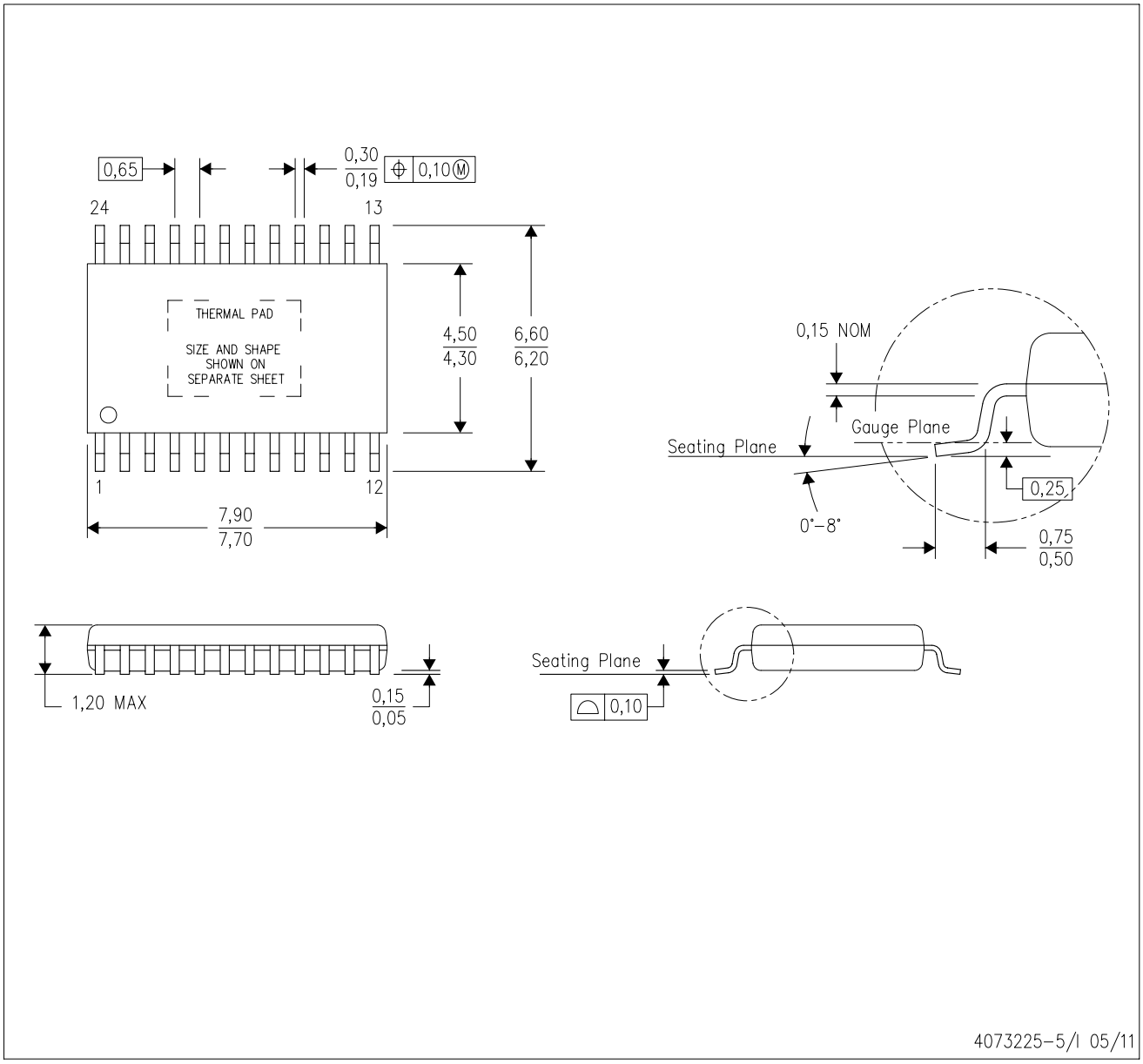
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV10983PWPR	HTSSOP	PWP	24	2000	367.0	367.0	38.0
DRV10983ZPWPR	HTSSOP	PWP	24	2000	367.0	367.0	38.0

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

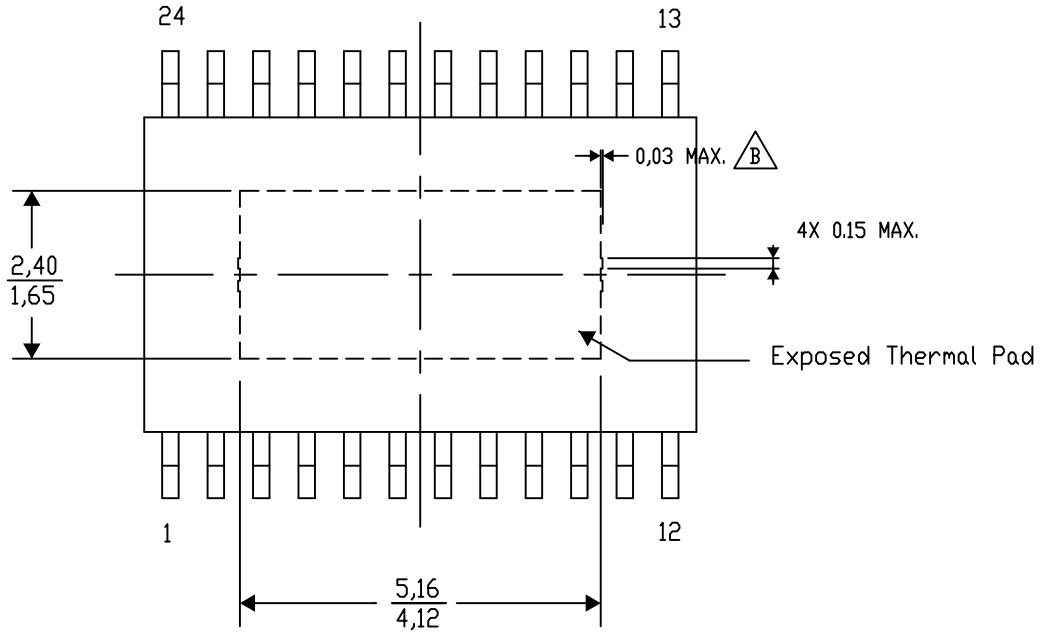
PWP (R–PDSO–G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

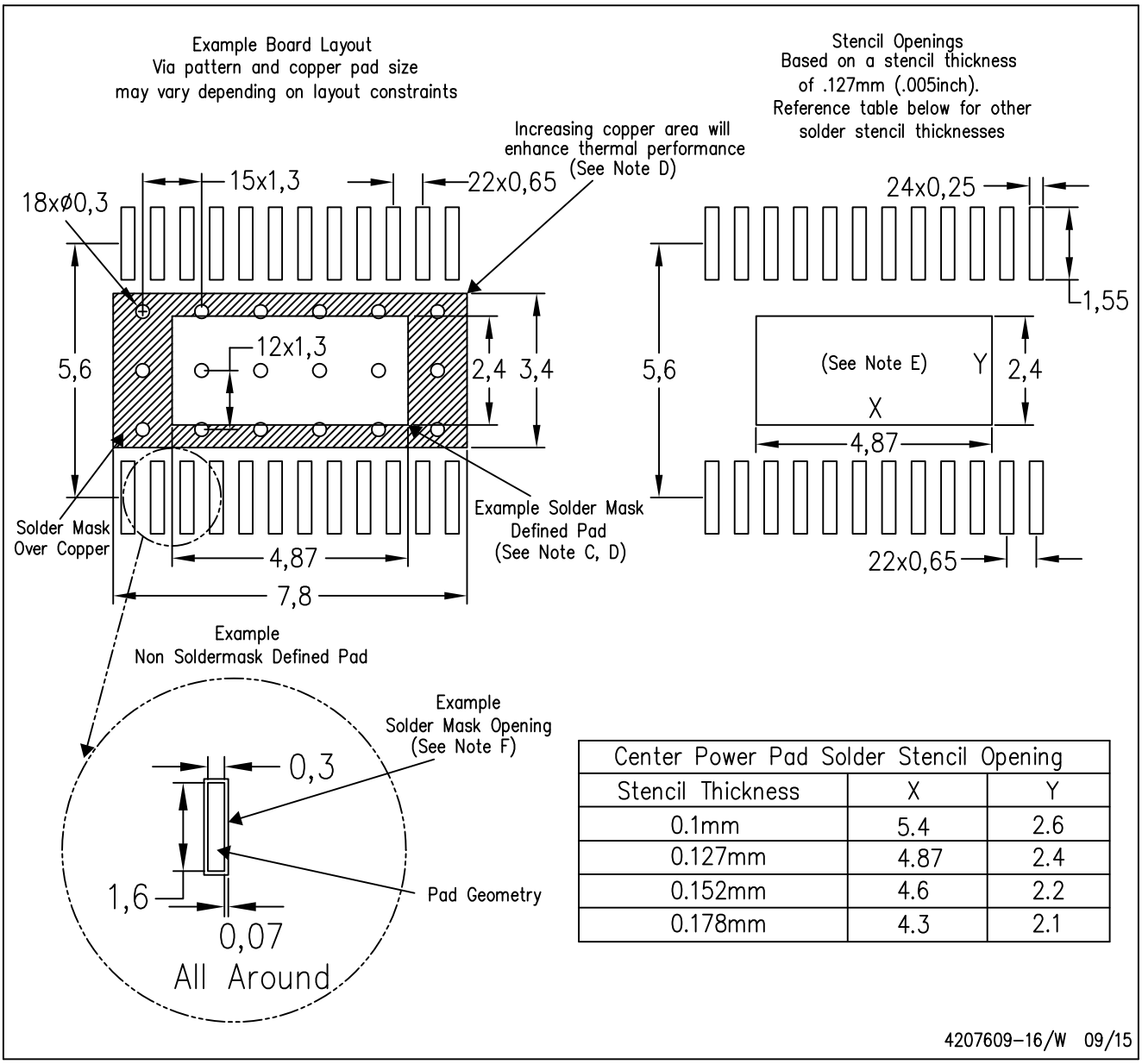
4206332–29/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.4	2.6
0.127mm	4.87	2.4
0.152mm	4.6	2.2
0.178mm	4.3	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

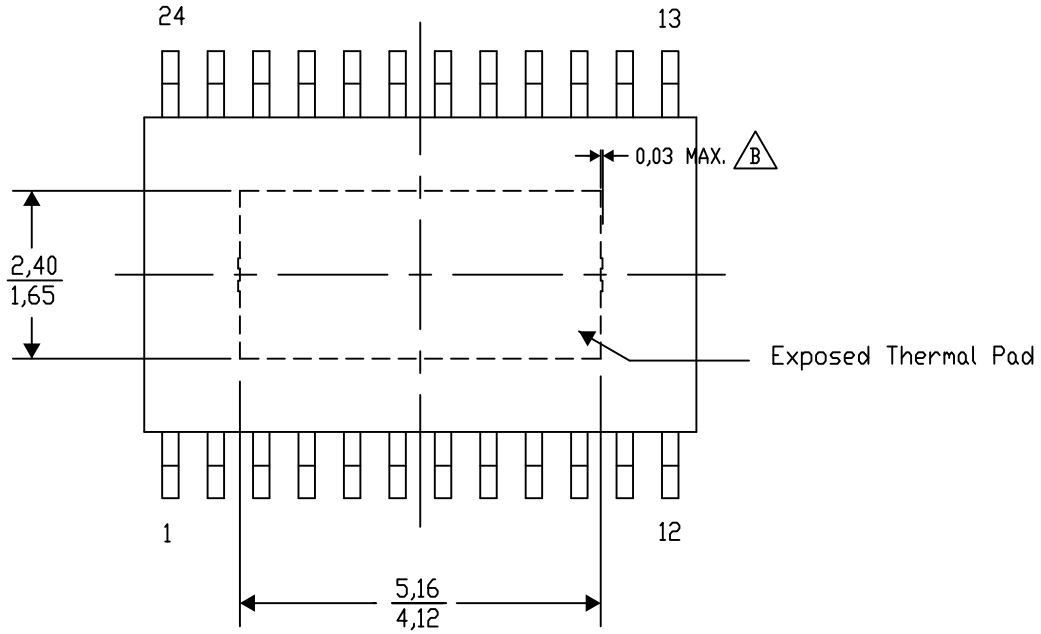
PWP (R–PDSO–G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–54/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

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