

LMZ34202 4.5V 至 42V 输入、2A SIMPLE SWITCHER 电源模块

1 特性

- 完整的集成式电源解决方案可实现小尺寸的薄型设计
- 10mm × 10mm × 4.3mm 封装
- 宽输出电压调节范围 (2.5V 至 7.5V)
- 可调节开关频率 (200kHz 至 1MHz)
- 与外部时钟同步
- 针对轻负载时效率的自动脉冲频率调制 (PFM) 模式
- 可调软启动时间
- 输出电压排序/跟踪
- 电源正常输出
- 可编程欠压锁定 (UVLO)
- 过热热关断保护
- 过流保护 (断续模式)
- 预偏置输出启动
- 工作温度范围: -40°C 至 105°C
- 增强的热性能; 14°C/W
- 符合 EN55022 B 类辐射标准
 - 集成屏蔽式电感

2 应用

- 工业和电机控制
- 自动测试设备
- 医疗和成像设备
- 高密度电源系统

3 说明

LMZ34202 SIMPLE SWITCHER[®]电源模块是一款易于使用的集成式电源，该模块由一个带屏蔽式电感的 2A DC-DC 转换器和无源元件组成，并且采用薄型 QFN 封装。这套整体电源解决方案允许最低只需采用三个外部组件，同时仍能够调整关键参数以满足特定的设计要求。

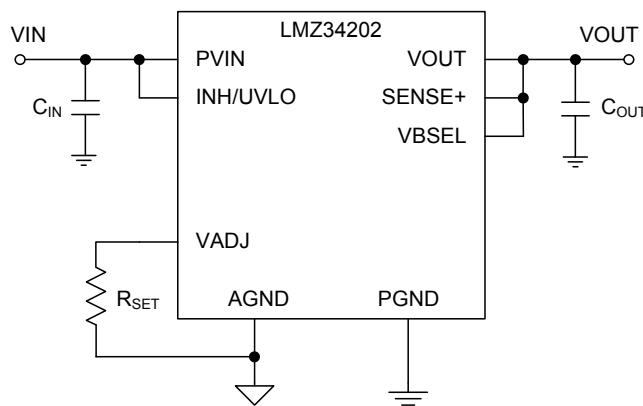
QFN 封装易于焊接到印刷电路板上，允许回流焊曲线最高达 260°C，并且具有出色的功耗特性。LMZ34202 极具灵活性且功能丰富，非常适合为各类器件和系统供电。

器件信息(1)

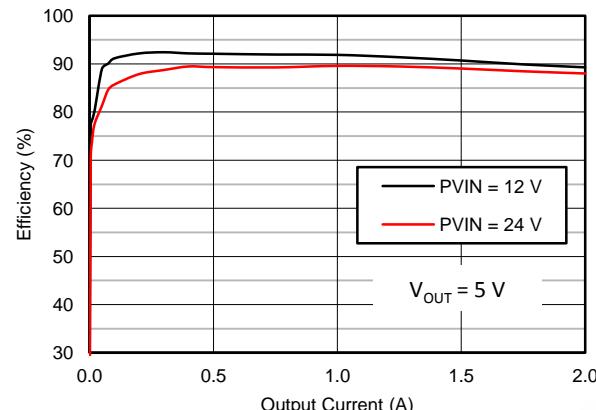
器件型号	封装	封装尺寸
LMZ34202	QFN (43)	10.0mm x 10.0mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

简化应用



效率与输出电流间的关系



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

English Data Sheet: [SNVSAJ2](#)

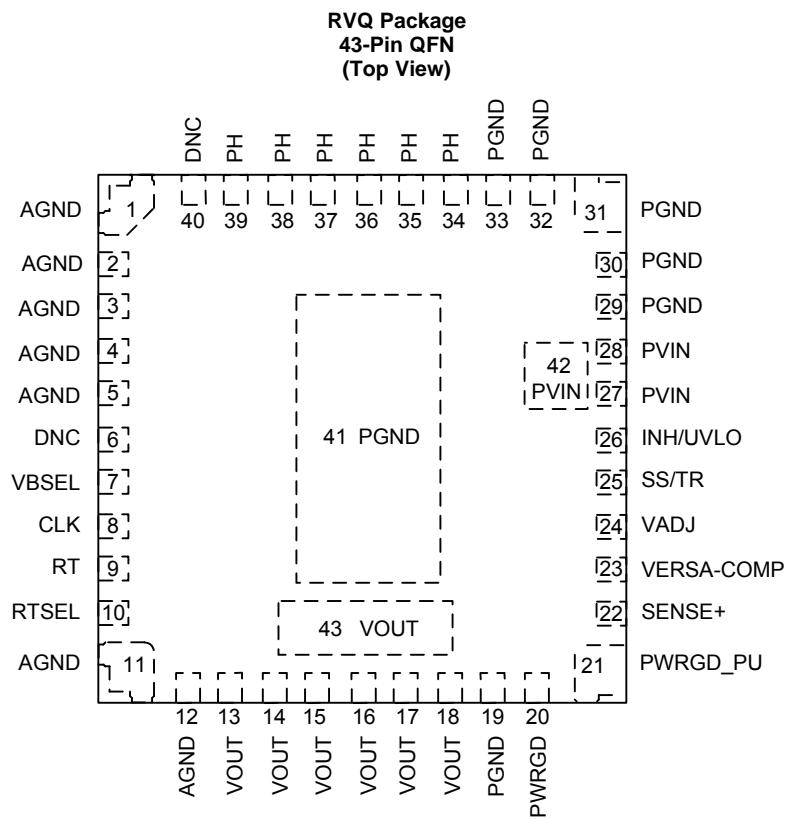
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4 修订历史记录

日期	修订版本	注释
2016 年 3 月	*	首次发布。

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
AGND	1, 2, 3, 4, 5, 11, 12	G	Zero volt reference for the analog control circuitry. All of these pins are not connected together internal to the device and must be connected to one another externally using an analog ground plane on the PCB. Pins 11 and 12 are internally connected to the PGND of the device at a single point. The analog ground plane of the PCB should allow only analog ground currents to flow through these pins.
CLK	8	I	Synchronization input to synchronize the device to an external clock. Connect this pin to AGND if not used.
DNC	6, 40	-	Do Not Connect. Do not connect these pins to AGND, to another DNC pin, or to any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad.
INH/UVLO	26	I	Inhibit and UVLO adjust pin. Use an open drain or open collector device to control the inhibit function. A resistor divider between this pin, AGND, and PVIN adjusts the UVLO voltage. Connect this pin to PVIN if not used.
PGND	19, 29, 30, 31, 32, 33, 41	G	This is the return current path for the power stage of the device. Connect these pins to the input source, the load, and to the bypass capacitors associated with PVIN and VOUT using power ground planes on the PCB. Pad 41 should be connected to the ground planes using multiple vias for good thermal performance.
PH	34, 35, 36, 37, 38, 39	O	Phase switch node. Do not place any external components on these pins or tie them to a pin of another function.
PVIN	27, 28, 42	I	Power input voltage. These pins supply all of the power to the device. Connect these pins to the input source and connect external bypass capacitors between these pins and PGND close to the device.
PWRGD	20	O	Power Good flag pin. This open drain output asserts low if the output voltage is more than approximately $\pm 10\%$ out of regulation. This pin is internally connected to an uncommitted 100k pull-up resistor that can be pulled up to a user-defined voltage applied to the PWRGD_PU pin.

(1) G = Ground, I = Input, O = Output

Pin Functions (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
PWRGD_PU	21	I	An internal 100 k pull-up resistor is connected between this pin and the PWRGD pin. If use of this internal pull-up resistor is desired, connect this pin to an appropriate voltage source that is less than or equal to 12 V. If unused, leave this pin floating.
RT	9	I	This pin is connected to internal frequency setting circuitry which sets the default switching frequency to 500 kHz. An external resistor can be connected from this pin to AGND to adjust the switching frequency. Refer to application section in datasheet.
RTSEL	10	I	This pin can be used to adjust the switching frequency to 1 MHz without the need for an external resistor. Connect this pin to AGND to adjust the frequency to 1 MHz. Otherwise, leave this pin floating.
SENSE+	22	I	Remote sense connection. This pin must be connected to VOUT at the load or at the device pins. Connect the pin to VOUT at the load for improved regulation.
SS/TR	25	I	soft-start and tracking pin. Connecting an external capacitor to this pin adjusts the output voltage soft-start ramp above its 4.1 ms default setting. A voltage applied to this pin allows for tracking and sequencing control.
VADJ	24	I	Connecting a resistor between this pin and AGND adjusts the output voltage.
VBSEL	7	I	Selectable internal bias supply. For output voltages \geq 4.5 V, connect this pin to VOUT. For output voltages $<$ 4.5 V, connect this pin to AGND.
VERSA-COMP	23	I	Connects to internal compensation network. This pin can be left floating or connected to the VADJ pin to select the proper compensation depending on the output voltage.
VOUT	13, 14, 15, 16, 17, 18, 43	O	Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external bypass capacitors between these pins and PGND close to the device.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage	PVIN, INH/UVLO	-0.3	50	V
	VOUT, SENSE+, VBSEL	-0.3	30 ⁽²⁾	V
	VADJ, VERSA-COMP, RT, RTSEL, SS/TR	-0.3	3.6	V
	PWRGD, PWRGD_PU	-0.3	15	V
	CLK	-0.3	5.5	V
Output voltage	PH	-0.3	50	V
Operating junction temperature ⁽³⁾		-40	125	°C
Mechanical shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		1500	G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20-2000Hz		20	G
Storage temperature, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The maximum voltage that can be applied to these pins is 30 V or PVIN, whichever is less.

(3) See temperature derating curves in the Typical Characteristics section for thermal information.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
P _{VIN}	Input voltage	4.5		42	V
V _{OUT}	Output voltage	2.5		7.5	V
f _{SW}	Switching frequency	300		1000	kHz
T _A	Operating ambient temperature	-40		105	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	LMZ34202	UNIT
	RVQ (QFN)	
	43 PINS	
R _{θJA}	14	°C/W
Ψ _{JT}	2.6	°C/W
Ψ _{JB}	9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

Over -40°C to $+105^{\circ}\text{C}$ free-air temperature, $\text{PV}_{\text{IN}} = 24 \text{ V}$, $\text{V}_{\text{OUT}} = 5 \text{ V}$, $\text{I}_{\text{OUT}} = \text{I}_{\text{OUT}} \text{ max}$, $f_{\text{sw}} = 500 \text{ kHz}$, $\text{C}_{\text{IN}1} = 1 \times 10\text{-}\mu\text{F}$, 100-V 1210 ceramic, $\text{C}_{\text{IN}2} = 1 \times 100\text{-}\mu\text{F}$ 100-V electrolytic bulk, and $\text{C}_{\text{OUT}} = 3 \times 47\text{-}\mu\text{F}$, 16-V 1210 ceramic (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (PV_{IN})						
PV_{IN}	Input voltage range	Over I_{OUT} range	4.5 ⁽¹⁾	42	42	V
UVLO	PV_{IN} undervoltage lockout	PV_{IN} increasing		3.2	3.8	V
		PV_{IN} decreasing		2.8		V
OUTPUT VOLTAGE						
V_{OUT} (ADJ)	Output voltage adjust range	Over I_{OUT} range	2.5	7.5	7.5	V
V_{OUT}	Set-point voltage tolerance	$T_A = 25^{\circ}\text{C}$, $\text{I}_{\text{OUT}} = 200 \text{ mA}$		± 0.7	± 1.5 ⁽²⁾	%
	Temperature variation	$-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$, $\text{I}_{\text{OUT}} = 0 \text{ A}$		± 0.9		%
	Line regulation	$T_A = 25^{\circ}\text{C}$, Over PV_{IN} range, $\text{I}_{\text{OUT}} = 300 \text{ mA}$		± 0.1		%
	Load regulation	$T_A = 25^{\circ}\text{C}$, $\text{I}_{\text{OUT}} = 300 \text{ mA}$ to I_{OUT} max		± 0.3		%
	Total output voltage variation	Includes set-point, line, load, and temperature		± 2		%
V_{OUT} ripple	Output voltage ripple	20-MHz Bandwidth		10		mV/pp
OUTPUT CURRENT						
I_{OUT}	Output current	$T_A = 105^{\circ}\text{C}$, natural convection	0	1.5	1.5	A
I_{OUT}	Output current	$T_A = 105^{\circ}\text{C}$, 200LFM	0	2	2	A
I_{OUT}	Output current	$T_A = 95^{\circ}\text{C}$, natural convection	0	2	2	A
I_{LIM}	Overcurrent threshold			2.5		A
PERFORMANCE						
η	Efficiency	$\text{PV}_{\text{IN}} = 12 \text{ V}$ $\text{I}_{\text{OUT}} = 1 \text{ A}$	$\text{V}_{\text{OUT}} = 7.5 \text{ V}$; $f_{\text{sw}} = 400 \text{ kHz}$	95		%
			$\text{V}_{\text{OUT}} = 5 \text{ V}$; $f_{\text{sw}} = 200 \text{ kHz}$	93		%
			$\text{V}_{\text{OUT}} = 5 \text{ V}$; $f_{\text{sw}} = 500 \text{ kHz}$	92		%
			$\text{V}_{\text{OUT}} = 3.3 \text{ V}$; $f_{\text{sw}} = 200 \text{ kHz}$	90		%
			$\text{V}_{\text{OUT}} = 2.5 \text{ V}$; $f_{\text{sw}} = 200 \text{ kHz}$	87		%
		$\text{PV}_{\text{IN}} = 24 \text{ V}$ $\text{I}_{\text{OUT}} = 1 \text{ A}$	$\text{V}_{\text{OUT}} = 7.5 \text{ V}$; $f_{\text{sw}} = 400 \text{ kHz}$	92		%
			$\text{V}_{\text{OUT}} = 5 \text{ V}$; $f_{\text{sw}} = 250 \text{ kHz}$	90		%
			$\text{V}_{\text{OUT}} = 5 \text{ V}$; $f_{\text{sw}} = 500 \text{ kHz}$	88		%
			$\text{V}_{\text{OUT}} = 3.3 \text{ V}$; $f_{\text{sw}} = 250 \text{ kHz}$	86		%
			$\text{V}_{\text{OUT}} = 2.5 \text{ V}$; $f_{\text{sw}} = 250 \text{ kHz}$	81		%
	Transient response	$\text{I}_{\text{OUT}} = 50\%$ load step 1 A/ μs slew rate	Recovery time	100		μs
			Over/Ubershoot	2		%
SLOW START						
T_{SS}	Internal slow start time	SS/TR pin open		4.1		ms
INHIBIT						
V_{INH} (high)	Inhibit control	Precision inhibit level	2.00	2.1	2.42	V
V_{INH} (low)		Inhibit turn-off hysteresis		-0.294		V
I_{I} (shutdown)	Input shutdown supply current	INH/UVLO pin connected to AGND		2.4	6.2 ⁽³⁾	μA
POWER GOOD (PWRGD)						
V_{PWRGD}	PWRGD thresholds	V_{OUT} rising	Good	95		%
			Fault	110		%
		V_{OUT} falling	Fault	90		%
			Good	105		%

(1) The minimum PV_{IN} is 4.5 V or $(\text{V}_{\text{OUT}} / 0.75)$, whichever is greater. For $\text{V}_{\text{OUT}} = 3.3 \text{ V}$, the minimum PV_{IN} is 4.75 V when $\text{I}_{\text{OUT}} > 1.5 \text{ A}$.

(2) The stated limit of the set-point voltage tolerance includes the tolerance of both the internal voltage reference and the internal adjustment resistor. The overall output voltage tolerance will be affected by the tolerance of the external R_{SET} resistor.

(3) Guaranteed by design. Not production tested.

Electrical Characteristics (continued)

Over -40°C to $+105^{\circ}\text{C}$ free-air temperature, $\text{PV}_{\text{IN}} = 24 \text{ V}$, $\text{V}_{\text{OUT}} = 5 \text{ V}$, $\text{I}_{\text{OUT}} = \text{I}_{\text{OUT}} \text{ max}$, $f_{\text{sw}} = 500 \text{ kHz}$, $\text{C}_{\text{IN}1} = 1 \times 10\text{-}\mu\text{F}$, 100-V 1210 ceramic, $\text{C}_{\text{IN}2} = 1 \times 100\text{-}\mu\text{F}$ 100-V electrolytic bulk, and $\text{C}_{\text{OUT}} = 3 \times 47\text{-}\mu\text{F}$, 16-V 1210 ceramic (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN						
$\text{T}_{\text{SHUTDOWN}}$	Thermal shutdown	Shutdown Temperature		160		$^{\circ}\text{C}$
		Hysteresis		10		$^{\circ}\text{C}$
INPUT/OUTPUT CAPACITANCE						
C_{IN}	External input capacitance	ceramic		$10^{(4)}$		μF
		non-ceramic		100		μF
C_{OUT}	External output capacitance	Ceramic		$64^{(5)}$	See ⁽⁶⁾	μF
		Non-ceramic		100	See ⁽⁶⁾	μF
		ceramic + non-ceramic			See ⁽⁶⁾	μF
		Equivalent series resistance (ESR)			20	$\text{m}\Omega$

- (4) The specified minimum ceramic input capacitance represents the standard capacitance value. The actual effective capacitance after considering the effects of DC bias and temperature variation should be $\geq 4.7 \mu\text{F}$.
- (5) The amount of required output capacitance varies depending on the output voltage (see [Output Capacitor Selection](#)). The minimum required output capacitance must be comprised of ceramic capacitance. The amount of required ceramic capacitance represents the standard capacitance value. Locate the capacitance close to the device. Adding additional ceramic or non-ceramic capacitance close to the load improves the response of the regulator to load transients.
- (6) The maximum allowable output capacitance varies depending on the output voltage (see [Output Capacitor Selection](#)).

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{sw}	Switching frequency	RT and RTSEL pins open	410	500	590	kHz
f_{CLK}	CLK Control	Synchronization frequency	200		1000	kHz
$V_{\text{CLK-H}}$		CLK high level	2		5.5	V
$V_{\text{CLK-L}}$		CLK low level			0.4	V
D_{CLK}		CLK duty cycle	10%	50%	90%	

6.7 Typical Characteristics

$T_A = 25^\circ\text{C}$, unless otherwise noted.

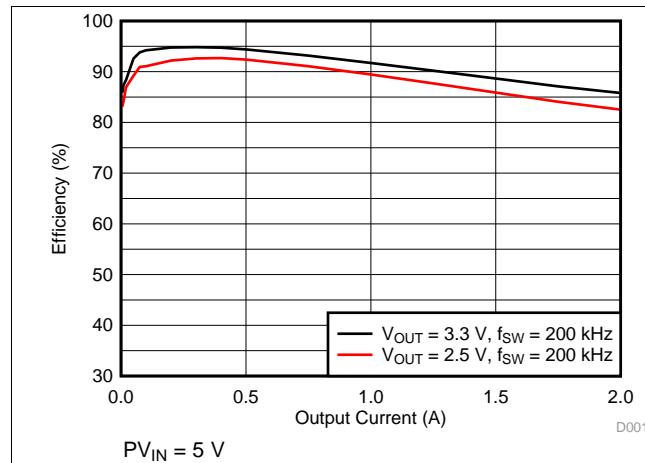


图 1. Efficiency vs Output Current

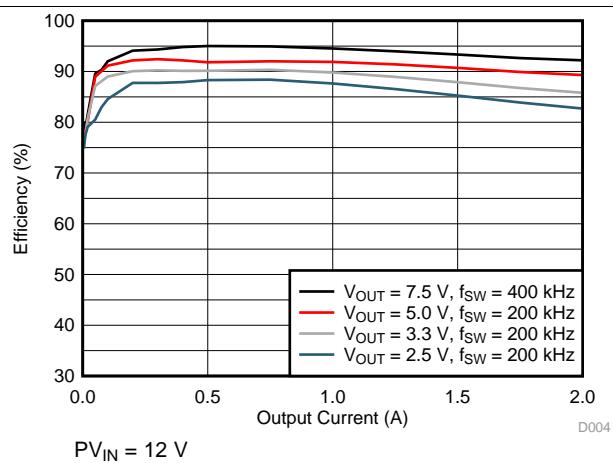


图 2. Efficiency vs Output Current

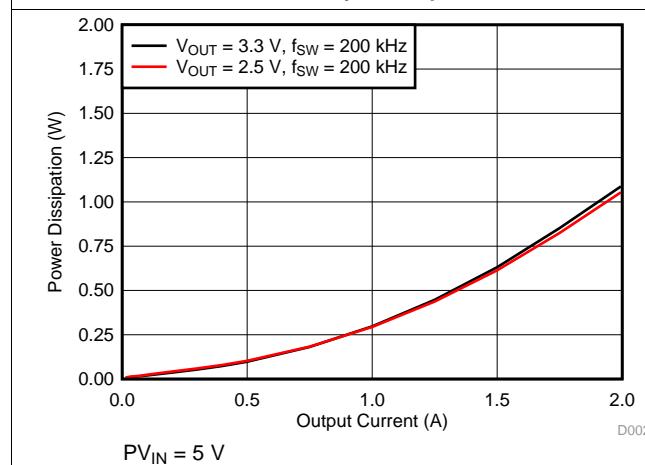


图 3. Power Dissipation vs Output Current

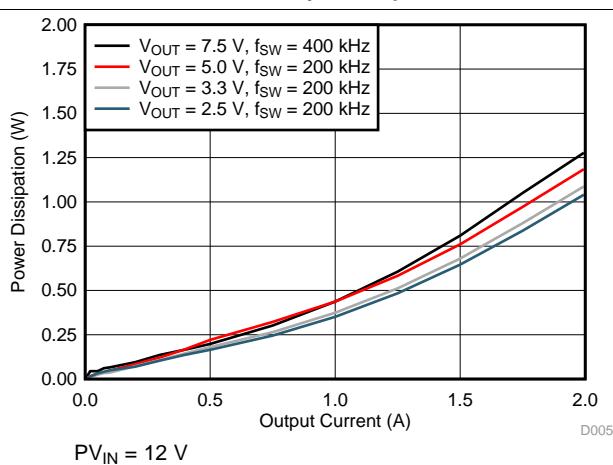


图 4. Power Dissipation vs Output Current

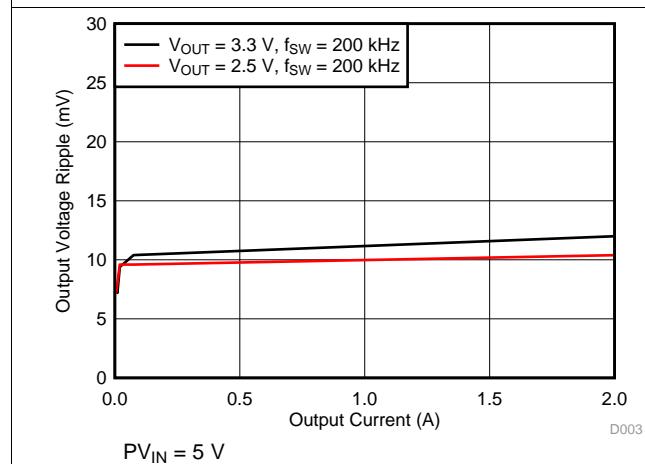


图 5. Voltage Ripple vs Output Current

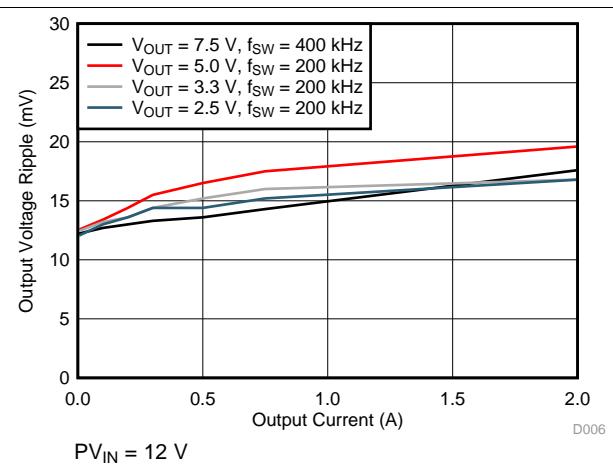


图 6. Voltage Ripple vs Output Current

Typical Characteristics (接下页)

$T_A = 25^\circ\text{C}$, unless otherwise noted.

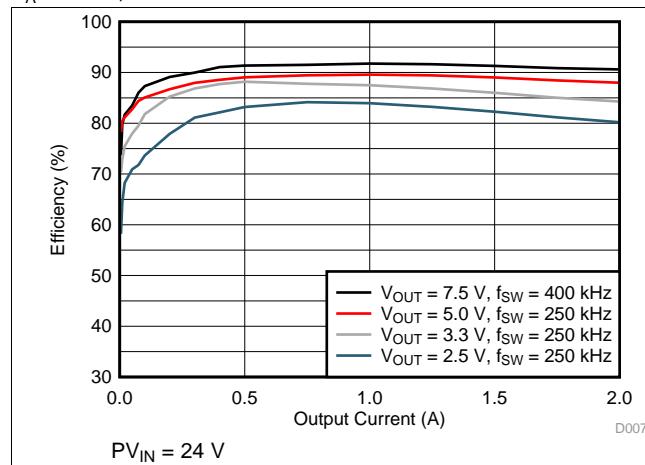


图 7. Efficiency vs Output Current

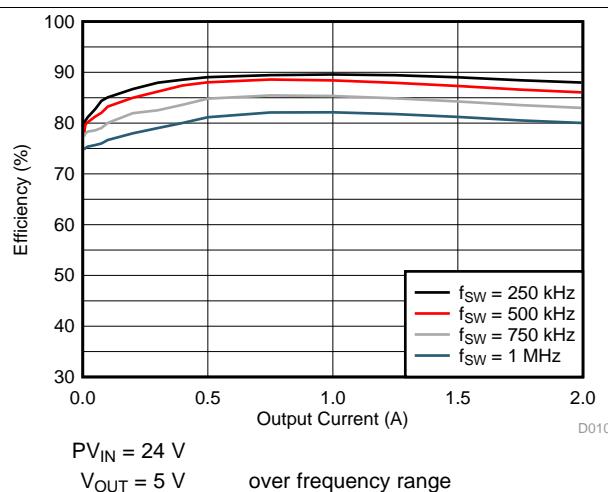


图 8. Efficiency vs Output Current

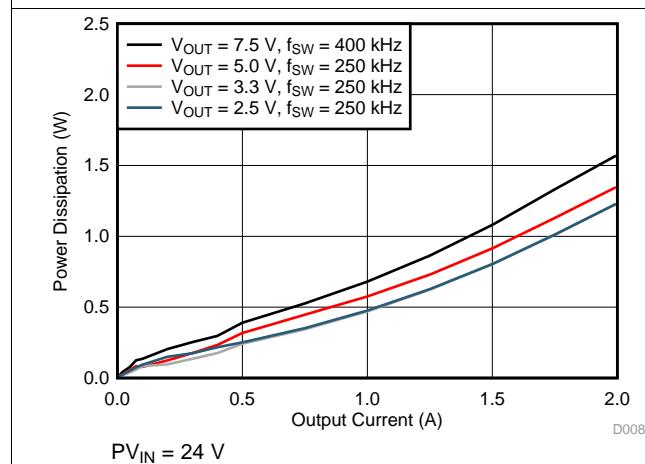


图 9. Power Dissipation vs Output Current

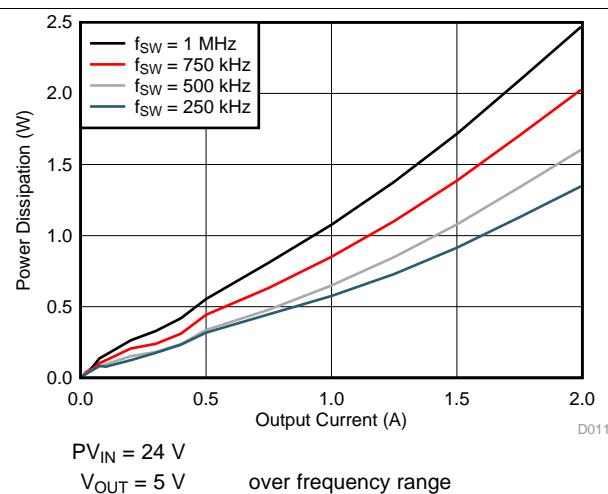


图 10. Power Dissipation vs Output Current

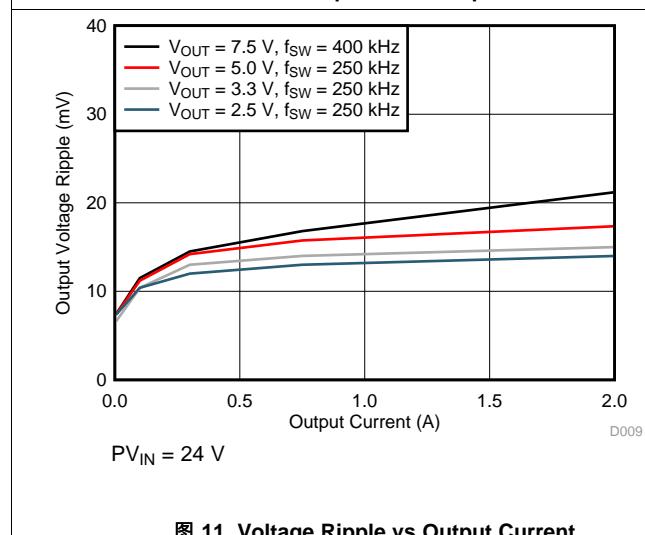


图 11. Voltage Ripple vs Output Current

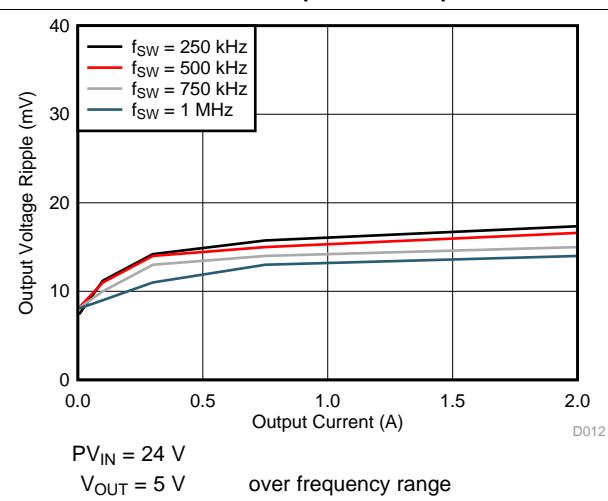


图 12. Voltage Ripple vs Output Current

Typical Characteristics (接下页)

$T_A = 25^\circ\text{C}$, unless otherwise noted.

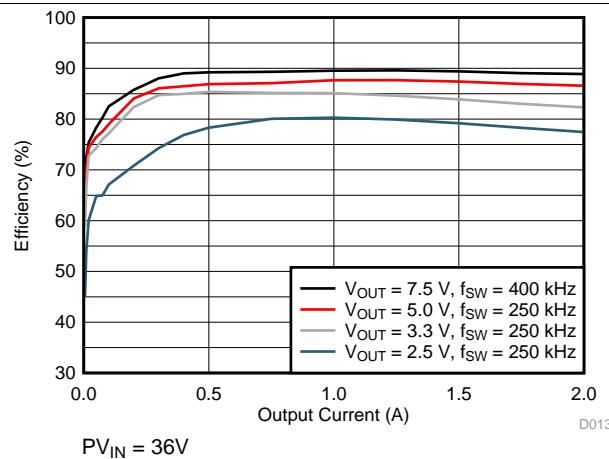


图 13. Efficiency vs Output Current

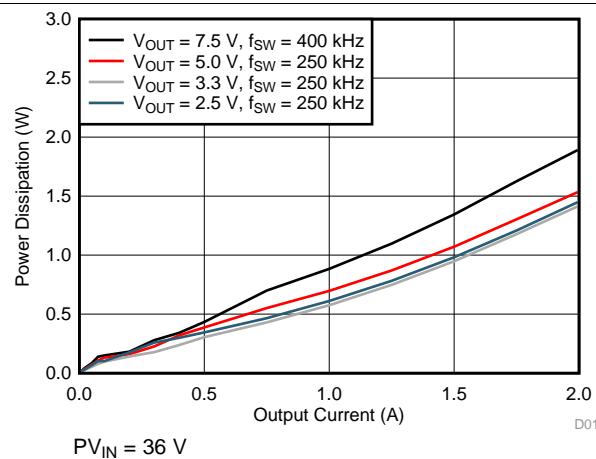


图 14. Power Dissipation vs Output Current

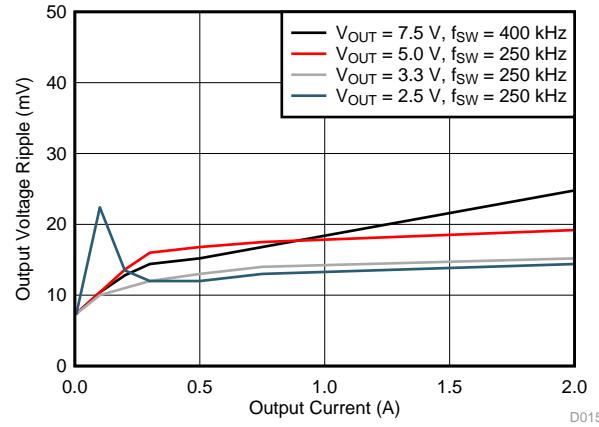


图 15. Voltage Ripple vs Output Current

6.8 Typical Characteristics (Thermal Derating)

The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 50 mm × 100 mm, 4-layer PCB with 2 oz. copper.

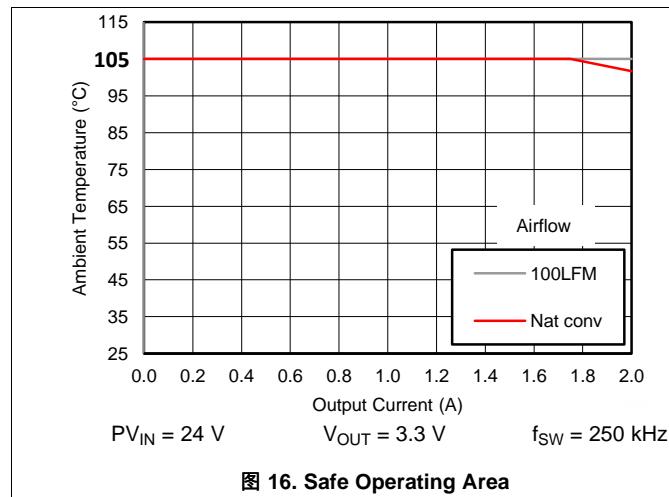


图 16. Safe Operating Area

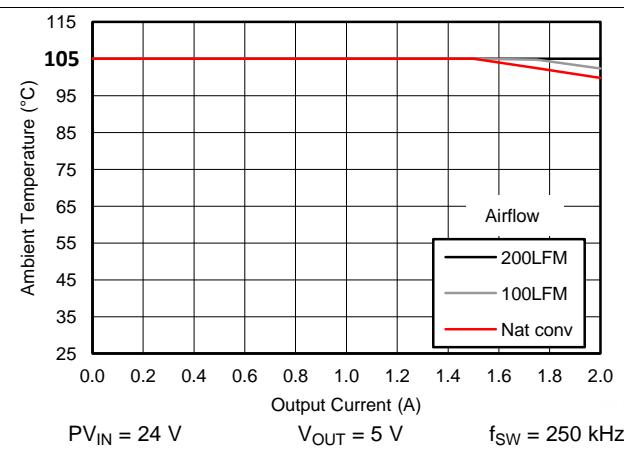


图 17. Safe Operating Area

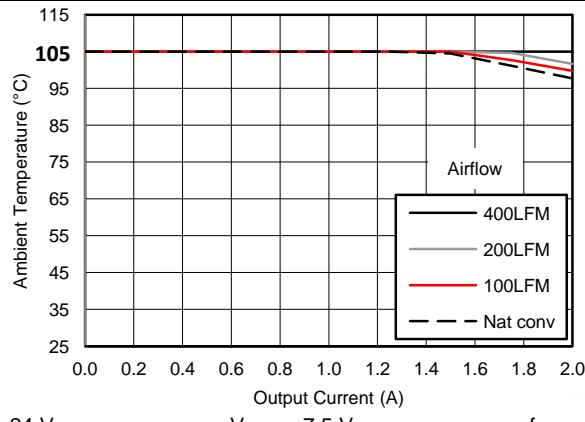


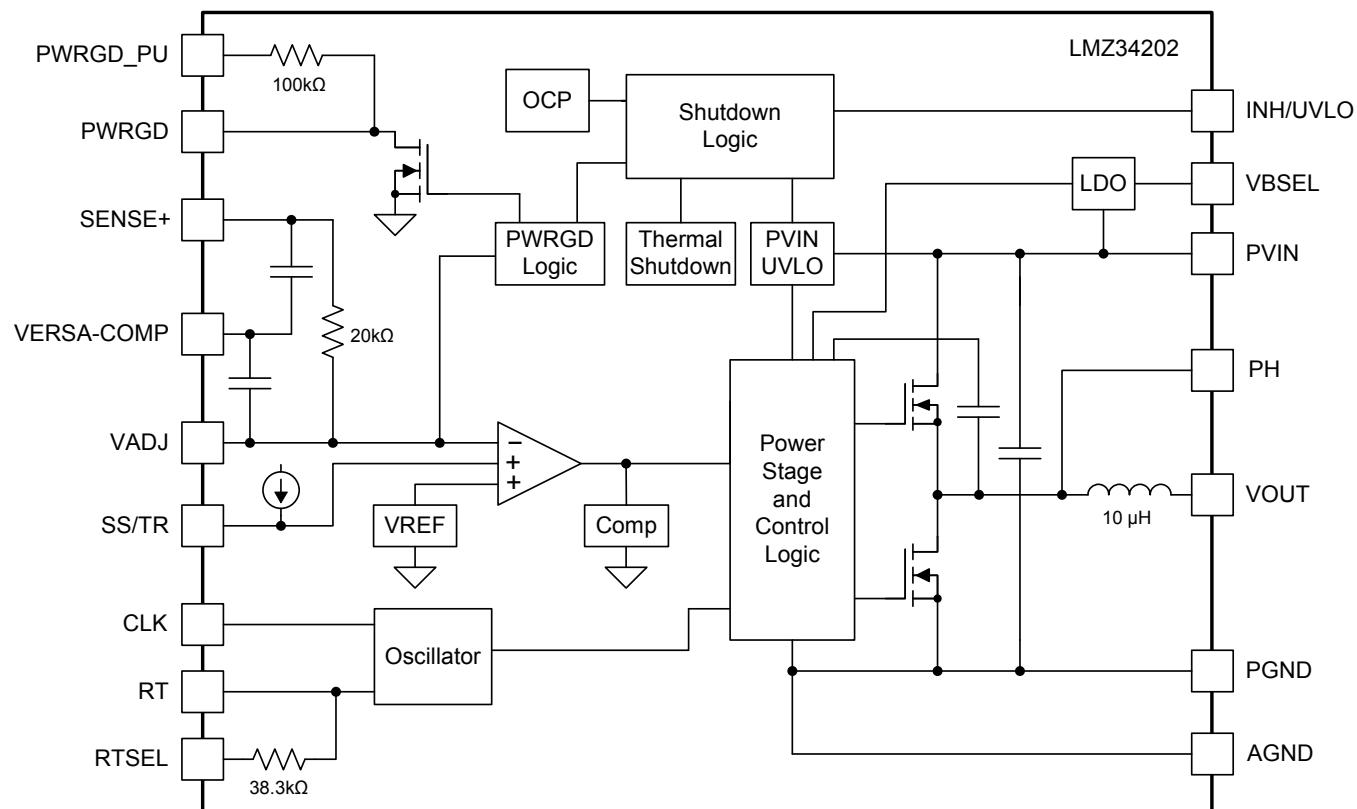
图 18. Safe Operating Area

7 Detailed Description

7.1 Overview

The LMZ34202 is a full featured 42-V input, 2-A, synchronous step down converter with PWM, MOSFETs, inductor, and control circuitry integrated into a low-profile, overmolded package. This device enables small designs by integrating all but the input and output capacitors, while still leaving the ability to adjust key parameters to meet specific design requirements. The LMZ34202 provides a 3x output voltage range of 2.5 V to 7.5 V. A single external resistor is used to adjust the output voltage to the desired output. The switching frequency is also adjustable by using an external resistor or a synchronization pulse to accommodate various input and output voltage conditions and to optimize efficiency. The device provides accurate voltage regulation for a variety of loads by using an internal voltage reference that is 2% accurate over temperature. Input undervoltage lockout is internally set at 3.2 V, but can be adjusted upward using a resistor divider on the INH/UVLO pin of the device. The INH/UVLO pin can also be pulled low to put the device in standby mode to reduce input quiescent current. The device provides a power good signal to indicate when the output is within $\pm 5\%$ of its nominal voltage. Thermal shutdown and current limit features protect the device during an overload condition. Automatic PFM mode improves light-load efficiency. A 43-pin, QFN, package that includes exposed bottom pads provides a thermally enhanced solution for space-constrained applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adjusting the Output Voltage

The VADJ pin sets the output voltage of the LMZ34202. The output voltage adjustment range is from 2.5 V to 7.5 V. The switching frequency range for any output voltage must be determined from 表 4 or 表 5. The adjustment method requires the addition of R_{SET} , which sets the output voltage, and the connection of SENSE+ to VOUT. The R_{SET} resistor must be connected directly between the VADJ (pin 24) and AGND. The SENSE+ pin (pin 22) must be connected to VOUT either at the load for improved regulation or at VOUT of the device. 表 1 lists the standard external R_{SET} resistor for a number of common bus voltages.

表 1. Standard R_{SET} Resistor Values for Common Output Voltages

	OUTPUT VOLTAGE V_{OUT} (V)				
	2.5	3.3	5.0	6.0	7.5
R_{SET} (kΩ)	13.7	8.87	5.11	4.02	3.09

For other output voltages, the value of the required resistor can either be calculated using the following formula, or simply selected from the range of values given in 表 2.

$$R_{SET} = \frac{20}{\left(\frac{V_{OUT}}{1.011}\right) - 1} \text{ (kΩ)} \quad (1)$$

表 2. Standard R_{SET} Resistor Values

V_{OUT} (V)	R_{SET} (kΩ)	V_{OUT} (V)	R_{SET} (kΩ)
2.5	13.7	5.1	4.99
2.6	12.7	5.2	4.87
2.7	11.8	5.3	4.75
2.8	11.3	5.4	4.64
2.9	10.7	5.5	4.53
3.0	10.2	5.6	4.42
3.1	9.76	5.7	4.32
3.2	9.31	5.8	4.22
3.3	8.87	5.9	4.12
3.4	8.45	6.0	4.02
3.5	8.06	6.1	3.97
3.6	7.87	6.2	3.92
3.7	7.50	6.3	3.83
3.8	7.32	6.4	3.74
3.9	6.98	6.5	3.65
4.0	6.81	6.6	3.61
4.1	6.49	6.7	3.57
4.2	6.34	6.8	3.48
4.3	6.19	6.9	3.40
4.4	5.90	7.0	3.36
4.5	5.76	7.1	3.32
4.6	5.62	7.2	3.24
4.7	5.49	7.3	3.20
4.8	5.36	7.4	3.16
4.9	5.23	7.5	3.09
5.0	5.11		

7.3.2 Switching Frequency (RT)

The switching frequency range of the LMZ34202 is 200 kHz to 1 MHz. Not all V_{IN} , V_{OUT} , and I_{OUT} conditions can be set to all of the frequencies in this range. See [Recommended Operating Range](#) for the allowable operating ranges. The switching frequency can easily be set one of three ways. First, leaving the RT pin (pin 9) and RTSEL pin (pin 10) floating (OPEN) allows operation at the default switching frequency of 500 kHz. Also, connecting the RTSEL pin to AGND while floating the RT pin, sets the switching frequency to 1 MHz. The option is also available to set the switching frequency to any frequency in the range of 200 kHz to 1 MHz, by connecting a resistor (R_{RT}) between the RT pin and AGND, while floating the RTSEL pin. See [表 3](#) for standard resistor values for setting the switching frequency or use [公式 2](#) to calculate R_{RT} for other switching frequencies.

表 3. Switching Frequency R_{RT} Values

Switching Frequency	R_{RT} (k Ω)
250 kHz	158
500 kHz	78.7 or (RT pin OPEN, RTSEL pin OPEN)
750 kHz	53.6
1 MHz	38.3 or (RT pin OPEN, RTSEL pin to AGND)

$$R_{RT} = \frac{40200}{F_{sw}(\text{kHz})} - 0.6 \quad (\text{k}\Omega) \quad (2)$$

7.3.3 Recommended Operating Range

[表 4](#) and [表 5](#) below show the allowable switching frequencies for a given range of output voltages. Reference [表 4](#) for applications where the maximum output current is 1.75 A or less. Reference [表 5](#) for applications that the output current is greater than 1.75 A. Notice that applications requiring less than 1.75 A can operate over a much wider range of switching frequencies. For the most efficient solution, always operate at the lowest allowable frequency.

**表 4. Switching Frequency vs Output Voltage
Output Current ≤ 1.75 A**

V_{OUT} RANGE (V)	SWITCHING FREQUENCY RANGE (kHz)					
	PVIN = 12 V		PVIN = 24 V		PVIN = 36 V	
	MIN	MAX	MIN	MAX	MIN	MAX
2.5 - 3.5 V	200	1000	200	600	200	400
>3.5 - 4.5 V	200	1000	200	850	200	550
>4.5 - 5.5 V	200	1000	200	1000	200	750
>5.5 - 6.5 V	300	1000	200	1000	200	1000
>6.5 - 7.5 V	300	900	300	1000	300	950

**表 5. Switching Frequency vs Output Voltage
Output Current > 1.75 A**

V_{OUT} RANGE (V)	SWITCHING FREQUENCY RANGE (kHz)					
	PVIN = 12 V		PVIN = 24 V		PVIN = 36 V	
	MIN	MAX	MIN	MAX	MIN	MAX
2.5 - 3.5 V	200	450	200	500	200	400
>3.5 - 4.5 V	200	500	200	600	200	550
>4.5 - 5.5 V	200	500	200	650	200	700
>5.5 - 6.5 V	300	500	250	700	250	800
>6.5 - 7.5 V	300	400	300	750	300	800

7.3.4 Synchronization (CLK)

The LMZ34202 switching frequency can also be synchronized to an external clock from 200 kHz to 1 MHz. Not all $P_{V_{IN}}$, V_{OUT} , and I_{OUT} conditions can be set to all of the frequencies in this range. See [Recommended Operating Range](#) for the allowable operating ranges.

To implement the synchronization feature, connect a clock signal to the CLK pin with a duty cycle between 10% and 90%. The clock signal amplitude must transition lower than 0.4 V and higher than 2.0 V. The start of the switching cycle is synchronized to the rising edge of CLK pin. Before the external clock is present the device operates in RT mode and the switching frequency is set by R_{RT} resistor. Select R_{RT} to set the frequency close to the external synchronization frequency. When the external clock is present, the CLK mode overrides the RT mode. If the external clock is removed or fails at logic high or low, the LMZ34202 will switch at the frequency programmed by the R_{RT} resistor after a time-out period. Connect the CLK pin (pin 8) to AGND if not used.

7.3.5 Output Capacitor Selection

The minimum required and maximum output capacitance of the LMZ34202 is a function of the output voltage as shown in [表 6](#). Additionally, the output voltage will determine the Versa-Comp configuration (see [VERSA-COMP Pin Configurations](#)), which is also included in [表 6](#). The capacitance values listed in [表 6](#) are the specified capacitance values. The effects of DC bias and temperature variation must be considered when using ceramic capacitance. For ceramic capacitors, package size, voltage rating, and dielectric material will contribute to differences between the specified value and the actual effective value of the capacitance. $C_{OUT(min)}$ must be comprised of ceramic type capacitors. Additional capacitance, not exceeding $C_{OUT(max)}$, may be ceramic type or low-ESR polymer type. See [表 7](#) for a preferred list of output capacitors by vendor.

表 6. Required Output Capacitance

V_{OUT} (V)	MINIMUM REQUIRED C_{OUT} (μ F) ⁽¹⁾ ⁽²⁾	MAXIMUM C_{OUT} (μ F) ⁽²⁾	Versa-Comp Connection
2.5	64	350	Leave OPEN
3.3	64	350	Connect to VADJ
5.0	64	350	Connect to VADJ
6.0	64	200	Connect to VADJ
7.5	100	200	Connect to VADJ

(1) Minimum required output capacitance must be comprised of ceramic capacitance.

(2) C_{OUT} values represent specified capacitance values.

表 7. Recommended Output Capacitors⁽¹⁾

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE ⁽²⁾ (μ F)	ESR ⁽³⁾ (m Ω)
TDK	X5R	C3225X5R1C106K	16	10	2
Murata	X5R	GRM32ER61C106K	16	10	2
TDK	X5R	C3225X5R1C226M	16	22	2
Murata	X5R	GRM32ER61C226K	16	22	2
TDK	X5R	C3225X5R1A476M	10	47	2
Murata	X5R	GRM32ER61C476K	16	47	3
TDK	X5R	C3225X5R0J107M	6.3	100	2
Murata	X5R	GRM32ER60J107M	6.3	100	2
Murata	X5R	GRM32ER61A107M	10	100	2
Kemet	X5R	C1210C107M4PAC7800	16	100	2
Panasonic	POSCAP	6TPE100MI	6.3	100	18
Panasonic	POSCAP	6TPF220M9L	6.3	220	9
Panasonic	POSCAP	6TPE220ML	6.3	220	12

(1) Capacitor Supplier Verification, RoHS, Lead-free and Material Details

Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.

(2) Specified capacitance values.

(3) Maximum ESR @ 100kHz, 25°C.

7.3.6 VERSA-COMP Pin Configurations

The versa-comp feature of the LMZ34202 allows a simple method to adjust the internal compensation network to provide the optimized phase and gain margin based on the output voltage. This easy-to-use feature requires no external components and is implemented by the simple configuration of two adjacent pins on the module.

The versa-comp feature must be configured in one of two ways; VERSA-COMP pin left OPEN or VERSA-COMP pin tied to VADJ. The output voltage determines the appropriate Versa-Comp pin configuration. [表 8](#) lists the Versa-Comp configuration. [图 19](#) shows the two possible Versa-Comp pin configurations.

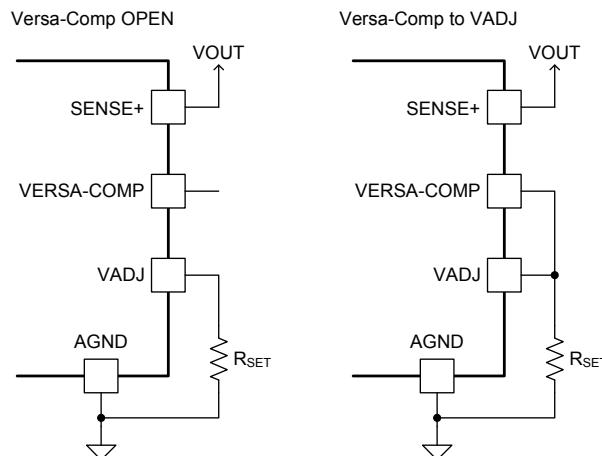


图 19. Versa-Comp Configurations

表 8. VERSA-COMP Pin Configurations

V _{OUT} RANGE (V)		VERSACOMP PIN CONFIGURATION
MIN	MAX	
2.5	< 3.0	OPEN
3.0	7.5	Connect to VADJ

7.3.7 Input Capacitor Selection

The LMZ34202 requires a ceramic capacitor with a minimum effective input capacitance of 4.7 μ F. Use only high-quality ceramic type X5R or X7R capacitors with sufficient voltage rating. An additional 100 μ F of non-ceramic capacitance is recommended for applications with transient load requirements. The voltage rating of input capacitors must be greater than the maximum input voltage. To compensate the derating of ceramic capacitors, a voltage rating of twice the maximum input voltage is recommended. At worst case, when operating at 50% duty cycle and maximum load, the combined ripple current rating of the input capacitors must be at least 1.0 Arms. [表 9](#) includes a preferred list of capacitors by vendor.

表 9. Recommended Input Capacitors⁽¹⁾

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE ⁽²⁾ (μ F)	ESR ⁽³⁾ (m Ω)
TDK	X5R	C3225X5R1H106K	50	10	3
Murata	X7R	GRM32ER71H106K	50	10	2
Murata	X7R	GRM32ER71J106K	63	10	2
Panasonic	ZA	EEHZA1H101P	50	100	28
Panasonic	ZA	EEHZA1J560P	63	56	30

(1) **Capacitor Supplier Verification, RoHS, Lead-free and Material Details**

Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.

(2) Specified capacitance values

(3) Maximum ESR @ 100kHz, 25°C.

7.3.8 Output On/Off Inhibit (INH/UVLO)

The INH/UVLO pin provides on and off control of the device. The INH input provides a precise 2.1 V rising threshold to allow direct logic drive or connection to a voltage divider from a higher voltage source such as PV_{IN}. Once the INH/UVLO pin voltage exceeds the threshold voltage, the device starts operation. The INH input also incorporates 300 mV (typ) of hysteresis resulting in a falling threshold of 1.8 V. If the INH/UVLO pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state. The INH/UVLO pin cannot be open circuit or floating. The simplest way to enable the operation of the LMZ34202 is to connect the INH/UVLO pin to PVIN pin directly as shown in [图 20](#). This connection allows the LMZ34202 device to restart when PV_{IN} is again within the operation range.

If an application requires controlling the INH/UVLO pin, either drive it directly with a logic input or use an open drain and collector device to interface with the pin and place a 100-k Ω resistor between this pin and PVIN pin as shown in [图 21](#). When turning Q1 on applies a low voltage to the inhibit control (INH/UVLO) pin and disables the output of the supply, shown in [图 22](#). If Q1 is turned off, the supply executes a soft-start power-up sequence, as shown in [图 23](#).

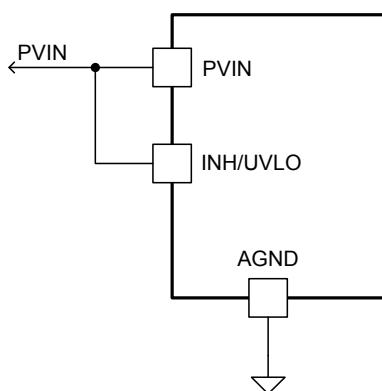


图 20. Enabling the Device

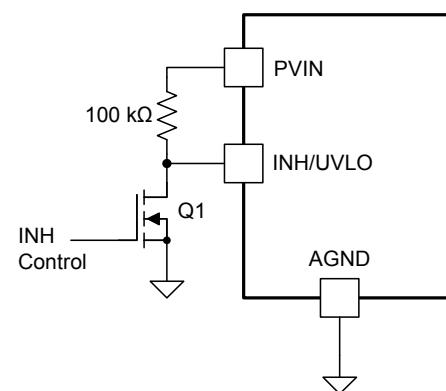


图 21. Typical Inhibit Control

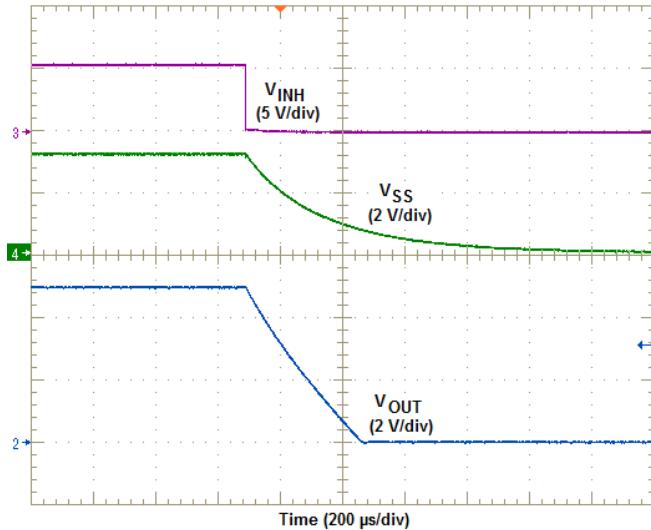


图 22. Inhibit Turn-Off

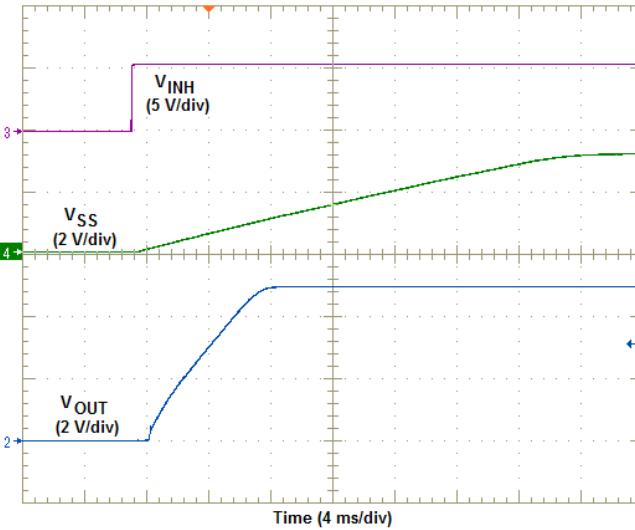


图 23. Inhibit Turn-On

7.3.9 Under Voltage Lockout (UVLO)

The LMZ34202 device has an internal UVLO circuit which prevents the device from operating until the $P_{V_{IN}}$ voltage exceeds the UVLO threshold, (3.2 V (typ)). The device will begin switching and the output voltage will begin to rise once $P_{V_{IN}}$ exceeds the threshold, however $P_{V_{IN}}$ must be greater than $(V_{OUT}/0.75)$ in order to for V_{OUT} to regulate at the set-point voltage.

Applications may require a higher UVLO threshold to prevent early turn-on, for sequencing requirements, or to prevent input current draw at lower input voltages. An external resistor divider can be added to the INH/UVLO pin to adjust the UVLO threshold higher. The external resistor divider can be configured as shown in [图 24. 表 10](#) lists standard values for R_{UVLO1} and R_{UVLO2} to adjust the UVLO voltage higher.

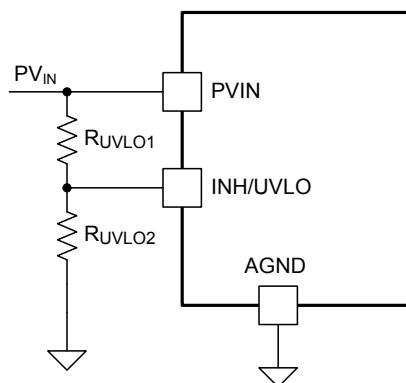


图 24. Adjustable PVIN UVLO

表 10. Resistor Values for Adjusting PVIN UVLO

PVIN UVLO (V)	4.5	10	15	20	25	30
R_{UVLO1} (kΩ)	100	100	100	100	100	100
R_{UVLO2} (kΩ)	46.4	21.0	14.0	10.5	8.45	6.98

7.3.10 Remote Sense

The SENSE+ pin must be connected to V_{OUT} at the load, or at the device pins.

Connecting the SENSE+ pin to V_{OUT} at the load improves the load regulation performance of the device by allowing it to compensate for any I-R voltage drop between its output pins and the load. An I-R drop is caused by the high output current flowing through the small amount of pin and trace resistance. This should be limited to a maximum of 300 mV.

注

The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the SENSE+ connection, they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

7.3.11 VBSEL

The VBSEL pin allows the user to select the input source of the internal bias circuitry to improve efficiency. For output voltages ≥ 4.5 V, connect this pin to V_{OUT} . For output voltages < 4.5 V, connect this pin to AGND.

7.3.12 Soft-Start (SS/TR)

Leaving SS/TR pin open enables the internal slow start time interval of approximately 4.1 ms. Adding additional capacitance between the SS pin and AGND increases the slow start time. Increasing the slow start time will reduce inrush current seen by the input source and reduce the current seen by the device when charging the output capacitors. To avoid the activation of current limit and ensure proper start-up, the SS capacitor may need to be increased when operating near the maximum output capacitance limit.

See 表 11 below for SS capacitor values and timing interval.

表 11. Soft-Start Capacitor Values and Soft-Start Time

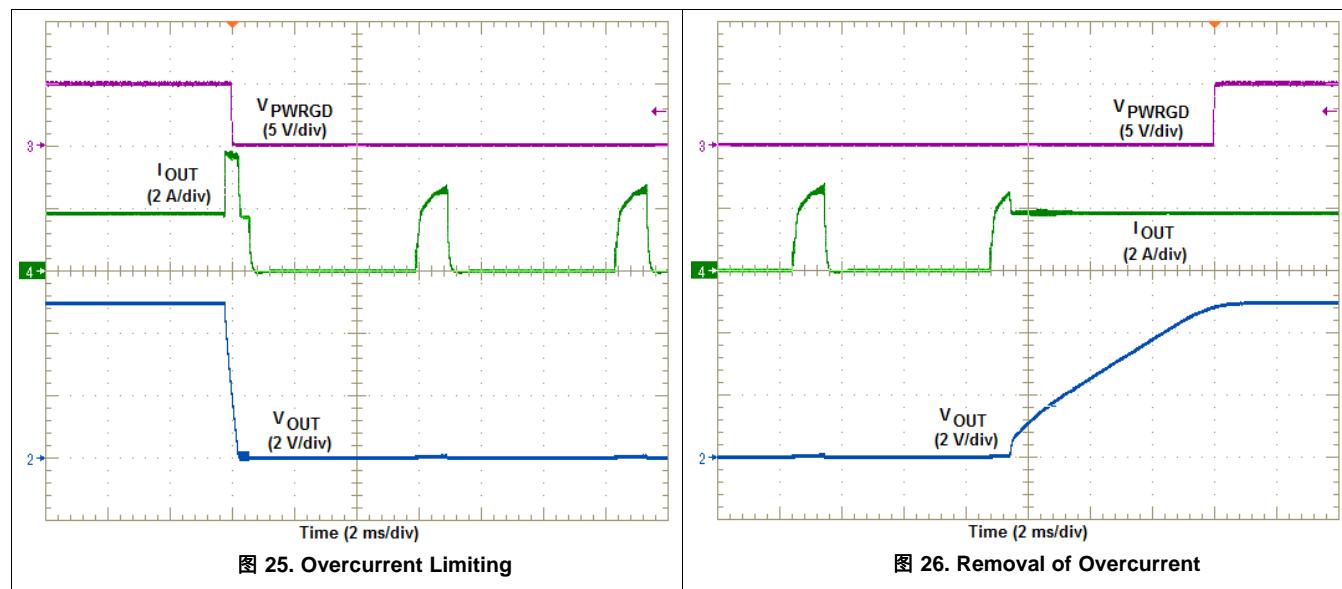
C_{SS} (nF)	open	15	22	33	47
SS Time (ms)	4.1	7	10	15	20

7.3.13 Power Good (PWRGD) and Pull-up (PWRGD_PU)

The PWRGD pin is an open drain output. Once the voltage on the SENSE+ pin is between 95% and 105% of the set voltage, the PWRGD pin pull-down is released and the pin floats. The recommended pullup resistor value is between 10 k Ω and 100-k Ω to a voltage source that is 12 V or less. The LMZ34202 has an internal 100-k Ω between the PWRGD pin (pin 20) and the PWRGD_PU pin (pin 21). Connect the PWRGD_PU pin to an external voltage source to avoid using an external pullup resistor. The PWRGD pin is pulled low when the voltage on SENSE+ is lower than 90% or greater than 110% of the nominal set voltage.

7.3.14 Overcurrent Protection

For protection against load faults, the LMZ34202 incorporates output overcurrent protection. Applying a load that exceeds the regulator's overcurrent threshold causes the output to shut down when the output voltage falls below the PWRGD threshold. Following shutdown, the module periodically attempts to recover by initiating a soft-start power-up as shown in 图 25. This is described as a hiccup mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced which reduces power dissipation. Once the fault is removed, the module automatically recovers and returns to normal operation as shown in 图 26.



7.3.15 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C typically. The device reinitiates the power up sequence when the junction temperature drops below 150°C typically.

7.4 Device Functional Modes

7.4.1 Active Mode

The LMZ34202 is in Active Mode when P_{VIN} is above the UVLO threshold and the INH/UVLO pin voltage is above the INH high threshold. The simplest way to enable the LMZ34202 is to connect the INH/UVLO terminal to P_{VIN} . This allows self start-up of the LMZ34202 when the input voltage is in the operation range: 4.5 V to 42 V.

7.4.2 Light Load Operation

At light load, the LMZ34202 operates in pulse skip mode to improve efficiency and decrease power dissipation by reducing switching losses and gate drive losses. In light load operation (PFM mode), the output voltage can rise slightly above the set-point specification. To avoid this behavior, a 300-mA load is required on the output.

7.4.3 Shutdown Mode

The INH/UVLO pin provides electrical ON and OFF control for the LMZ34202. When the INH/UVLO pin voltage is below the INH threshold, the device is in shutdown mode. In shutdown mode the stand-by current is 2.4 μ A typically with $P_{VIN} = 24$ V. The LMZ34202 also employs under voltage lock out protection. If P_{VIN} is below the UVLO level, the output of the regulator turns off.

8 Applications and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMZ34202 is a synchronous step down DC-DC power module. It is used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 2 A. The following design procedure can be used to select components for the LMZ34202. Alternately, the WEBENCH® software may be used to generate complete designs. When generating a design, the WEBENCH software utilizes an iterative design procedure and accesses comprehensive databases of components. Please visit www.ti.com/webench for more details.

8.1.1 Minimum External Component Application

The LMZ34202 requires only a few external components to convert from a wide input voltage supply range to a wide range of output voltages. [图 27](#) shows a basic LMZ34202 schematic with only the minimum required components.

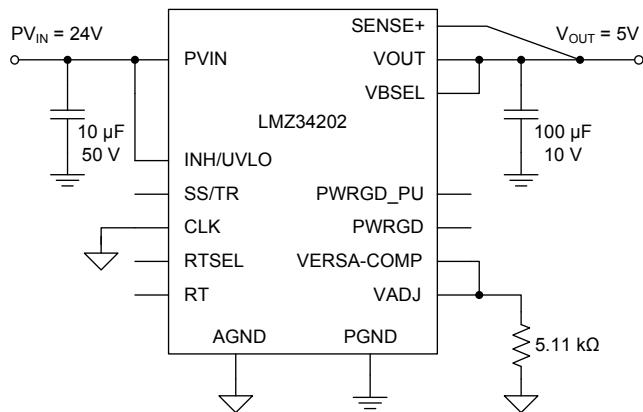


图 27. LMZ34202 Minimum External Component Application

8.1.1.1 Design Requirements

For this design example, use the parameters listed in [表 12](#) and follow the design procedures below.

表 12. Design Example Parameters

DESIGN PARAMETER	VALUE
Input Voltage PV _{IN}	24 V typical
Output Voltage V _{OUT}	5.0 V
Output Current Rating	2 A
Operating Frequency	500 kHz

8.1.1.2 Detailed Design Procedure

8.1.1.2.1 Output Voltage Set-Point

The output voltage of the LMZ34202 device is externally adjustable using a single resistor (R_{SET}). Select the value of R_{SET} from [表 2](#) or calculate using [公式 3](#):

$$R_{SET} = \frac{20}{\left[\left(\frac{V_{OUT}}{1.011} \right) - 1 \right]} \text{ (k}\Omega\text{)} \quad (3)$$

Knowing the desired output voltage is 5 V, the R_{SET} value can then be calculated using [公式 3](#) or selected from [表 2](#). The formula yields a value of 5.07 k Ω . Choose the closest available value of 5.11 k Ω for R_{SET} .

8.1.1.2.2 RT and RTSEL

The default switching frequency of the LMZ34202 is set to 500 kHz by leaving the RT pin open and the RTSEL pin open. The switching frequency of this application is 500-kHz, therefore no additional resistor is required to set the switching frequency. If another frequency is desired, use [表 3](#) to select the required resistor value.

8.1.1.2.3 VERSA-COMP

The Versa-Comp feature of the LMZ34202 configures the internal compensation based on the output voltage. From [表 8](#), the required Versa-Comp configuration for a 5-V output is to connect the VERSA-COMP pin to the VADJ pin.

8.1.1.2.4 VBSEL

The VBSEL pin allows the user to select the input source of the internal bias circuitry to improve efficiency. For output voltages ≥ 4.5 V, connect this pin to VOUT. For output voltages < 4.5 V, connect this pin to AGND.

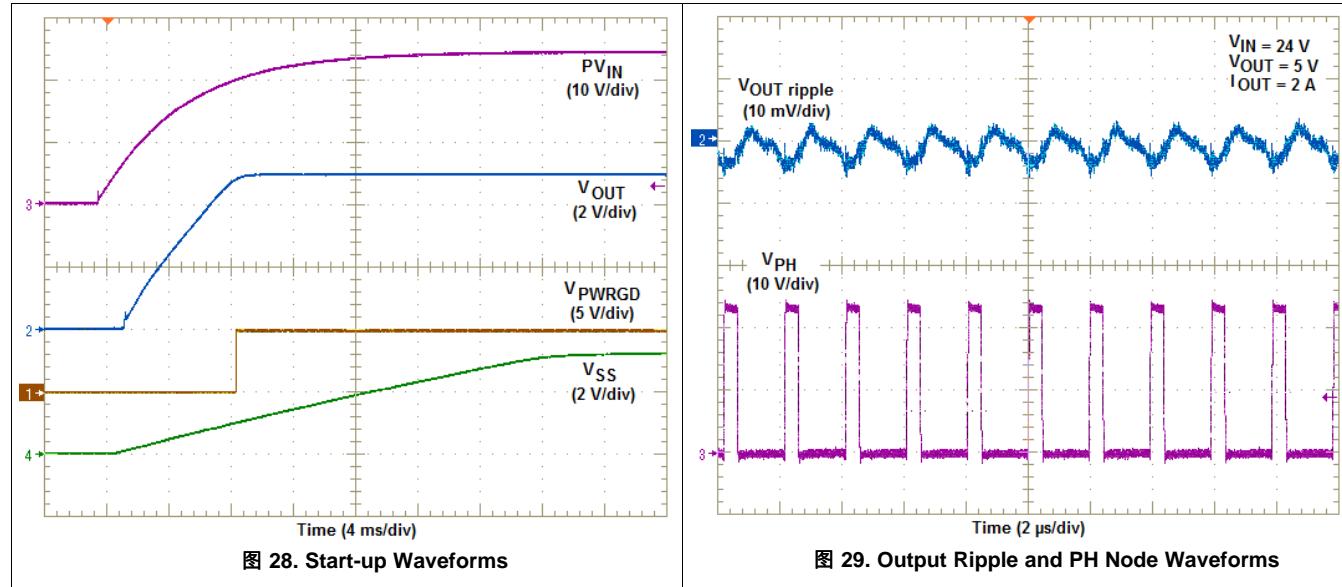
8.1.1.2.5 Input Capacitors

For this design, a 10- μ F, X7R dielectric ceramic capacitor rated for 50 V is used for the input decoupling capacitor. The effective capacitance at 24 V is 5.7 μ F, the equivalent series resistance (ESR) is approximately 3 m Ω , and the current-rating is 5 A.

8.1.1.2.6 Output Capacitors

The minimum required output capacitance for a 5 V output is 64 μ F of ceramic capacitance. For this design, a 100 μ F, X5R dielectric ceramic capacitor rated for 10 V is used for the output capacitor.

8.1.1.2.7 Application Waveforms



8.1.2 INH Control Application

图 30 显示了一个更典型的使用示例，它利用了 INH 控制、Versa-Comp、SS、PWRGD 和 PWRGD_PU 功能，以及通过外部电阻调整开关频率。设置这些附加功能的说明如下。

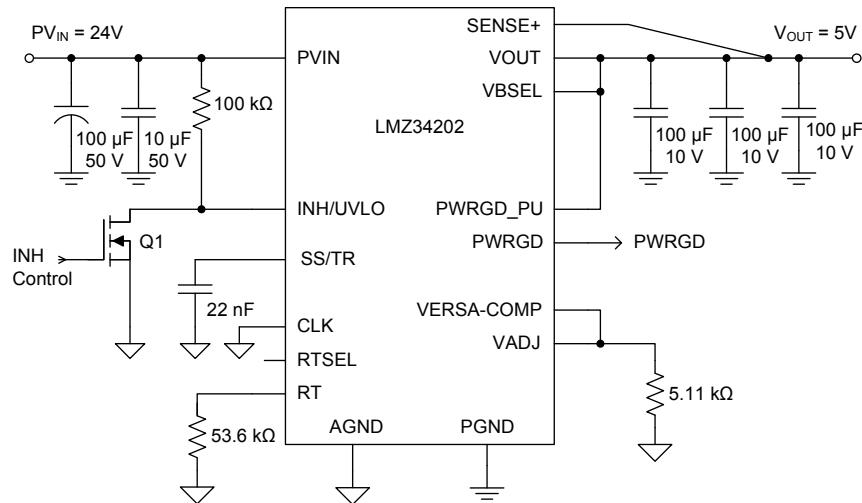


图 30. LMZ34202 Typical Schematic

8.1.2.1 Design Requirements

对于此设计示例，使用表 13 中列出的参数作为输入参数。对于完整的设计流程，请从基本应用示例开始，然后参考以下列出的流程。

表 13. Design Example Parameters

DESIGN PARAMETER	VALUE
Input Voltage PV_{IN}	24 V typical
Output Voltage V_{OUT}	5.0 V
Output Current Rating	2 A
Operating Frequency	750 kHz
Inhibit Control	Yes
Power Good Signal	Yes
Slow Start Time	10 ms
Output Capacitance	300 μ F

8.1.3 Detailed Design Procedure

8.1.3.1 Switching Frequency

要调整开关频率，请在 RT 引脚（引脚 9）和 AGND 之间放置一个电阻。参考表 3 选择所需的 RT 电阻值。要将开关频率设置为 750 kHz，所需的 RT 电阻值为 53.6 kΩ，从表 3 选择。

8.1.3.2 Power Good

Power Good 引脚是一个开漏输出。LMZ34202 包含一个从 Power Good 引脚到 PWRGD_PU 引脚的 100 kΩ 上拉电阻。将 PWRGD_PU 引脚连接到上拉电压，可以使用 Power Good 信号而无需添加额外的组件。在本示例中，5-V 输出被用作上拉电压。

8.1.3.3 Inhibit Control

To control the turn ON and OFF of the LMZ34202, an open-drain and collector device is recommended. The open-drain and collector device must be rated for the maximum voltage applied to PVIN. A pull-up resistor is required between the INH/UVLO pin and PVIN. Place a 100-k Ω resistor between the INH/UVLO pin and the PVIN pin.

8.1.3.4 VERSA-COMP

The Versa-Comp feature of the LMZ34202 configures the internal compensation based on the output voltage. From [表 8](#), the required Versa-Comp configuration for a 5-V output is to connect the VERSA-COMP pin to the VADJ pin.

8.1.3.5 VBSEL

The VBSEL pin allows the user to select the input source to the internal power circuitry to improve efficiency. For output voltages \geq 4.5 V, connect this pin to VOUT. For output voltages $<$ 4.5 V, connect this pin to AGND.

8.1.3.6 Soft-Start Capacitors

When the SS/TRK pin remains floating the LMZ34202 implements a typical soft-start time of 4.1 ms. In order to increase the slow start time, an external slow start capacitor, C_{SS} must be placed between the SS/TRK pin and AGND. Select a value for C_{SS} from [表 11](#).

For the desired soft-start time of 10 ms, a soft-start capacitor value of 22 nF is selected from [表 11](#).

8.1.3.7 Input Capacitors

For this design, a 10- μ F ceramic capacitor plus a 100- μ F aluminum electrolytic capacitor, both rated for 50 V are used for the input decoupling capacitors.

8.1.3.8 Output Capacitors

The maximum allowable output capacitance for a 5-V output is 350 μ F of capacitance. At least 64 μ F of capacitance must be ceramic type. For this design, 3x 100- μ F, X5R dielectric ceramic capacitors rated for 10 V are used for the output capacitors.

9 Power Supply Recommendations

The LMZ34202 is designed to operate from an input voltage supply range between 4.5 V and 42 V. This input supply should be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail should be low enough that an input current transient does not cause a high enough drop at the LMZ34202 supply voltage that can cause a false UVLO fault triggering and system reset.

If the input supply is located more than a few inches from the LMZ34202 additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The typical amount of bulk capacitance is 47 μ F or the typical amount of electrolytic capacitance is 100 μ F.

10 Layout

The performance of any switching power supply depends as much upon the layout of the PCB as the component selection. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

10.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. 图 31 thru 图 34, shows a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (PVIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Keep AGND and PGND separate from one another. The connection is made internal to the device.
- Place R_{SET} , R_{RT} , and C_{SS} as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.

10.2 Layout Example

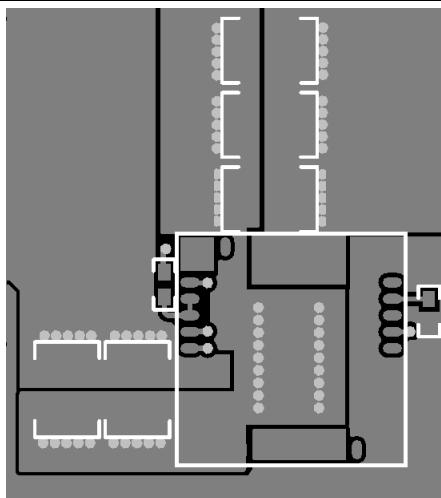


图 31. Typical Top-Layer Layout

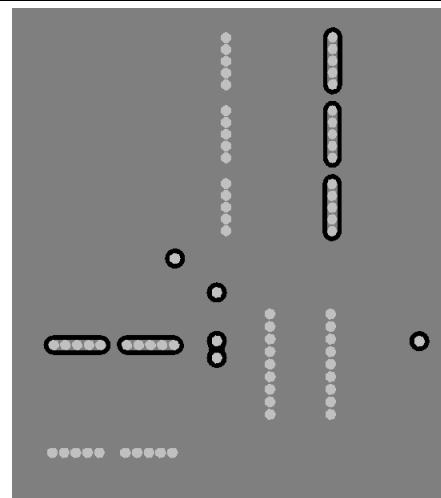


图 32. Typical Layer-2 Layout

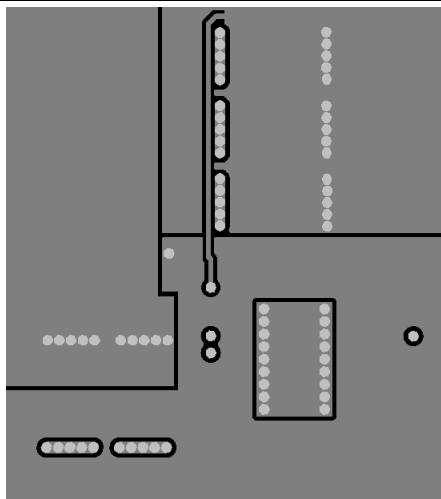


图 33. Typical Layer-3 Layout

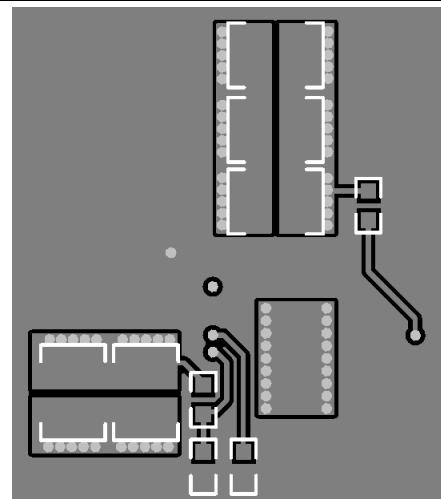
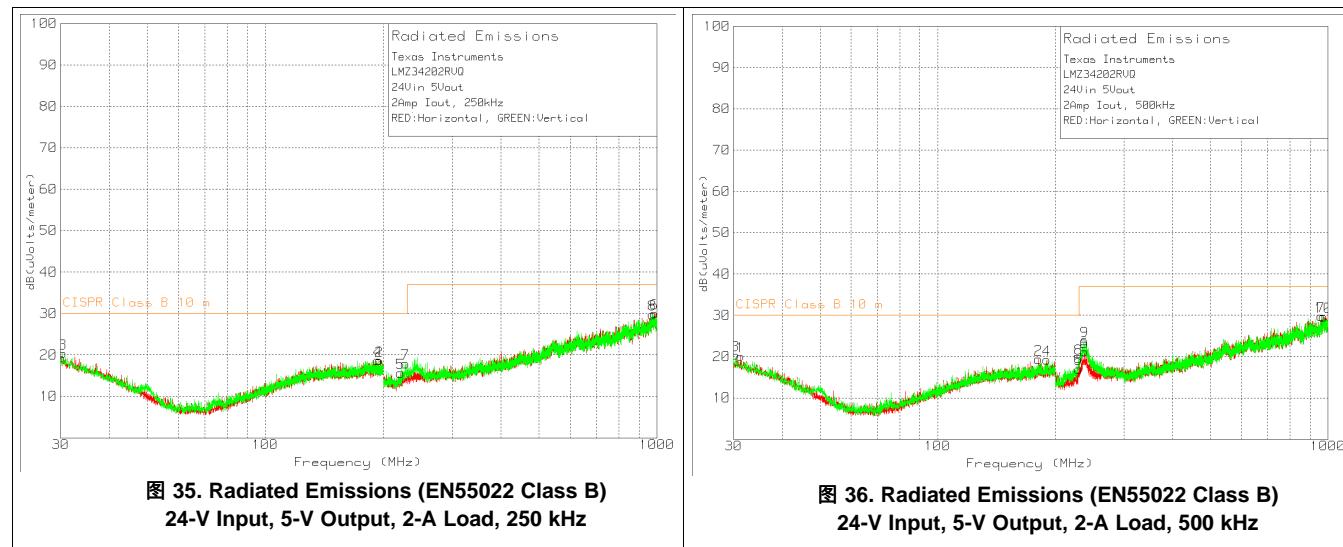


图 34. Typical Bottom-Layer Layout

10.3 EMI

The LMZ34202 is compliant with EN55022 Class B radiated emissions. [图 35](#) [图 36](#) show typical examples of radiated emissions plots for the LMZ34202 operating from 24 V. Both graphs include the plots of the antenna in the horizontal and vertical positions.



11 器件和文档支持

11.1 器件支持

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11.5 Glossary

[SLYZ022 — TI Glossary](#).

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMZ34202RVQR	ACTIVE	B3QFN	RVQ	43	500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-240C-1 YEAR	-40 to 105	(46002WV ~ LMZ34202)	Samples
LMZ34202RVQT	ACTIVE	B3QFN	RVQ	43	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-240C-1 YEAR	-40 to 105	(46002WV ~ LMZ34202)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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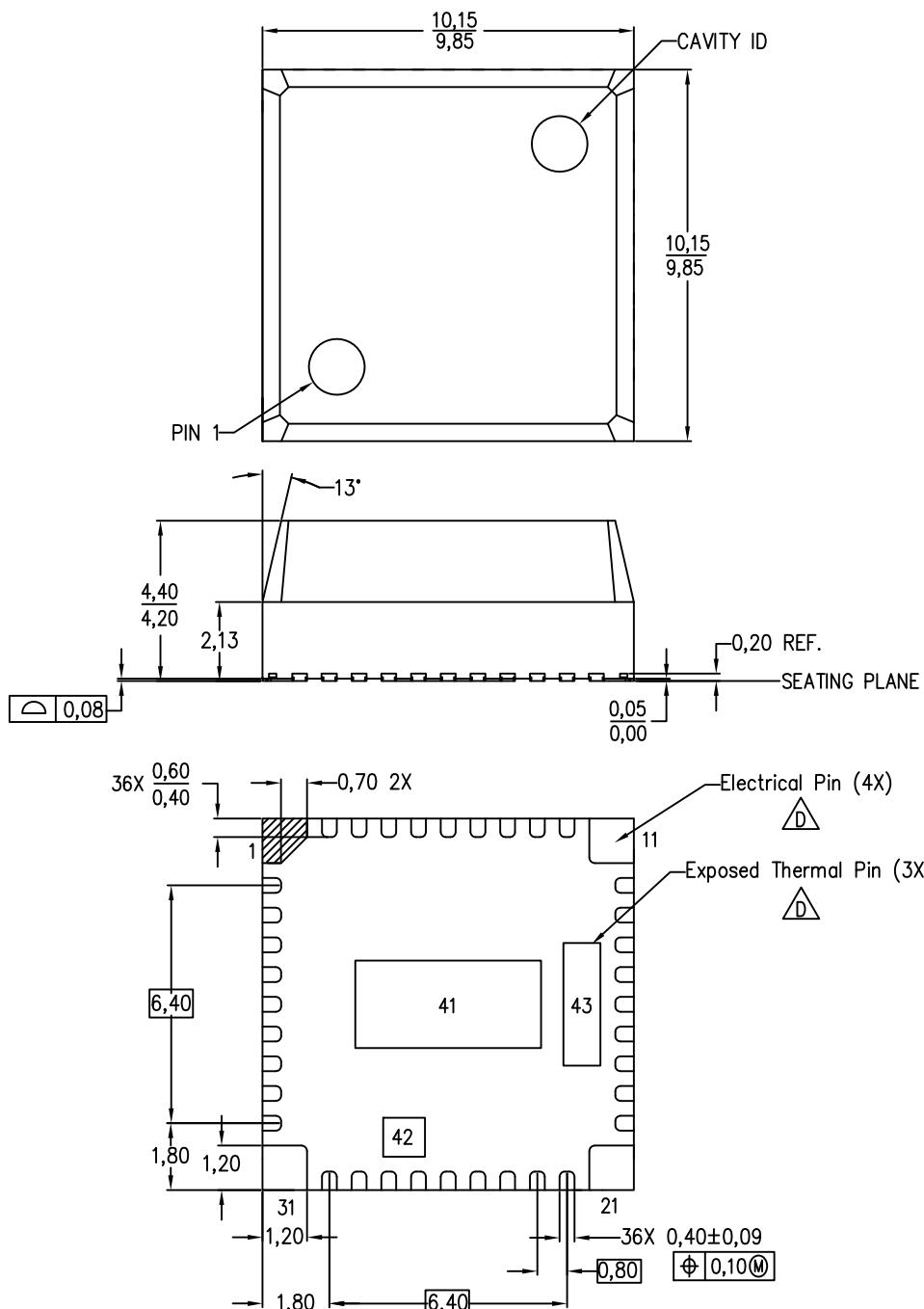
www.ti.com

PACKAGE OPTION ADDENDUM

11-Jul-2017

RVQ (S-PB3QFN-N43)

PLASTIC QUAD FLATPACK NO-LEAD



4212144-3/E 11/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Quad Flatpack, No-leads (QFN) package configuration.

D The package thermal pad must be soldered to the board for thermal and mechanical performance.

E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

F The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane.

THERMAL PAD MECHANICAL DATA

RVQ (R-PB3QFN-N43)

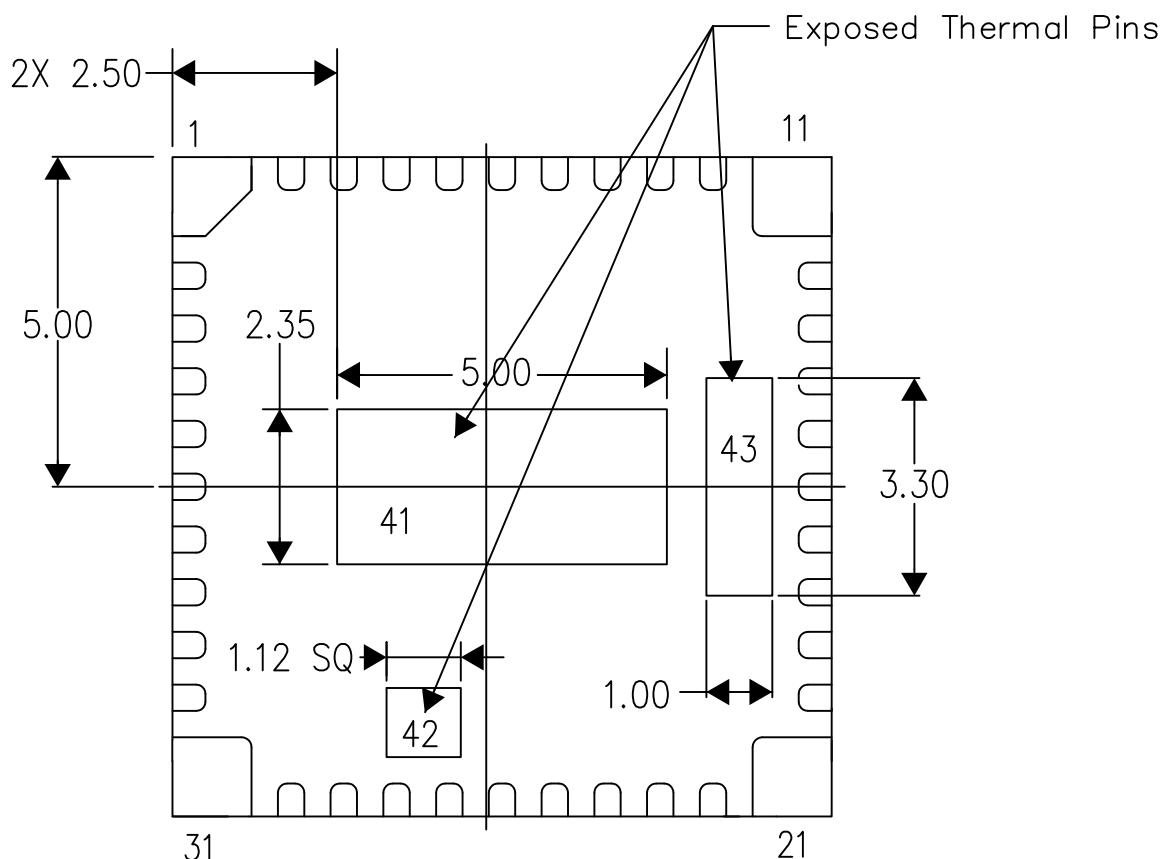
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



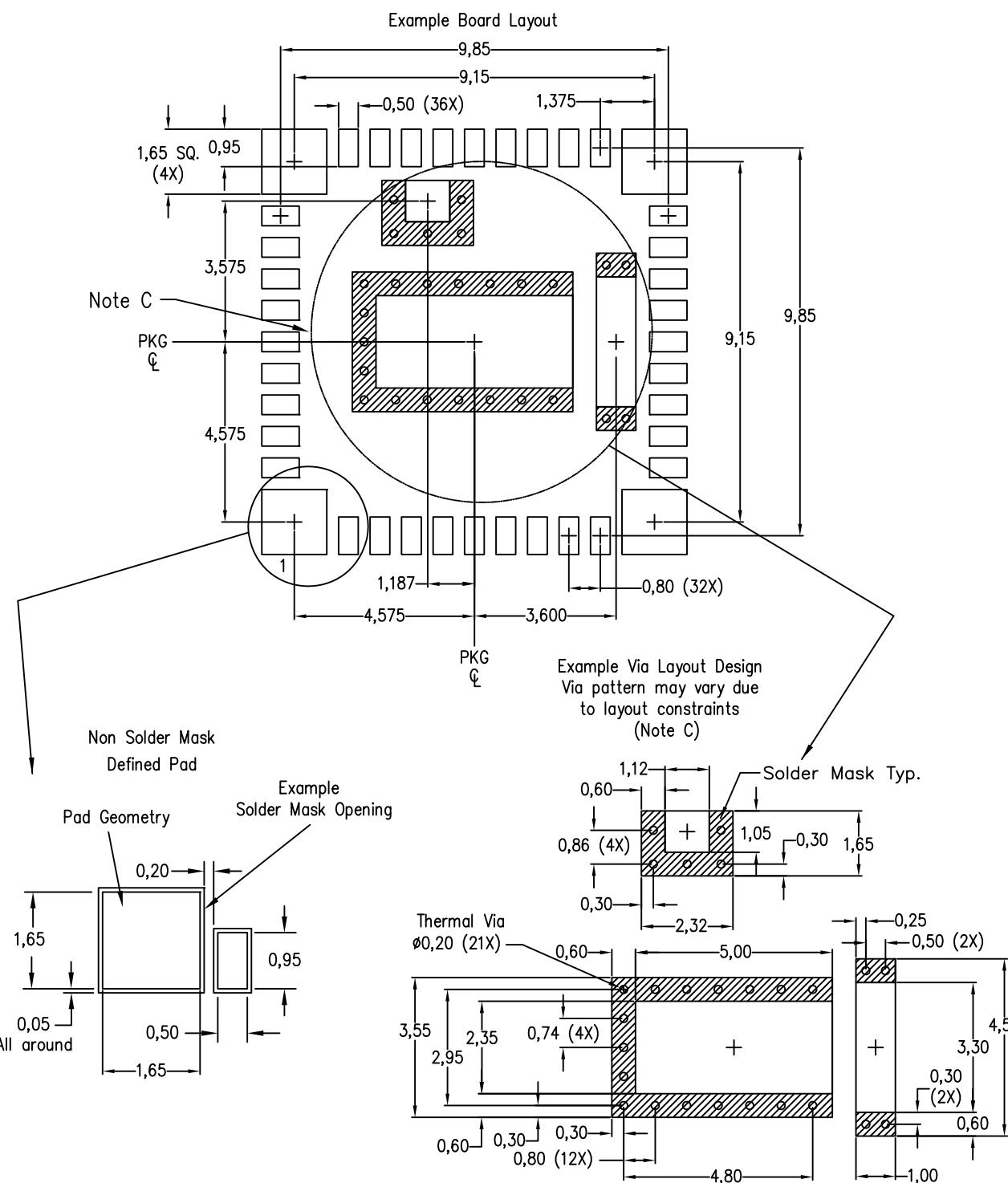
Bottom View
Exposed Thermal Pad Dimensions
Thermal Pad Tolerance: $\pm 0.10\text{mm}$

4221144-3/C 02/14

NOTE: All linear dimensions are in millimeters

RVQ (S-PB3QFN-N43)

PLASTIC QUAD FLATPACK NO-LEAD



4215269-4/F 08/14

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

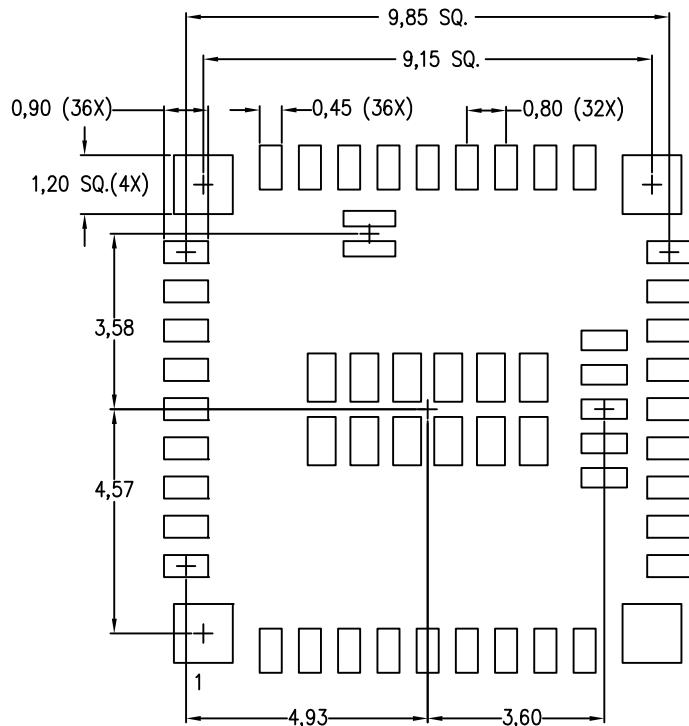
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.

D. See next page for stencil design recommendation.

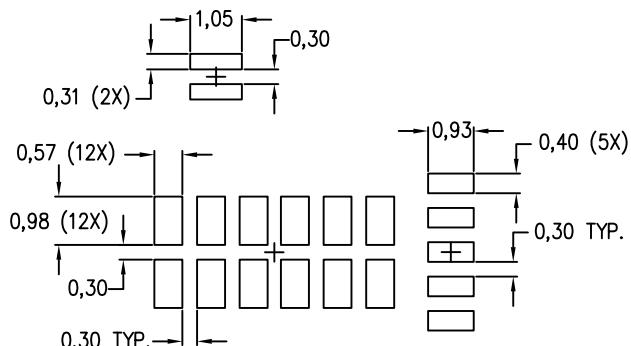
RVQ (S-PB3QFN-N43)

PLASTIC QUAD FLATPACK NO-LEAD

Example Stencil Design (Note E)



60% solder coverage on center pads



4215269-5/F 08/14

NOTES.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

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