

LM5175-Q1 42 V Wide V_{IN} Synchronous 4-Switch Buck-Boost Controller

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the following results:
 - Device Temperature Grade 1: -40°C to $+125^{\circ}\text{C}$ Ambient Operating Temperature Range
 - Device HBM ESD Classification Level 2
 - Device CDM ESD Classification Level C4B
- Single Inductor Buck-Boost Controller for Step-Up/Step-Down DC/DC Conversion
- Wide V_{IN} Range: 3.5 V to 42 V, 60 V Maximum
- Flexible V_{OUT} Range: 0.8 V to 55 V
- V_{OUT} Short Protection
- High Efficiency Buck-Boost Transition
- Adjustable Switching Frequency
- Optional Frequency Sync and Dithering
- Integrated 2-A MOSFET Gate Drivers
- Cycle-by-Cycle Current Limit and Optional Hiccup
- Optional Input or Output Average Current Limiting
- Programmable Input UVLO and Soft-Start
- Power Good and Output Overvoltage Protection
- Selectable CCM or DCM with Pulse Skipping
- HTSSOP-28 Package

2 Applications

- Automotive Start-Stop Systems
- Backup Battery and Supercapacitor Charging
- Industrial PC Power Supplies
- USB Power Delivery
- LED Lighting

3 Description

The LM5175-Q1 is a synchronous four-switch buck-boost DC/DC controller capable of regulating the output voltage at, above, or below the input voltage. The LM5175-Q1 operates over a wide input voltage range of 3.5 V to 42 V (60 V maximum) to support a variety of applications.

The LM5175-Q1 employs current-mode control both in buck and boost modes of operation for superior load and line regulation. The switching frequency is programmed by an external resistor and can be synchronized to an external clock signal.

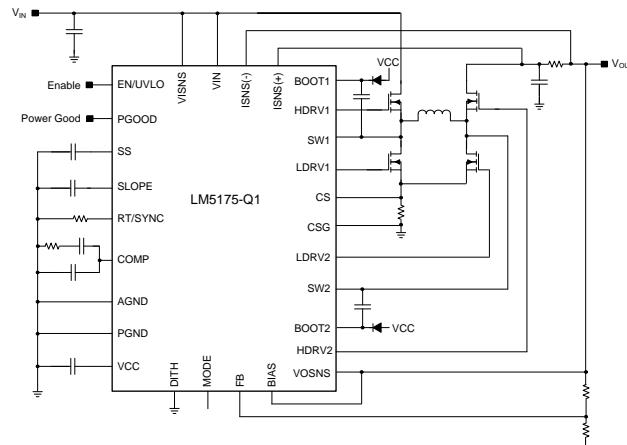
The device also features a programmable soft-start function and offers protection features including cycle-by-cycle current limiting, input undervoltage lockout (UVLO), output overvoltage protection (OVP), and thermal shutdown. In addition, the LM5175-Q1 features selectable Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM) operation, optional average input or output current limiting, optional spread spectrum to reduce peak EMI, and optional hiccup mode protection in sustained overload conditions.

Device Information⁽¹⁾

ORDER NUMBER	PACKAGE	BODY SIZE
LM5175-Q1	HTSSOP-28	9.7 mm x 4.4 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



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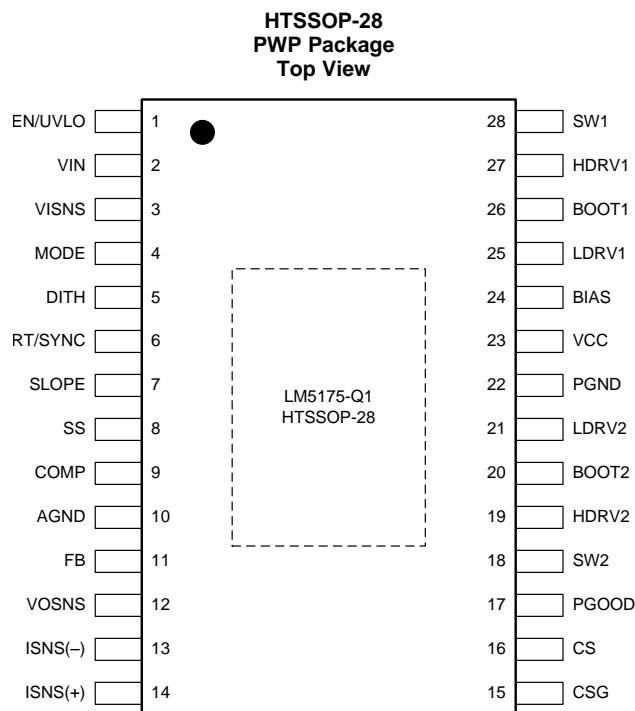
Table of Contents

1	Features	1	8.4	Device Functional Modes	19
2	Applications	1	9	Application and Implementation	20
3	Description	1	9.1	Application Information	20
4	Simplified Schematic	1	9.2	Typical Application	20
5	Revision History	2	10	Power Supply Recommendations	27
6	Pin Configuration and Functions	3	11	Layout	27
7	Specifications	4	11.1	Layout Guidelines	27
	7.1 Absolute Maximum Ratings	4	11.2	Layout Example	28
	7.2 ESD Ratings	5	12	Device and Documentation Support	29
	7.3 Recommended Operating Conditions	5	12.1	Documentation Support	29
	7.4 Thermal Information	5	12.2	Community Resources	29
	7.5 Electrical Characteristics	6	12.3	Trademarks	29
	7.6 Typical Characteristics	9	12.4	Electrostatic Discharge Caution	29
8	Detailed Description	12	12.5	Glossary	29
	8.1 Overview	12	13	Mechanical, Packaging, and Orderable	29
	8.2 Functional Block Diagram	13		Information	29
	8.3 Feature Description	14	13.1	Package Option Addendum	30

5 Revision History

DATE	REVISION	NOTES
April 2016	*	Initial Release

6 Pin Configuration and Functions



Pin Functions

PIN		DESCRIPTION
NO.	NAME	
1	EN/UVLO	Enable pin. For EN/UVLO < 0.4 V, the LM5175-Q1 is in a low current shutdown mode. For 0.7 V < EN/UVLO < 1.23 V, the controller operates in standby mode in which the VCC regulator is enabled but the PWM controller is not switching. For EN/UVLO > 1.23 V, the PWM function is enabled, provided VCC exceeds the VCC UV threshold.
2	VIN	The input supply pin to the IC. Connect V _{IN} to a supply voltage between 3.5 V and 42 V.
3	VISNS	V _{IN} sense input. Connect to the input capacitor.
4	MODE	Mode = GND, DCM, Hiccup Disabled (Set R _{MODE} resistor to GND = 0 Ω)
		Mode = 1.00 V, DCM, Hiccup Enabled (Set R _{MODE} resistor to GND = 49.9 kΩ)
		Mode = 1.85 V, CCM, Hiccup Enabled (Set R _{MODE} resistor to GND = 93.1 kΩ)
		Mode = VCC, CCM, Hiccup Disabled (Set R _{MODE} resistor to VCC = 0 Ω)
5	DITH	A capacitor connected between the DITH pin and AGND is charged and discharged with a 10 uA current source. As the voltage on the DITH pin ramps up and down the oscillator frequency is modulated between -5% and +5% of the nominal frequency set by the RT resistor. Grounding the DITH pin will disable the dithering feature. In the external Sync mode, the DITH pin voltage is ignored.
6	RT/SYNC	Switching frequency programming pin. An external resistor is connected to the RT/SYNC pin and AGND to set the switching frequency. This pin can also be used to synchronize the PWM controller to an external clock.
7	SLOPE	A capacitor connected between the SLOPE pin and AGND provides the slope compensation ramp for stable current mode operation in both buck and boost mode.
8	SS	Soft-start programming pin. A capacitor between the SS pin and AGND pin programs soft-start time.
9	COMP	Output of the error amplifier. An external RC network connected between COMP and AGND compensates the regulator feedback loop.
10	AGND	Analog ground of the IC.
11	FB	Feedback pin for output voltage regulation. Connect a resistor divider network from the output of the converter to the FB pin.

Pin Functions (continued)

PIN		DESCRIPTION
NO.	NAME	
12	VOSNS	V_{out} sense input. Connect to the output capacitor.
13 14	ISNS(–) ISNS(+)	Input or Output Current Sense Amplifier inputs. An optional current sense resistor connected between ISNS(+) and ISNS(–) can be located either on the input side or on the output side of the converter. If the sensed voltage across the ISNS(+) and ISNS(–) pins reaches 50 mV, a slow Constant Current (CC) control loop becomes active and starts discharging the soft-start capacitor to regulate the drop across ISNS(+) and ISNS(–) to 50 mV. Short ISNS(+) and ISNS(–) together to disable this feature.
15	CSG	The negative or ground input to the PWM current sense amplifier. Connect directly to the low-side (ground) of the current sense resistor.
16	CS	The positive input to the PWM current sense amplifier.
17	PGOOD	Power Good open drain output. PGOOD is pulled low when FB is outside a 0.8 V $\pm 10\%$ regulation window.
18 28	SW2 SW1	The boost and the buck side switching nodes respectively.
19 27	HDRV2 HDRV1	Output of the high-side gate drivers. Connect directly to the gates of the high-side MOSFETs.
20 26	BOOT2 BOOT1	An external capacitor is required between the BOOT1, BOOT2 pins and the SW1, SW2 pins respectively to provide bias to the high-side MOSFET gate drivers.
21 25	LDRV2 LDRV1	Output of the low-side gate drivers. Connect directly to the gates of the low-side MOSFETs.
22	PGND	Power ground of the IC. The high current ground connection to the low-side gate drivers.
23	VCC	Output of the VCC bias regulator. Connect capacitor to ground.
24	BIAS	Optional input to the VCC bias regulator. Powering VCC from an external supply instead of V_{IN} can reduce power loss at high V_{IN} . For $V_{BIAS} > 8$ V, the VCC regulator draws power from the BIAS pin. The BIAS pin voltage must not exceed 40 V.
-	PowerPAD™	The PowerPAD should be soldered to the analog ground. If possible, use thermal vias to connect to a PCB ground plane for improved power dissipation.

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

	MIN	MAX	UNIT
V_{IN} , EN/UVLO, VISNS, VOSNS, ISNS(+), ISNS(–)	-0.3	60	
BIAS	-0.3	40	
FB, SS, DITH, SLOPE, COMP	-0.3	3.6	
RT/SYNC	-0.3	6	
SW1, SW2	-1	60	
SW1, SW2 (20 ns transient)	-3.0	65	
VCC, MODE, PGOOD	-0.3	8.5	
LDRV1, LDRV2	-0.3	8.5	
BOOT1, HDRV1 with respect to SW1	-0.3	8.5	
BOOT2, HDRV2 with respect to SW2	-0.3	8.5	
BOOT1, BOOT2	-0.3	68	
CS, CSG	-0.3	0.3	
Maximum junction temperature ⁽²⁾	-40	150	°C
Storage temperature, T_{stg}	-65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000
		Charged-device model (CDM), per AEC Q100-011	All pins Corner pins
			±500 ±750

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage range	3.5	42		V
BIAS	Bias supply voltage range	8	36		
V _{OUT}	Output voltage range	0.8	55		
EN/JVLO	Enable voltage range	0	42		
ISNS(+), ISNS(-)	Average current sense common mode range	0	55		
T _J	Operating temperature range ⁽²⁾	-40	150		
F _{sw}	Operating frequency range	100	600		

(1) Recommended Operating Conditions are conditions under the device is intended to be functional. For specifications and test conditions, see [Electrical Characteristics](#).

(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾	LM5175-Q1	UNIT
	HTSSOP (PWP)	
	28 PINS	
R _{θJA}	33.1	°C/W
R _{θJC(top)}	17.7	
R _{θJB}	14.9	
Ψ _{JT}	0.4	
Ψ _{JB}	14.7	
R _{θJC(bot)}	1.1	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, [SPRA953](#).

7.5 Electrical Characteristics

Typical values correspond to $T_J = 25^\circ\text{C}$. Minimum and maximum limits apply over the $T_J = -40^\circ\text{C}$ to 125°C junction temperature range unless otherwise stated. $V_{IN} = 24\text{ V}$ unless otherwise stated.⁽¹⁾⁽²⁾

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_Q	V_{IN} shutdown current	$V_{EN/UVLO} = 0\text{ V}$	1.4	10	10	μA
	V_{IN} operating current	$V_{EN/UVLO} = 2\text{ V}$, $V_{FB} = 0.9\text{ V}$	1.65	4	4	mA
VCC						
$V_{VCC(VIN)}$	Regulation voltage	$V_{BIAS} = 0\text{ V}$, VCC open	6.95	7.35	7.88	V
$V_{UV(VCC)}$	VCC Undervoltage lockout	VCC increasing	3.11	3.27	3.43	
	Undervoltage hysteresis		160			mV
I_{VCC}	VCC current limit	$V_{VCC} = 0\text{ V}$	65			mA
$R_{OUT(VCC)}$	VCC regulator output impedance	$I_{VCC} = 30\text{ mA}$, $V_{IN} = 3.5\text{ V}$	9.3	16	16	Ω
BIAS						
$V_{BIAS(SW)}$	BIAS switchover voltage	$V_{IN} = 24\text{ V}$	7.25	8	8.75	V
EN/UVLO						
$V_{EN(STBY)}$	Standby threshold	EN/UVLO rising	0.55	0.79	0.97	V
$I_{EN(STBY)}$	Standby source current	$V_{EN/UVLO} = 1.1\text{ V}$	1	2	3	μA
$V_{EN(OP)}$	Operating threshold	EN/UVLO rising	1.15	1.23	1.29	V
$\Delta I_{HYS(OP)}$	Operating hysteresis current	$V_{EN/UVLO} = 1.5\text{ V}$	1.5	3.5	5.5	μA
SS						
I_{SS}	Soft-start pull up current	$V_{SS} = 0\text{ V}$	4.0	5.65	7.25	μA
$V_{SS(CL)}$	SS clamp voltage	SS open	1.27			V
$V_{FB} - V_{SS}$	FB to SS offset	$V_{SS} = 0\text{ V}$	-15			mV
EA (ERROR AMPLIFIER)						
V_{REF}	Feedback reference voltage	FB = COMP	0.788	0.800	0.812	V
gm_{EA}	Error amplifier gm		1.27			mS
I_{SINK}/I_{SOURCE}	COMP sink/source current	$V_{FB} = V_{REF} \pm 300\text{ mV}$	280			μA
R_{OUT}	Amplifier output resistance		20			$\text{M}\Omega$
BW	Unity gain bandwidth		2			MHz
$I_{BIAS(FB)}$	Feedback pin input bias current	FB in regulation	100			nA
FREQUENCY						
$f_{SW(1)}$	Switching Frequency 1	$RT = 133\text{ k}\Omega$	180	200	220	kHz
$f_{SW(2)}$	Switching Frequency 2	$RT = 47\text{ k}\Omega$	430	500	565	

- (1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
- (2) The junction temperature (T_J in $^\circ\text{C}$) is calculated from the ambient temperature (T_A in $^\circ\text{C}$) and power dissipation (P_D in Watts) as follows: $T_J = T_A + (P_D \cdot R_{\theta JA})$ where $R_{\theta JA}$ (in $^\circ\text{C}/\text{W}$) is the package thermal impedance provided in the [Thermal Information](#) section.

Electrical Characteristics (continued)

Typical values correspond to $T_J = 25^\circ\text{C}$. Minimum and maximum limits apply over the $T_J = -40^\circ\text{C}$ to 125°C junction temperature range unless otherwise stated. $V_{IN} = 24\text{ V}$ unless otherwise stated.⁽¹⁾⁽²⁾

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT	
DITHER						
I_{DITHER}	Dither source/sink current		10.5		μA	
V_{DITHER}	Dither high threshold		1.27		V	
	Dither low threshold		1.16			
SYNC						
V_{SYNC}	Sync input high threshold	2.1			V	
	Sync input low threshold		1.2			
PW_{SYNC}	Sync input pulse width	75	500		ns	
CURRENT LIMIT						
$V_{CS(BUCK)}$	Buck current limit threshold (Valley)	$V_{IN} = V_{VISNS} = 24\text{ V}$, $V_{VOSNS} = 12\text{ V}$, $V_{SLOPE} = 0\text{ V}$, $T_J = 25^\circ\text{C}$	53.2	76	98	mV
$V_{CS(BOOST)}$	Boost current limit threshold (Peak)	$V_{IN} = V_{VISNS} = 12\text{ V}$, $V_{VOSNS} = 24\text{ V}$, $V_{SLOPE} = 0\text{ V}$, $T_J = 25^\circ\text{C}$	114	160	202	
$I_{BIAS(CS/CSG)}$	CS/CSG pin bias current	$V_{CS} = V_{CSG} = 0\text{ V}$		-75		μA
$I_{OFFSET(CS/CSG)}$	CSG pin bias current	$V_{CS} = V_{CSG} = 0\text{ V}$			14	
CONSTANT CURRENT LOOP						
V_{SNS}	Average current loop regulation target	$V_{ISNS(-)} = 24\text{ V}$, sweep $ISNS(+)$, $V_{SS} = 0.8\text{ V}$	43	50	57	mV
I_{SNS}	$ISNS(+)$ / $ISNS(-)$ pin bias currents	$V_{ISNS(+)} = V_{ISNS(-)} = V_{IN} = 24\text{ V}$		7		μA
Gm	gm of soft-start pull down amplifier	$V_{ISNS(+)} - V_{ISNS(-)} = 50\text{ mV}$, $V_{SS} = 0.5\text{ V}$		1		mS
SLOPE						
I_{SLOPE}	Buck adaptive slope current	$V_{VISNS} = 24\text{ V}$, $V_{VOSNS} = 12\text{ V}$, $V_{SLOPE} = 0\text{ V}$	24	30	35	μA
	Boost adaptive slope current	$V_{VISNS} = 12\text{ V}$, $V_{VOSNS} = 18\text{ V}$, $V_{SLOPE} = 0\text{ V}$	13	17	21	
gm_{SLOPE}	Slope compensation amplifier gm			2		μS
MODE						
I_{MODE}	Source current out of MODE pin		17	20	23	μA
V_{DCM_HIC}	DCM with hiccup threshold		0.60	0.7	0.76	V
V_{CCM_HIC}	CCM with hiccup threshold		1.18	1.28	1.38	
V_{CCM}	CCM no hiccup threshold		2.22	2.4	2.6	

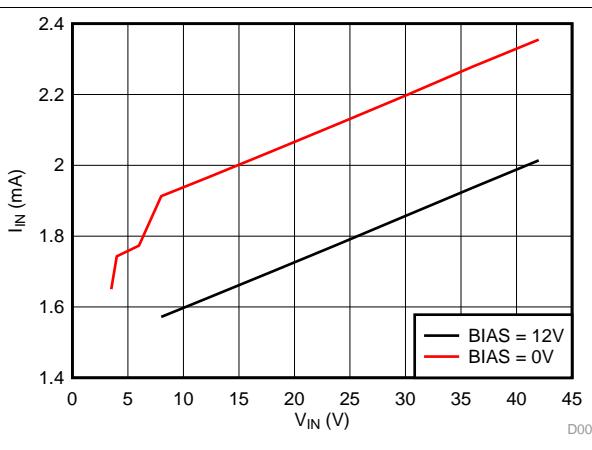
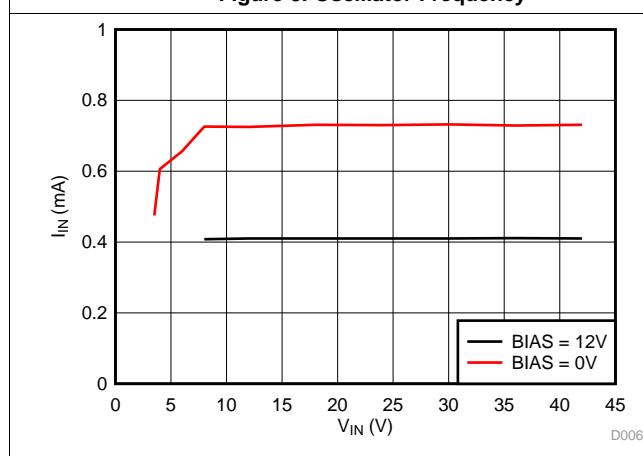
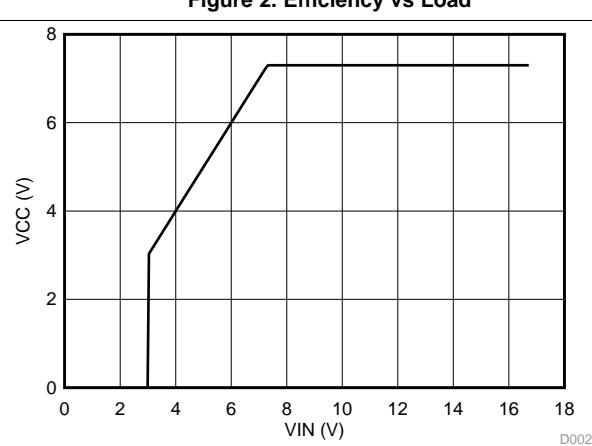
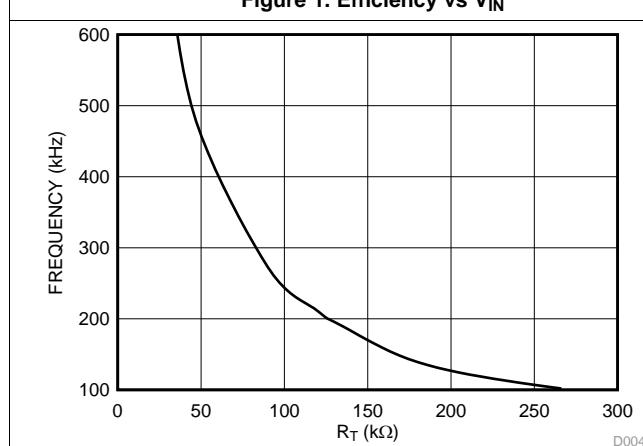
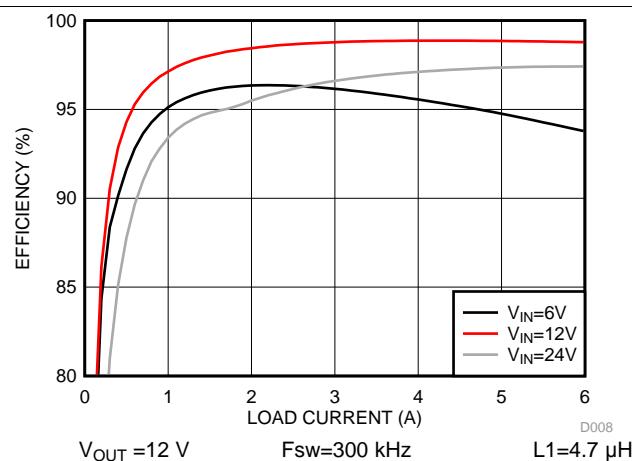
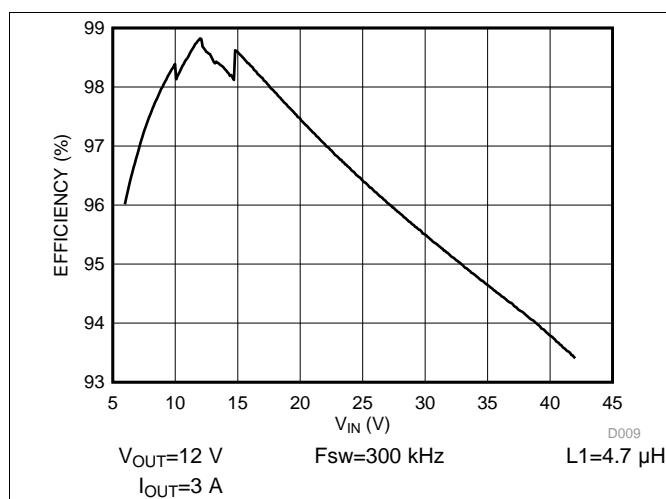
Electrical Characteristics (continued)

Typical values correspond to $T_J = 25^\circ\text{C}$. Minimum and maximum limits apply over the $T_J = -40^\circ\text{C}$ to 125°C junction temperature range unless otherwise stated. $V_{IN} = 24\text{ V}$ unless otherwise stated.⁽¹⁾⁽²⁾

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
PGOOD					
V_{PGD}	PGOOD trip threshold for falling FB	Measured with respect to V_{REF}		-9%	
	PGOOD trip threshold for rising FB	Measured with respect to V_{REF}		10%	
	Hysteresis			2%	
$I_{LEAK(PGD)}$	PGOOD leakage current			100	nA
$I_{SINK(PGD)}$	PGOOD sink current	$V_{PGOOD} = 0.4\text{ V}$	2	4.2	6.5
OUTPUT OVP					
V_{OVP}	Output overvoltage threshold	At the FB pin		0.86	V
	Hysteresis			21	mV
NMOS DRIVERS					
$I_{HDRV1,2}$	Driver peak source current	$V_{BOOT} - V_{SW} = 7\text{ V}$		1.8	A
	Driver peak sink current	$V_{BOOT} - V_{SW} = 7\text{ V}$		2.2	
$I_{LDRV1,2}$	Driver peak source current			1.8	
	Driver peak sink current			2.2	
$R_{HDRV1,2}$	Driver pull up resistance	$V_{BOOT} - V_{SW} = 7\text{ V}$		1.9	Ω
	Driver pull down resistance	$V_{BOOT} - V_{SW} = 7\text{ V}$		1.3	
$V_{UV(BOOT1,2)}$	BOOT1,2 to SW1,2 UVLO threshold	HDRV1,2 shut off		2.73	V
	BOOT1,2 to SW1,2 UVLO hysteresis	HDRV1,2 start switching		280	mV
	BOOT1,2 to SW1,2 threshold for refresh pulse			4.45	V
$R_{LDRV1,2}$	Driver pull up resistance			2	Ω
	Driver pull down resistance			1.5	
t_{DT1}	Dead time HDRV1,2 off to LDRV1,2 on			55	ns
t_{DT2}	Dead time LDRV1,2 off to HDRV1,2 on			55	
THERMAL SHUTDOWN					
T_{SD}	Thermal shutdown temperature			165	$^\circ\text{C}$
$T_{SD(HYS)}$	Thermal shutdown hysteresis			15	

7.6 Typical Characteristics

At $T_A = 25^\circ\text{C}$, unless otherwise stated.



Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, unless otherwise stated.

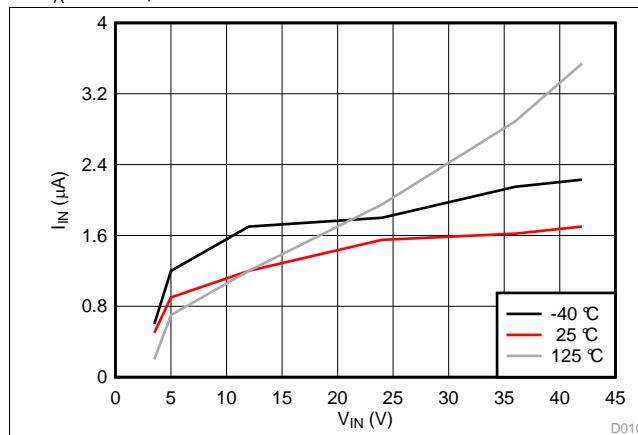


Figure 7. I_{IN} Shutdown vs V_{IN}

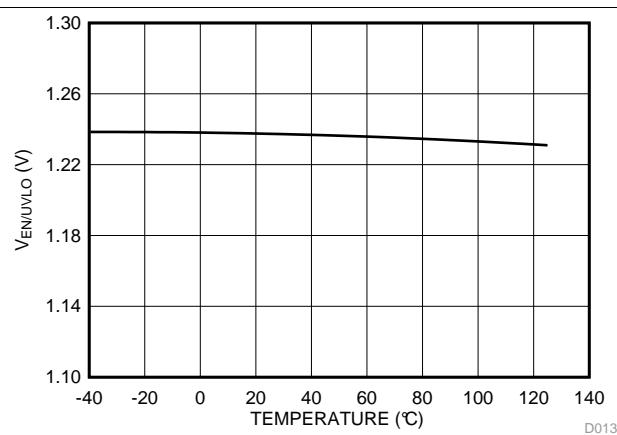


Figure 8. ENABLE/UVLO Rising Threshold vs Temperature

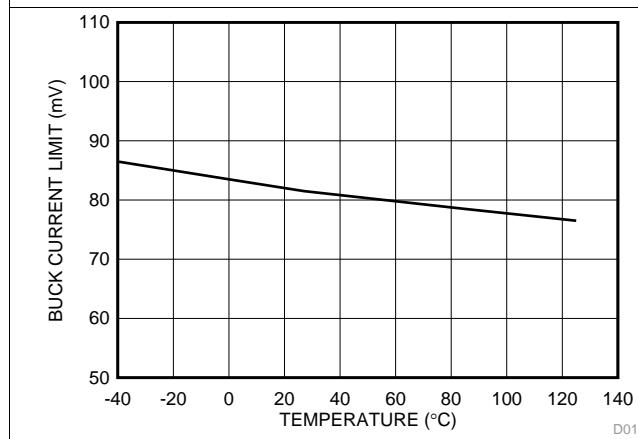


Figure 9. Buck Current Limit vs Temperature

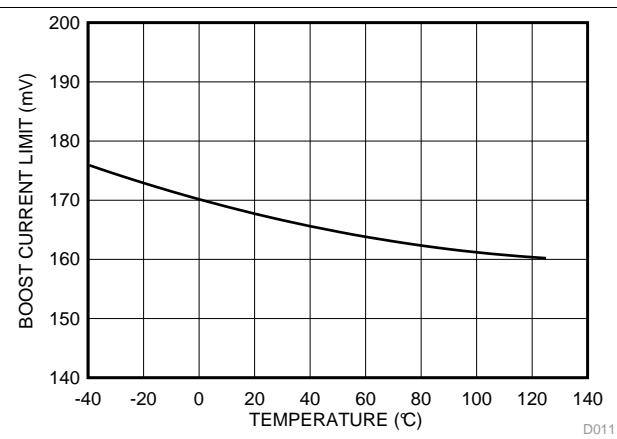


Figure 10. Boost Current Limit vs Temperature

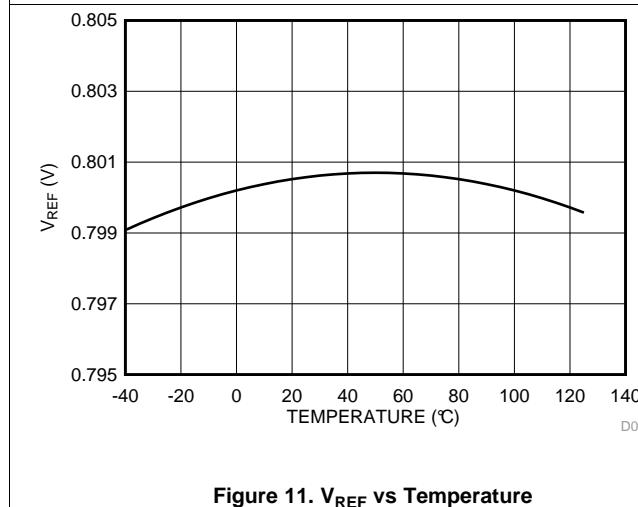


Figure 11. V_{REF} vs Temperature

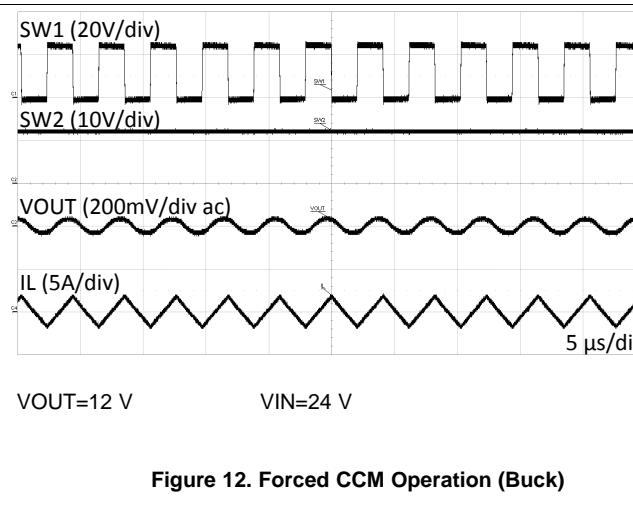


Figure 12. Forced CCM Operation (Buck)

Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, unless otherwise stated.

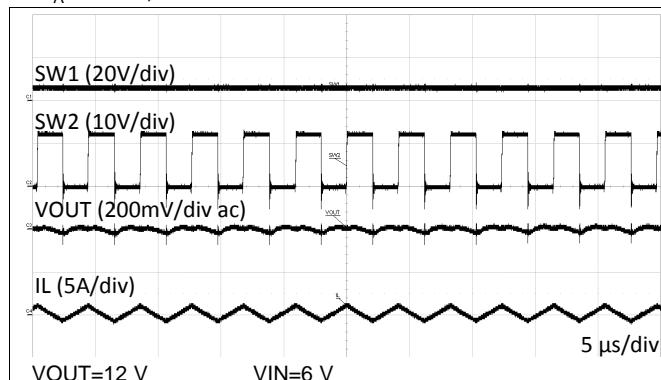


Figure 13. Forced CCM Operation (Boost)

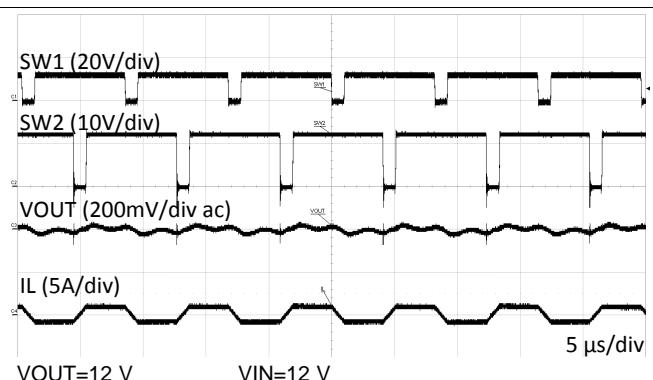


Figure 14. Forced CCM Operation (Buck-Boost)

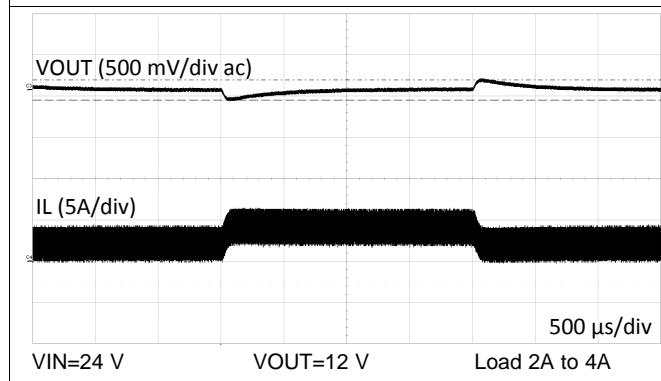


Figure 15. Load Step (Buck)

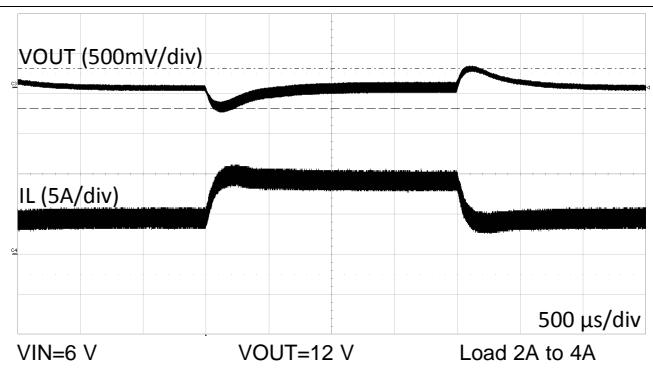


Figure 16. Load Step (Boost)

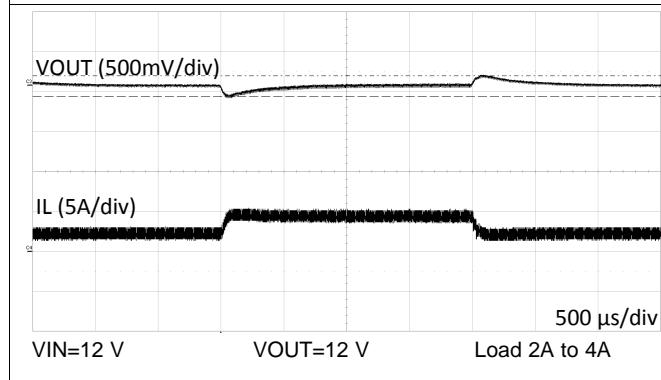


Figure 17. Load Step (Buck-Boost)

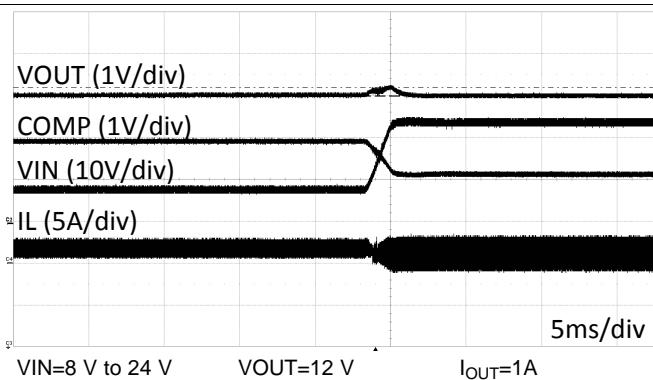


Figure 18. Line Transient

Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, unless otherwise stated.

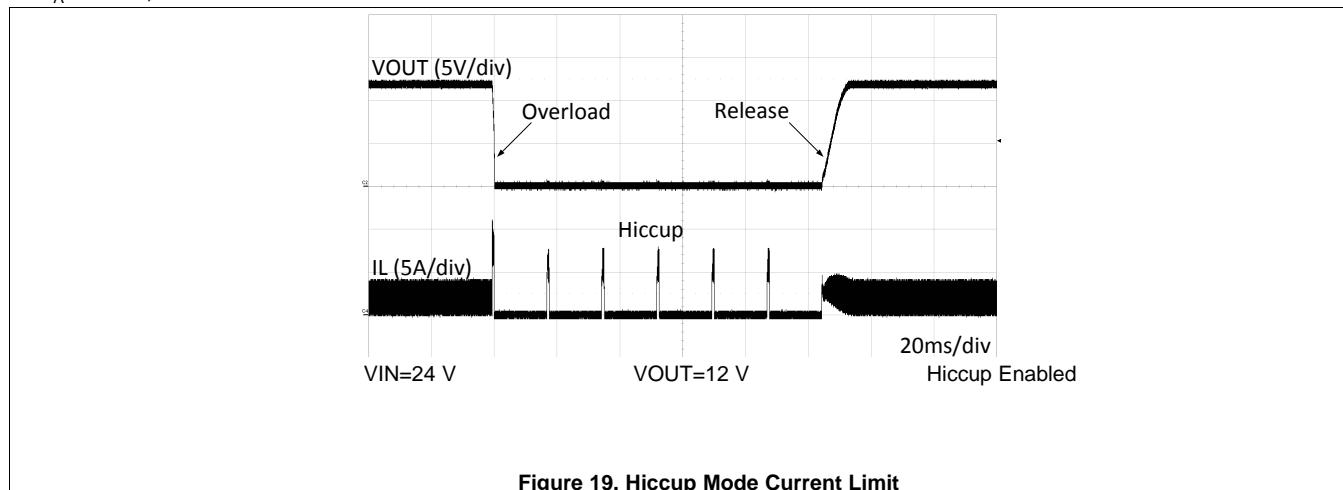


Figure 19. Hiccup Mode Current Limit

8 Detailed Description

8.1 Overview

The LM5175-Q1 is a wide input voltage four-switch buck-boost controller IC with integrated drivers for N-channel MOSFETs. It operates in the buck mode when V_{IN} is greater than V_{OUT} and in the boost mode when V_{IN} is less than V_{OUT} . When V_{IN} is close to V_{OUT} , the device operates in a proprietary transition buck or boost mode. The control scheme provides smooth operation for any input/output combination within the specified operating range. The buck or boost transition control scheme provides a low ripple output voltage when V_{IN} equals V_{OUT} without compromising the efficiency.

The LM5175-Q1 integrates four N-Channel MOSFET drivers including two low-side drivers and two high-side drivers, eliminating the need for external drivers or floating bias supplies. The internal VCC regulator supplies internal bias rails as well as the MOSFET gate drivers. The VCC regulator is powered either from the input voltage through the VIN pin or from the output or an external supply through the BIAS pin for improved efficiency.

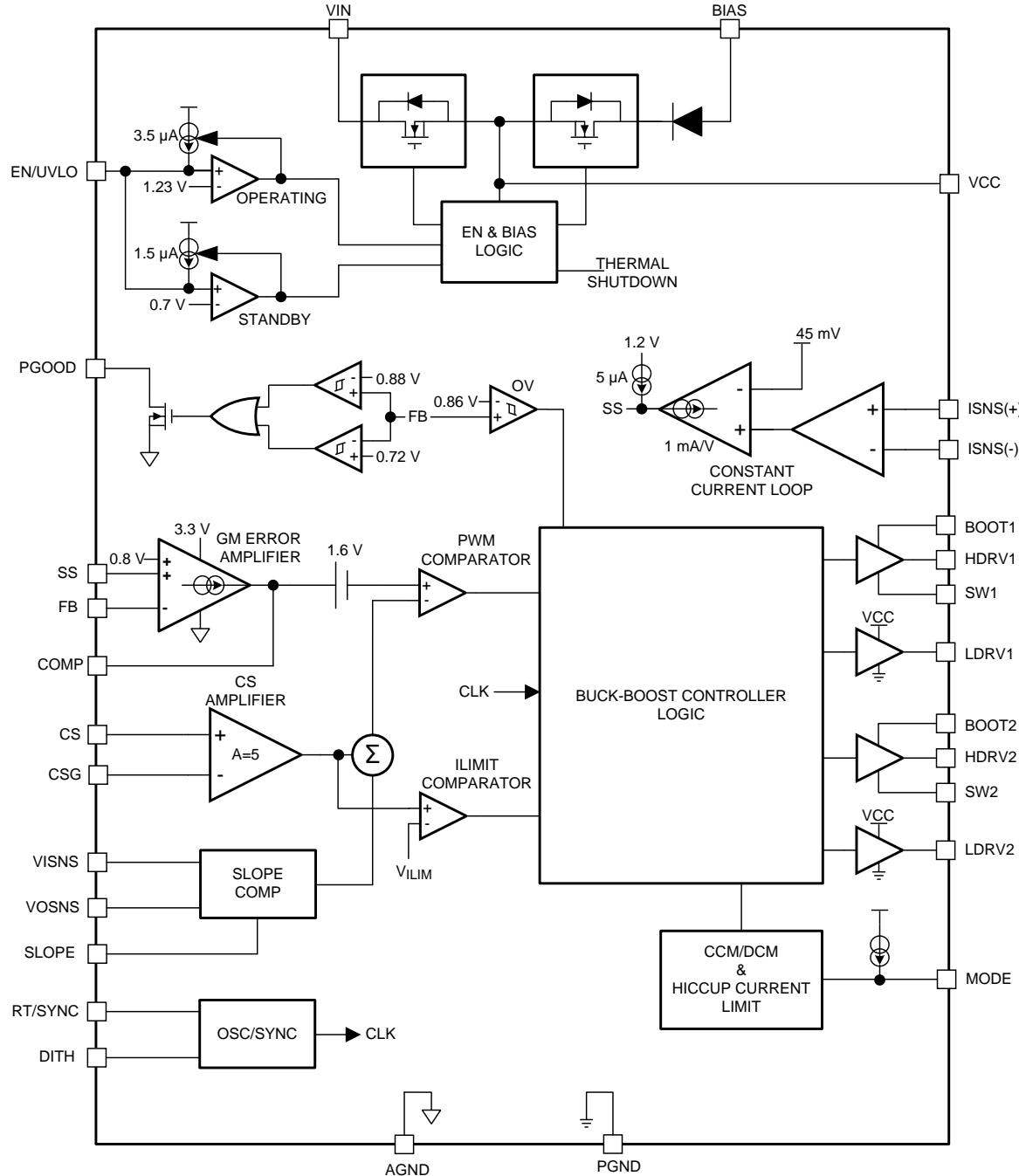
The PWM control scheme is based on valley current mode control for buck operation and peak current mode control for boost operation. The inductor current is sensed through a single sense resistor in series with the low-side MOSFETs. The sensed current is also monitored for cycle-by-cycle current limit. The behavior of the LM5175-Q1 during an overload condition is dependent on the MODE pin programming (see [MODE Pin Configuration](#)). If hiccup mode fault protection is selected, the controller turns off after a fixed number of switching cycles in cycle-by-cycle current limit and restarts after another fixed number of clock cycles. The hiccup mode reduces the heating in the power components in a sustained overload condition. If hiccup mode is disabled through the MODE pin, the controller remains in a cycle-by-cycle current limit condition until the overload is removed. The MODE pin also selects continuous conduction mode (CCM) for noise sensitive applications or discontinuous conduction mode (DCM) for higher light load efficiency.

In addition to the cycle-by-cycle current limiting, the LM5175-Q1 also provides an optional average current regulation loop that can be configured for either input or output current limiting. This is useful for battery charging or other applications where a constant current behavior may be required.

The soft-start time of LM5175-Q1 is programmed by a capacitor connected to the SS pin to minimize the inrush current and overshoot during startup.

The precision EN/UVLO pin supports programmable input undervoltage lockout (UVLO) with hysteresis. The output overvoltage protection (OVP) feature turns off the high-side drivers when the voltage at the FB pin is 7.5% above the nominal 0.8-V V_{REF} . The PGOOD output indicates when the FB voltage is inside a $\pm 10\%$ regulation window centered at V_{REF} .

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Fixed Frequency Valley/Peak Current Mode Control with Slope Compensation

The LM5175-Q1 implements a fixed frequency current mode control of both the buck and boost switches. The output voltage, scaled down by the feedback resistor divider, appears at the FB pin and is compared to the internal reference (V_{REF}) by an internal error amplifier. The error amplifier produces an error voltage by driving the COMP pin. An adaptive slope compensation signal based on V_{IN} , V_{OUT} , and the capacitor at the SLOPE pin is added to the current sense signal measured across the CS and CSG pins. The result is compared to the COMP error voltage by the PWM comparator.

The LM5175-Q1 regulates the output using valley current mode control in buck mode and peak current mode control in boost mode. For valley current mode control, the high-side buck MOSFET controlled by HDRV1 is turned on by the PWM comparator at the valley of the inductor ripple current and turned off by the oscillator clock signal. Valley current mode control is advantageous for buck converters where the PWM controller must resolve very short on-times. For peak current mode control in the boost mode, the low-side boost MOSFET controlled by LDRV2 is turned on by the clock signal in each switching cycle and turned off by the PWM comparator at the peak of the inductor ripple current.

The low-side gate drive LDRV1, complementary to the HDRV1 drive signal, controls the synchronous rectification MOSFET of the buck stage. The high-side gate drive HDRV2, complementary to the low-side gate drive LDRV2, controls the high-side synchronous rectifier of the boost stage. For operation with V_{IN} close to V_{OUT} , the LM5175-Q1 uses a proprietary buck or boost transition scheme to achieve smooth, low ripple transition zone behavior.

Peak and valley current mode controllers require slope compensation for stable current loop operation at duty cycle greater than 50% in peak current mode control and less than 50% in valley current mode control. The LM5175-Q1 provides a SLOPE pin to program optimum slope for any V_{IN} and V_{OUT} combination using an external capacitor.

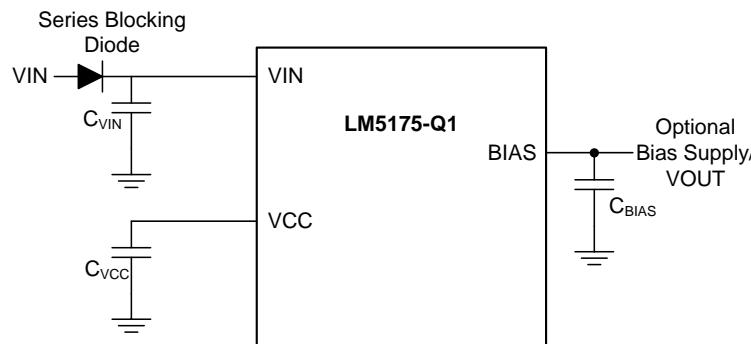
8.3.2 VCC Regulator and Optional BIAS Input

The VCC regulator provides a regulated 7.5-V bias supply to the gate drivers. When EN/UVLO is above the 0.7-V (typical) standby threshold, the VCC regulator is turned on. For V_{IN} less than 7.5 V, the VCC voltage tracks V_{IN} with a small voltage drop as shown in Figure 4. If the EN/UVLO input is above the 1.23 V operating threshold and VCC exceeds the 3.3 V (typical) VCC UV threshold, the controller is enabled and switching begins.

The VCC regulator draws power from V_{IN} when there is no supply voltage connected to the BIAS pin. If the BIAS pin is connected to an external voltage source that exceeds VCC by one diode drop, the VCC regulator draws power from the BIAS input instead of V_{IN} . Connecting the BIAS pin to V_{OUT} in applications with V_{OUT} greater than 8.5 V improves the efficiency of the regulator in the buck mode. The BIAS pin voltage should not exceed 36 V.

For low V_{IN} operation, ensure that the VCC voltage is sufficient to fully enhance the MOSFETs. Use an external bias supply if V_{IN} dips below the voltage required to sustain the VCC voltage. For these conditions, use a series blocking diode between the input supply and the VIN pin (Figure 20). This prevents VCC from back-feeding into V_{IN} through the body diode of the VCC regulator.

A 1- μ F capacitor to PGND is required to supply the VCC regulator load transients.



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Figure 20. VCC Regulator

Feature Description (continued)

8.3.3 Enable/UVLO

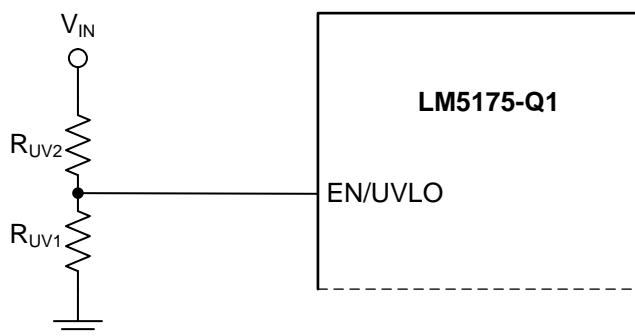
The LM5175-Q1 has a dual function enable and undervoltage lockout (UVLO) circuit. The EN/UVLO pin has three distinct voltage ranges: shutdown, standby, and operating (see [Shutdown, Standby, and Operating Modes](#)). When the EN/UVLO pin is below the standby threshold (0.7 V typical), the converter is held in a low power shutdown mode. When EN/UVLO voltage is greater than the standby threshold but less than the 1.23 V operating threshold, the internal bias rails and the VCC regulator are enabled but the soft-start (SS) pin is held low and the PWM controller is disabled. A 1.5 μ A pull-up current is sourced out of the EN/UVLO pin in standby mode to provide hysteresis between the shutdown mode and the standby mode. When EN/UVLO is greater than the 1.23 V operating threshold, the controller commences operation if VCC is above VCC UV threshold (3.3 V). A hysteresis current of 3.5 μ A is sourced into the EN/UVLO pin when the EN/UVLO input exceeds the 1.23 V operation threshold to provide hysteresis that prevents on/off chattering in the presence of noise with a slowly changing input voltage.

The V_{IN} undervoltage lockout turn-on threshold is typically set by a resistor divider from the V_{IN} pin to AGND with the mid-point of the divider connected to EN/UVLO. The turn-on threshold $V_{IN(UV)}$ is calculated using [Equation 1](#) where R_{UV2} is the upper resistor and R_{UV1} is the lower resistor in the EN/UVLO resistor divider:

$$V_{IN(UV)} = 1.23 \text{ V} \times \left(1 + \frac{R_{UV2}}{R_{UV1}} \right) - R_{UV2} \times 1.5 \mu\text{A} \quad (1)$$

The hysteresis between the UVLO turn-on threshold and turn-off threshold is set by the upper resistor in the EN/UVLO resistor divider and is given by:

$$\Delta V_{HYS(UV)} = 3.5 \mu\text{A} \times R_{UV2} \quad (2)$$



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Figure 21. UVLO Threshold Programming

8.3.4 Soft-Start

The LM5175-Q1 soft-start time is programmed using a soft-start capacitor from the SS pin to AGND. When the converter is enabled, an internal 5- μ A current source charges the soft-start capacitor. When the SS pin voltage is below the 0.8-V feedback reference voltage V_{REF} , the soft-start pin controls the regulated FB voltage. Once SS exceeds V_{REF} , the soft-start interval is complete and the error amplifier is referenced to V_{REF} . The soft-start time is given by [Equation 3](#):

$$t_{ss} = \frac{C_{ss} \times 0.8 \text{ V}}{5 \mu\text{A}} \quad (3)$$

The soft-start capacitor is internally discharged when the converter is disabled because of EN/UVLO falling below the operation threshold or VCC falling below the VCC UV threshold. The soft-start pin is also discharged when the converter is in hiccup mode current limiting or in thermal shutdown. When average input or output current limiting is active, the soft-start capacitor is discharged by the constant current loop transconductance (gm) amplifier to limit either input or output current.

Feature Description (continued)

8.3.5 Overcurrent Protection

The LM5175-Q1 provides cycle-by-cycle current limit to protect against overcurrent and short circuit conditions. In buck operation, the sensed valley voltage across the CSG and CS pins is limited to 76 mV. The high-side buck switch skips a cycle if the sensed voltage does not fall below this threshold during the buck switch off time. In boost operation, the maximum peak voltage across CS and CSG is limited to 160 mV. If the peak current in the low-side boost switch causes the CS pin to exceed this threshold voltage, the boost switch is turned off for the remainder of the clock cycle.

Applying the appropriate voltage to the MODE pin of the LM5175-Q1 enables hiccup mode fault protection (see [MODE Pin Configuration](#)). In the hiccup mode, the controller shuts down after detecting cycle-by-cycle current limiting for 128 consecutive cycles and the soft-start capacitor is discharged. The soft-start capacitor is automatically released after 4000 oscillator clock cycles and the controller restarts. If hiccup mode protection is not enabled through the MODE pin, the LM5175-Q1 will operate in cycle-by-cycle current limiting as long as the overload condition persists.

8.3.6 Average Input/Output Current Limiting

The LM5175-Q1 provides optional average current limiting capability to limit either the input or the output current of the DC/DC converter. The average current limiting circuit uses an additional current sense resistor connected in series with the input supply or output voltage of the converter. A current sense gm amplifier with inputs at the ISNS(+) and ISNS(-) pins monitors the voltage across the sense resistor and compares it with an internal 50 mV reference. If the drop across the sense resistor is greater than 50 mV, the gm amplifier gradually discharges the soft-start capacitor. When the soft-start capacitor discharges below the 0.8-V feedback reference voltage V_{REF} , the output voltage of the converter decreases to limit the input or output current. The average current limiting feature can be used in applications requiring a regulated current from the input supply or into the load. The target constant current is given by [Equation 4](#):

$$I_{CL(AVG)} = \frac{50 \text{ mV}}{R_{SNS}} \quad (4)$$

The average current loop can be disabled by shorting the ISNS(+) and ISNS(-) pins together.

8.3.7 CCM/DCM Operation

The LM5175-Q1 allows selection of continuous conduction mode (CCM) or discontinuous conduction mode (DCM) operation using the MODE pin (see [MODE Pin Configuration](#)). In CCM operation the inductor current can flow in either direction and the controller switches at a fixed frequency regardless of the load current. This mode is useful for noise-sensitive applications where a fixed switching eases filter design. In DCM operation the synchronous rectifier MOSFETs emulate diodes as LDRV1 or HDRV2 turn-off for the remainder of the PWM cycle when the inductor current reaches zero. The DCM mode results in reduced frequency operation at light loads, which lowers switching losses and increases light load efficiency of the converter.

8.3.8 Frequency and Synchronization (RT/SYNC)

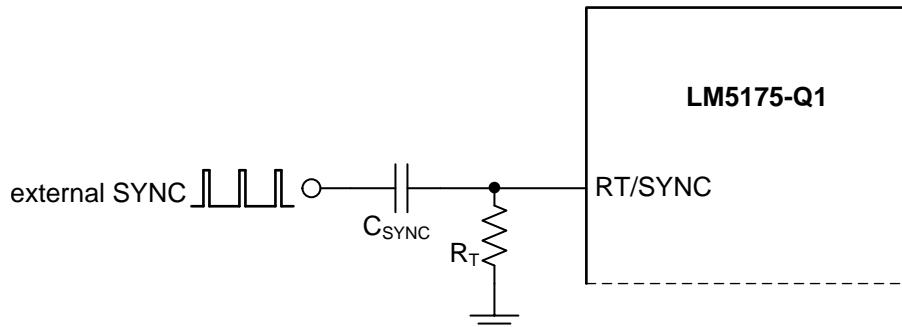
The LM5175-Q1 switching frequency can be programmed between 100 kHz and 600 kHz using a resistor from the RT/SYNC pin to AGND. The R_T resistor is related to the nominal switching frequency (F_{sw}) by the following equation:

$$R_T = \frac{\left(\frac{1}{F_{sw}}\right) - 200 \text{ ns}}{37 \text{ pF}} \quad (5)$$

[Figure 3](#) in the [Typical Characteristics](#) shows the relationship between the programmed switching frequency (F_{sw}) and the R_T resistor.

Feature Description (continued)

The RT/SYNC pin can also be used for synchronizing the internal oscillator to an external clock signal. The external synchronization pulse is ac coupled using a capacitor to the RT/SYNC pin. The voltage at the RT/SYNC pin must not exceed 3.3 V peak. The external synchronization pulse frequency should be higher than the internally set oscillator frequency and the pulse width should be between 75 ns and 500 ns.



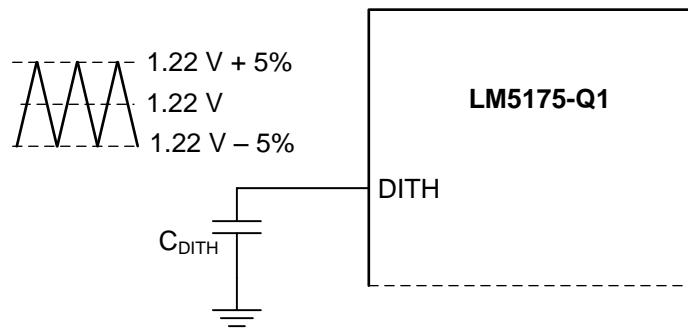
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Figure 22. Using External SYNC

8.3.9 Frequency Dithering

The LM5175-Q1 provides an optional frequency dithering function that is enabled by connecting a capacitor from DITH to AGND. Figure 23 illustrates the dithering circuit. A triangular waveform centered at 1.22 V is generated across the C_{DITH} capacitor. This triangular waveform modulates the oscillator frequency by $\pm 5\%$ of the nominal frequency set by the R_T resistor. The C_{DITH} capacitance value sets the rate of the low frequency modulation. A lower C_{DITH} capacitance will modulate the oscillator frequency at a faster rate than a higher capacitance. For the dithering circuit to effectively reduce peak EMI, the modulation rate must be much less than the oscillator frequency (F_{sw}). Equation 6 calculates the DITH pin capacitance required to set the modulation frequency, F_{MOD} . Connecting the DITH pin directly to AGND disables frequency dithering, and the internal oscillator operates at a fixed frequency set by the RT resistor. Dither is disabled when external SYNC is used.

$$C_{DITH} = \frac{10 \mu\text{A}}{F_{MOD} \times 0.24 \text{ V}} \quad (6)$$



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Figure 23. Dither Operation

8.3.10 Output Overvoltage Protection (OVP)

The LM5175-Q1 provides an output overvoltage protection (OVP) circuit that turns off the gate drives when the feedback voltage is 7.5% above the 0.8 V feedback reference voltage V_{REF} . Switching resumes once the output falls within 5% of V_{REF} .

Feature Description (continued)

8.3.11 Power Good (PGOOD)

PGOOD is an open drain output that is pulled low when the voltage at the FB pin is outside $-9\% / +10\%$ of the nominal 0.8-V reference voltage. The PGOOD internal N-Channel MOSFET pull-down strength is typically 4.2 mA. This pin can be connected to a voltage supply of up to 8 V through a pull-up resistor.

8.3.12 Gm Error Amplifier

The LM5175-Q1 has a gm error amplifier for loop compensation. The gm amplifier output (COMP) range is 0.3 V to 3 V. Connect an R_{c1} - C_{c1} compensation network between COMP and ground for type II (PI) compensation (see [Figure 24](#)). Another pole is usually added using C_{c2} to suppress higher frequency noise.

The COMP output voltage (V_{COMP}) range limits the possible V_{IN} and I_{OUT} range for a given design. In buck mode, the maximum V_{IN} for which the converter can regulate the output at no load is when V_{COMP} reaches 0.3 V. [Equation 7](#) gives V_{COMP} as a function of V_{IN} at no load in CCM buck mode:

$$V_{COMP(BUCK)} = 1.6 \text{ V} - A_{CS} \cdot R_{SENSE} \cdot \frac{V_{OUT}}{2 \cdot L_1 \cdot F_{sw}} \cdot (1 - D_{BUCK}) - \frac{2 \mu\text{S} \cdot (V_{IN} - V_{OUT}) + 6 \mu\text{A}}{C_{SLOPE} \cdot F_{sw}} \cdot (1 - D_{BUCK}) \quad (7)$$

Where D_{BUCK} in the equation [Equation 7](#) is the buck duty cycle given by:

$$D_{BUCK} = \frac{V_{OUT}}{V_{IN}} \quad (8)$$

A larger L_1 , lower slope ripple (higher C_{SLOPE}), smaller sense resistor (R_{SENSE}), and higher frequency can increase the maximum V_{IN} range for buck operation.

For boost mode, the minimum V_{IN} for which the converter can regulate the output at full load is when V_{COMP} reaches 3 V. [Equation 9](#) gives V_{COMP} as a function of V_{IN} in boost mode:

$$V_{COMP(BOOST)} = 1.6 \text{ V} + A_{CS} \cdot R_{SENSE} \cdot \left(I_{OUT} \cdot \frac{V_{OUT}}{V_{IN}} + \frac{V_{IN}}{2 \cdot L_1 \cdot F_{sw}} \cdot D_{BOOST} \right) + \frac{2 \mu\text{S} \cdot (V_{OUT} - V_{IN}) + 5 \mu\text{A}}{C_{SLOPE} \cdot F_{sw}} \cdot D_{BOOST} \quad (9)$$

Where D_{BOOST} in the [Equation 9](#) is the boost duty cycle given by:

$$D_{BOOST} = 1 - \frac{V_{IN}}{V_{OUT}} \quad (10)$$

A larger L_1 , lower slope ripple (higher C_{SLOPE}), smaller sense resistor (R_{SENSE}), and higher frequency can extend the minimum V_{IN} range for boost operation.

8.3.13 Integrated Gate Drivers

The LM5175-Q1 provides four N-channel MOSFET gate drivers: two floating high-side gate drivers at the HDRV1 and HDRV2 pins, and two ground referenced low-side drivers at the LDRV1 and LDRV2 pins. Each driver is capable of sourcing 1.5 A and sinking 2 A peak current. In buck operation, LDRV1 and HDRV1 are switched by the PWM controller while HDRV2 remains continuously on. In boost operation, LDRV2 and HDRV2 are switched while HDRV1 remains continuously on.

In DCM buck operation, LDRV1 and HDRV2 turn off when the inductor current drops to zero (diode emulation). In a DCM boost operation, HDRV2 turns off when inductor current drops to zero.

The gate drive output HDRV2 remains off during soft-start to prevent reverse current flow from a pre-biased output.

The low-side gate drivers are powered from VCC and the high-side gate drivers HDRV1 and HDRV2 are powered from bootstrap capacitors C_{BOOT1} (between BOOT1 and SW1) and C_{BOOT2} (between BOOT2 and SW2) respectively. The C_{BOOT1} and C_{BOOT2} capacitors are charged through external Schottky diodes connected to the VCC pin as shown in [Figure 24](#).

Feature Description (continued)

8.3.14 Thermal Shutdown

The LM5175-Q1 is protected by a thermal shutdown circuit that shuts down the device when the internal junction temperature exceeds 165°C (typical). The soft-start capacitor is discharged when thermal shutdown is triggered and the gate drivers are disabled. The converter automatically restarts when the junction temperature drops by the thermal shutdown hysteresis of 15°C below the thermal shutdown threshold.

8.4 Device Functional Modes

Please refer to [Enable/UVLO](#) section for the description of EN/UVLO pin function. [Shutdown, Standby, and Operating Modes](#) section lists the shutdown, standby, and operating modes for LM5175-Q1 as a function of EN/UVLO and VCC voltages.

8.4.1 Shutdown, Standby, and Operating Modes

EN/UVLO	VCC	DEVICE MODE
EN/UVLO < 0.7 V	—	Shutdown: VCC off, No switching
0.7 V < EN/UVLO < 1.23 V	—	Standby: VCC on, No switching
EN/UVLO > 1.23 V	VCC < 3.3 V	Standby: VCC on, No switching
EN/UVLO > 1.23 V	VCC > 3.3 V	Operating: VCC on, Switching enabled

8.4.2 MODE Pin Configuration

The MODE pin is used to select CCM/DCM operation and hiccup mode current limit. Mode is latched at startup.

MODE PIN CONNECTION	LIGHT LOAD MODE	HICCUP FAULT PROTECTION
Connect to VCC	CCM	No Hiccup
RMODE to AGND = 93.1 kΩ	CCM	Hiccup Enabled
RMODE to AGND = 49.9 kΩ	DCM	Hiccup Enabled
Connect to AGND	DCM	No Hiccup

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM5175-Q1 is a four-switch buck-boost controller. A quick-start tool on the LM5175-Q1 product webpage can be used to design a buck-boost converter using the LM5175-Q1. Alternatively, Webench® software can create a complete buck-boost design using the LM5175-Q1 and generate bill of materials, estimate efficiency, solution size, and cost of the complete solution. The following sections describe a detailed step-by-step design procedure for a typical application circuit.

9.2 Typical Application

A typical application example is a buck-boost converter operating from a wide input voltage range of 6 V to 36 V and providing a stable 12 V output voltage with current capability of 6 A.

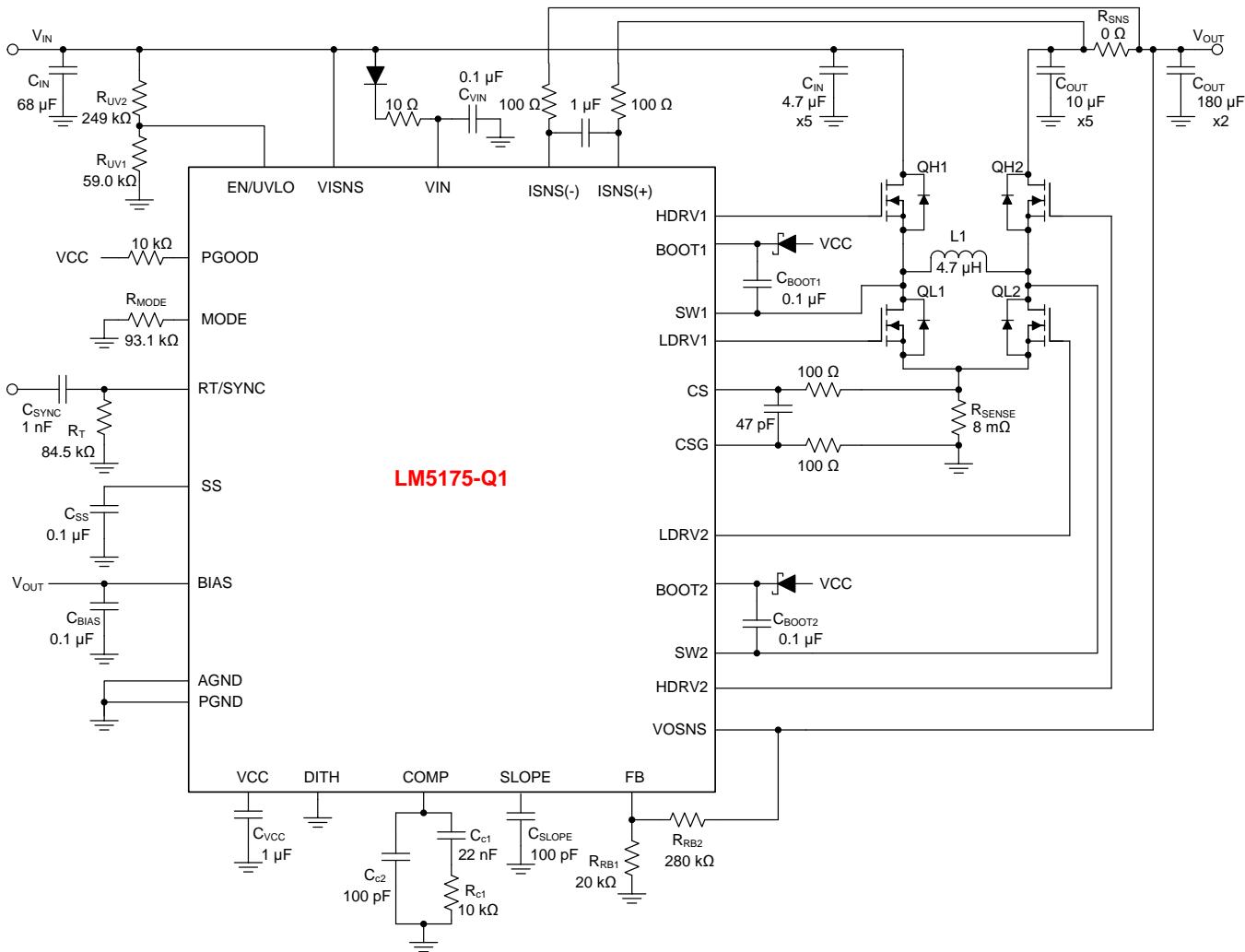


Figure 24. LM5175-Q1 Four-Switch Buck Boost Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

For this design example, the following are used as the input parameters.

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	6 V to 36 V
Output	12 V
Load Current	6 A
Switching Frequency	300 kHz
Mode	CCM, Hiccup

9.2.2 Detailed Design Procedure

9.2.2.1 Frequency

The switching frequency of LM5175-Q1 is set by an R_T resistor connected from RT/SYNC pin to AGND. The R_T resistor required to set the desired frequency is calculated using [Equation 5](#) or [Figure 3](#). A 1% standard resistor of 84.5 k Ω is selected for $F_{sw} = 300$ kHz.

9.2.2.2 V_{OUT}

The output voltage is set using a resistor divider to the FB pin. The internal reference voltage is 0.8 V. Normally the bottom resistor in the resistor divider is selected to be in the 1 k Ω to 100 k Ω range. Select

$$R_{FB1} = 20 \text{ k}\Omega \quad (11)$$

The top resistor in the feedback resistor divider is selected using [Equation 12](#):

$$R_{FB2} = \frac{V_{OUT} - 0.8 \text{ V}}{0.8 \text{ V}} \times R_{FB1} = 280 \text{ k}\Omega \quad (12)$$

9.2.2.3 Inductor Selection

The inductor selection is based on consideration of both buck and boost modes of operation. For the buck mode, inductor selection is based on limiting the peak to peak current ripple ΔI_L to ~40% of the maximum inductor current at the maximum input voltage. The target inductance for the buck mode is:

$$L_{BUCK} = \frac{(V_{IN(MAX)} - V_{OUT}) \times V_{OUT}}{0.4 \times I_{OUT(MAX)} \times F_{sw} \times V_{IN(MAX)}} = 11.1 \mu\text{H} \quad (13)$$

For the boost mode, the inductor selection is based on limiting the peak to peak current ripple ΔI_L to ~40% of the maximum inductor current at the minimum input voltage. The target inductance for the boost mode is:

$$L_{BOOST} = \frac{V_{IN(MIN)}^2 \times (V_{OUT} - V_{IN(MIN)})}{0.4 \times I_{OUT(MAX)} \times F_{sw} \times V_{OUT}^2} = 2.1 \mu\text{H} \quad (14)$$

In this particular application, the buck inductance is larger. Choosing a larger inductance reduces the ripple current but also increases the size of the inductor. A larger inductor also reduces the achievable bandwidth of the converter by moving the right half plane zero to lower frequencies. Therefore a judicious compromise should be made based on the application requirements. For this design a 4.7- μH inductor is selected. With this inductor selection, the inductor current ripple is 5.7 A, 4.3 A, and 2.1 A, at V_{IN} of 36 V, 24 V, and 6 V respectively.

The maximum average inductor current occurs at the minimum input voltage and maximum load current:

$$I_{L(MAX)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{0.9 \times V_{IN(MIN)}} = 13.3 \text{ A} \quad (15)$$

where a 90% efficiency is assumed. The peak inductor current occurs at minimum input voltage and is given by:

$$I_{L(PEAK)} = I_{L(MAX)} + \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{2 \times L_1 \times F_{sw} \times V_{OUT}} = 14.4 \text{ A} \quad (16)$$

To ensure sufficient output current, the current limit threshold must be set to allow the maximum load current in boost operation. To ensure that the inductor does not saturate in current limit, the peak saturation current of the inductor should be higher than the maximum current limit. Adjusting for a $\pm 20\%$ current limit threshold tolerance, the peak inductor current limit is:

$$I_{L(SAT)} = \frac{1.2 \times I_{L(Peak)}}{0.8} = 21.6 \text{ A} \quad (17)$$

Therefore, the inductor saturation current should be greater than 21.6 A. If hiccup mode protection is not enabled, the RMS current rating of the inductor should be sufficient to tolerate continuous operation in cycle-by-cycle current limiting.

9.2.2.4 Output Capacitor

In the boost mode, the output capacitor conducts high ripple current. The output capacitor RMS ripple current is given by [Equation 18](#) where the minimum V_{IN} corresponds to the maximum capacitor current.

$$I_{COUT(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} - 1} \quad (18)$$

In this example the maximum output ripple RMS current is $I_{COUT(RMS)} = 6$ A. A 5-mΩ output capacitor ESR causes an output ripple voltage of 60 mV as given by:

$$\Delta V_{RIPPLE(ESR)} = \frac{I_{OUT} \times V_{OUT}}{V_{IN(MIN)}} \times ESR \quad (19)$$

A 400 μF output capacitor causes a capacitive ripple voltage of 25 mV as given by:

$$\Delta V_{RIPPLE(COUT)} = \frac{I_{OUT} \times \left(1 - \frac{V_{IN(MIN)}}{V_{OUT}}\right)}{C_{OUT} \times F_{sw}} \quad (20)$$

Typically a combination of ceramic and bulk capacitors is needed to provide low ESR and high ripple current capacity. The complete schematic in [Figure 24](#) at the end of this section shows a good starting point for C_{OUT} for typical applications.

9.2.2.5 Input Capacitor

In the buck mode, the input capacitor supplies high ripple current. The RMS current in the input capacitor is given by:

$$I_{CIN(RMS)} = I_{OUT} \sqrt{D \times (1-D)} \quad (21)$$

The maximum RMS current occurs at $D = 0.5$, which gives $I_{CIN(RMS)} = I_{OUT}/2 = 3$ A. A combination of ceramic and bulk capacitors should be used to provide short path for high di/dt current and to reduce the output voltage ripple. The complete schematic in [Figure 24](#) is a good starting point for C_{IN} for typical applications.

9.2.2.6 Sense Resistor (R_{SENSE})

The current sense resistor between the CS and CSG pins should be selected to ensure that current limit is set high enough for both buck and boost modes of operation. For the buck operation, the current limit resistor is given by:

$$R_{SENSE(BUCK)} = \frac{76 \text{ mV} \times 70\%}{I_{OUT(MAX)}} = 8.8 \text{ m}\Omega \quad (22)$$

For the boost mode of operation, the current limit resistor is given by:

$$R_{SENSE(BOOST)} = \frac{160 \text{ mV} \times 70\%}{I_{L(Peak)}} = 7.7 \text{ m}\Omega \quad (23)$$

The closest standard value of $R_{SENSE} = 8 \text{ m}\Omega$ is selected based on the boost mode operation.

The maximum power dissipation in R_{SENSE} happens at $V_{IN(MIN)}$:

$$P_{RSENSE(MAX)} = \left(\frac{160 \text{ mV}}{R_{SENSE}} \right)^2 \cdot R_{SENSE} \cdot \left(1 - \frac{V_{IN(MIN)}}{V_{OUT}} \right) = 1.7 \text{ W} \quad (24)$$

Based on this, select the current sense resistor with power rating of 2 W or higher.

For some application circuits, it may be required to add a filter network to attenuate noise in the CS and CSG sense lines. Please see [Figure 24](#) for typical values. The filter resistance should not exceed 100Ω .

9.2.2.7 Slope Compensation

For stable current loop operation and to avoid sub-harmonic oscillations, the slope capacitor should be selected based on [Equation 25](#):

$$C_{SLOPE} = g_{m,SLOPE} \times \frac{L1}{R_{SENSE} \times A_{CS}} = 2 \mu\text{S} \times \frac{4.7 \mu\text{H}}{8 \text{ m}\Omega \times 5} = 235 \text{ pF} \quad (25)$$

This slope compensation results in “dead-beat” operation, in which the current loop disturbances die out in one switching cycle. Theoretically a current mode loop is stable with half the “dead-beat” slope (twice the calculated slope capacitor value in [Equation 25](#)). A smaller slope capacitor results in larger slope signal which is better for noise immunity in the transition region ($V_{IN} \sim V_{OUT}$). A larger slope signal, however, restricts the achievable input voltage range for a given output voltage, switching frequency, and inductor. For this design $C_{SLOPE} = 100 \text{ pF}$ is selected for better transition region behavior while still providing the required V_{IN} range. This selection of slope capacitor, inductor, switching frequency, and inductor satisfies the COMP range limitation explained in [Gm Error Amplifier](#) section.

9.2.2.8 UVLO

The UVLO resistor divider must be designed for turn-on below 6V. Selecting a $R_{UV2} = 249 \text{ k}\Omega$ gives a UVLO hysteresis of 0.8 V. The lower UVLO resistor is selected using [Equation 26](#):

$$R_{UV1} = \frac{R_{UV2} \times 1.23 \text{ V}}{V_{IN(UV)} + 1.5 \mu\text{A} \times R_{UV2} - 1.23 \text{ V}} = 59.5 \text{ k}\Omega \quad (26)$$

A standard value of $59.0 \text{ k}\Omega$ is selected for R_{UV1} .

When programming the UVLO threshold for lower input voltage operation, it is important to choose MOSFETs with gate (Miller) plateau voltage lower than the minimum V_{IN} .

9.2.2.9 Soft-Start Capacitor

The soft-start time is programmed using the soft-start capacitor. The relationship between C_{SS} and the soft-start time is given by:

$$t_{ss} = \frac{0.8 \text{ V} \times C_{SS}}{5 \mu\text{A}} \quad (27)$$

$C_{SS} = 0.1 \mu\text{F}$ gives a soft-start time of 16 ms.

9.2.2.10 Dither Capacitor

The dither capacitor sets the modulation frequency of the frequency dithering around the nominal switching frequency. A larger C_{DITH} results in lower modulation frequency. For proper operation the modulation frequency (F_{MOD}) must be much lower than the switching frequency. Use [Equation 28](#) to select C_{DITH} for the target modulation frequency.

$$C_{DITH} = \frac{10 \mu\text{A}}{F_{MOD} \times 0.24 \text{ V}} \quad (28)$$

For the current design dithering is not being implemented. Therefore a 0Ω resistor from the DITH pin to AGND disables this feature.

9.2.2.11 MOSFETs QH1 and QL1

The input side MOSFETs QH1 and QL1 need to withstand the maximum input voltage of 36 V. In addition they must withstand the transient spikes at SW1 during switching. Therefore QH1 and QL1 should be rated for 60 V. The gate plateau voltages of the MOSFETs should be smaller than the minimum input voltage of the converter, otherwise the MOSFETs may not fully enhance during startup or overload conditions.

The power loss in QH1 in the boost mode of operation is approximated by:

$$P_{COND(QH1)} = \left(I_{OUT} \cdot \frac{V_{OUT}}{V_{IN}} \right)^2 \cdot R_{DSON(QH1)} \quad (29)$$

The power loss in QH1 in the buck mode of operation consists of both conduction and switching loss components given by [Equation 30](#) and [Equation 31](#) respectively:

$$P_{COND(QH1)} = \left(\frac{V_{OUT}}{V_{IN}} \right) \cdot I_{OUT}^2 \cdot R_{DSON(QH1)} \quad (30)$$

$$P_{SW(QH1)} = \frac{1}{2} \cdot V_{IN} \cdot I_{OUT} \cdot (t_r + t_f) \cdot F_{sw} \quad (31)$$

The rise (t_r) and the fall (t_f) times are based on the MOSFET datasheet information or measured in the lab. Typically a MOSFET with smaller R_{DSON} (smaller conduction loss) will have longer rise and fall times (larger switching loss).

The power loss in QL1 in the buck mode of operation is given by the following equation:

$$P_{COND(QL1)} = \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \cdot I_{OUT}^2 \cdot R_{DSON(QL1)} \quad (32)$$

9.2.2.12 MOSFETs QH2 and QL2

The output side MOSFETs QH2 and QL2 see the output voltage of 12 V and additional transient spikes at SW2 during switching. Therefore QH2 and QL2 should be rated for 20 V or more. The gate plateau voltages of the MOSFETs should be smaller than the minimum input voltage of the converter, otherwise the MOSFETs may not fully enhance during startup or overload conditions.

The power loss in QH2 in the buck mode of operation is approximated by:

$$P_{COND(QH2)} = I_{OUT}^2 \cdot R_{DSON(QH2)} \quad (33)$$

The power loss in QL2 in the boost mode of operation consists of both conduction and switching loss components given by [Equation 34](#) and [Equation 35](#) respectively:

$$P_{COND(QL2)} = \left(1 - \frac{V_{IN}}{V_{OUT}} \right) \cdot \left(I_{OUT} \cdot \frac{V_{OUT}}{V_{IN}} \right)^2 \cdot R_{DSON(QL2)} \quad (34)$$

$$P_{SW(QL2)} = \frac{1}{2} \cdot V_{OUT} \cdot \left(I_{OUT} \cdot \frac{V_{OUT}}{V_{IN}} \right) \cdot (t_r + t_f) \cdot F_{sw} \quad (35)$$

The rise (t_r) and the fall (t_f) times can be based on the MOSFET datasheet information or measured in the lab. Typically a MOSFET with smaller R_{DSON} (lower conduction loss) has longer rise and fall times (larger switching loss).

The power loss in QH2 in the boost mode of operation is given by the following equation:

$$P_{COND(QH2)} = \frac{V_{IN}}{V_{OUT}} \cdot \left(I_{OUT} \cdot \frac{V_{OUT}}{V_{IN}} \right)^2 \cdot R_{DSON(QH2)} \quad (36)$$

9.2.2.13 Frequency Compensation

This section presents the control loop compensation design procedure for the LM5175-Q1 buck-boost controller. The LM5175-Q1 operates mainly in buck or boost modes, separated by a transition region, and therefore the control loop design is done for both buck and boost operating modes. Then a final selection of compensation is made based on the mode that is more restrictive from a loop stability point of view. Typically for a converter designed to go deep into both buck and boost operating regions, the boost compensation design is more restrictive due to the presence of a right half plane zero (RHPZ) in the boost mode.

The boost power stage output pole location is given by:

$$f_{p1(\text{boost})} = \frac{1}{2\pi} \left(\frac{2}{R_{\text{OUT}} \times C_{\text{OUT}}} \right) = 398 \text{ Hz} \quad (37)$$

where $R_{\text{OUT}} = 2 \Omega$ corresponds to the maximum load of 6 A.

The boost power stage ESR zero location is given by:

$$f_{z1} = \frac{1}{2\pi} \left(\frac{1}{R_{\text{ESR}} \times C_{\text{OUT}}} \right) = 79.6 \text{ kHz} \quad (38)$$

The boost power stage RHP zero location is given by:

$$f_{\text{RHP}} = \frac{1}{2\pi} \left(\frac{R_{\text{OUT}} \times (1 - D_{\text{MAX}})^2}{L_1} \right) = 16.9 \text{ kHz} \quad (39)$$

where D_{MAX} is the maximum duty cycle at the minimum V_{IN} .

The buck power stage output pole location is given by:

$$f_{p1(\text{buck})} = \frac{1}{2\pi} \left(\frac{1}{R_{\text{OUT}} \times C_{\text{OUT}}} \right) = 199 \text{ Hz} \quad (40)$$

The buck power stage ESR zero location is the same as the boost power stage ESR zero.

It is clear from [Equation 39](#) that RHP zero is the main factor limiting the achievable bandwidth. For a robust design the crossover frequency should be less than 1/3 of the RHP zero frequency. Given the position of the RHP zero, a reasonable target bandwidth in boost operation is around 4 kHz:

$$f_{\text{bw}} = 4 \text{ kHz} \quad (41)$$

For some power stages, the boost RHP zero might not be as restrictive. This happens when the boost maximum duty cycle (D_{MAX}) is small, or when a really small inductor is used. In those cases, compare the limits posed by the RHP zero ($f_{\text{RHP}}/3$) with 1/20 of the switching frequency and use the smaller of the two values as the achievable bandwidth.

The compensation zero can be placed at 1.5 times the boost output pole frequency. Keep in mind that this locates the zero at 3 times the buck output pole frequency which results in approximately 30 degrees of phase loss before crossover of the buck loop and 15 degrees of phase loss at intermediate frequencies for the boost loop:

$$f_{\text{zc}} = 600 \text{ Hz} \quad (42)$$

If the crossover frequency is well below the RHP zero and the compensation zero is placed well below the crossover, the compensation gain resistor R_{c1} is calculated using the approximation:

$$R_{\text{c1}} = \frac{2\pi \times f_{\text{bw}}}{\text{gm}_{\text{EA}}} \times \frac{R_{\text{FB1}} + R_{\text{FB2}}}{R_{\text{FB1}}} \times \frac{A_{\text{CS}} \times R_{\text{SENSE}} \times C_{\text{OUT}}}{1 - D_{\text{MAX}}} = 9.49 \text{ k}\Omega \quad (43)$$

where D_{MAX} is the maximum duty cycle at the minimum V_{IN} in boost mode and A_{CS} is the current sense amplifier gain. The compensation capacitor C_{c1} is then calculated from:

$$C_{\text{c1}} = \frac{1}{2 \times \pi \times f_{\text{zc}} \times R_{\text{c1}}} = 27.9 \text{ nF} \quad (44)$$

The standard values of compensation components are selected to be $R_{\text{c1}} = 10 \text{ k}\Omega$ and $C_{\text{c1}} = 22 \text{ nF}$.

A high frequency pole is added to suppress switching noise using a 100 pF capacitor (C_{c2}) in parallel with R_{c1} and C_{c1} . These values provide a good starting point for the compensation design. Each design should be tuned in the lab to achieve the desired balance between stability margin across the operating range and transient response time.

9.2.3 Application Curves

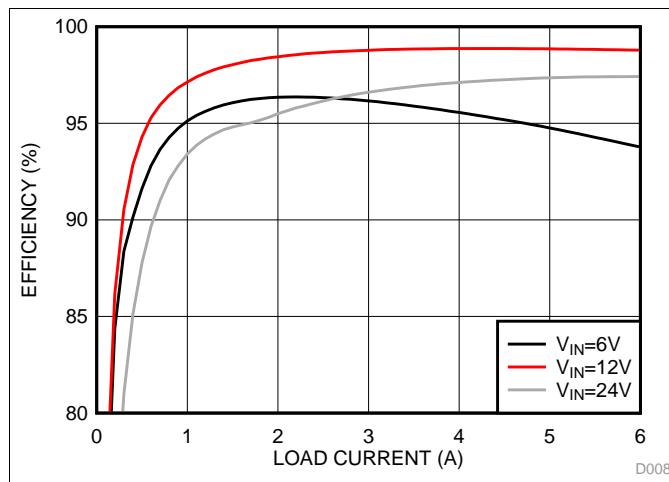


Figure 25. Efficiency vs Load

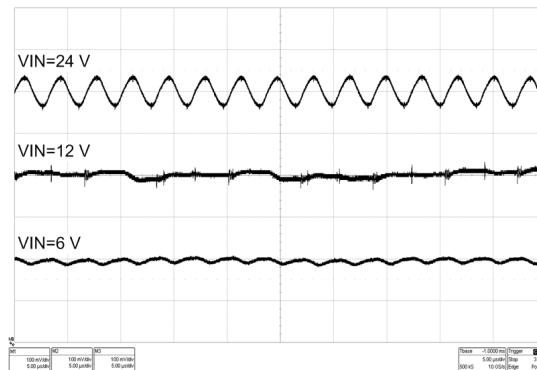


Figure 26. Output Voltage Ripple

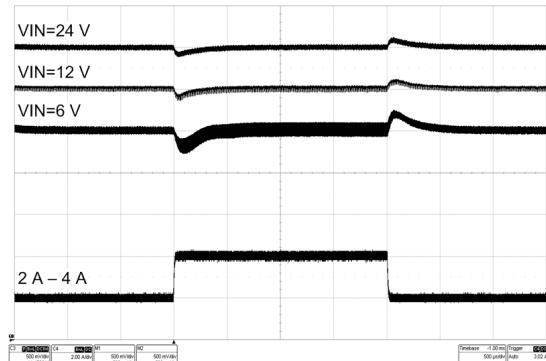


Figure 27. Load Transient Response

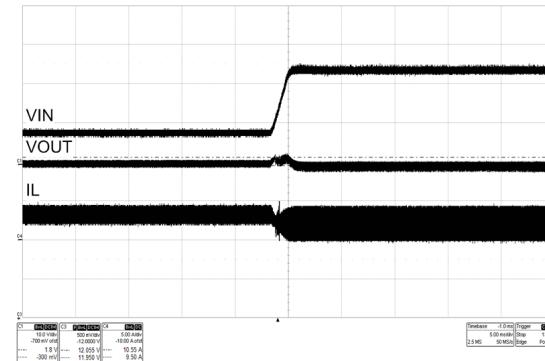


Figure 28. Line Transient Response (8 V – 24 V, $I_{OUT} = 2$ A)

10 Power Supply Recommendations

The LM5175-Q1 is a power management device. The power supply for the device is any dc voltage source within the specified input range. The supply should also be capable of supplying sufficient current based on the maximum inductor current in boost mode operation. The input supply should be bypassed with additional electrolytic capacitor at the input of the application board to avoid ringing due to parasitic impedance of the connecting cables.

11 Layout

11.1 Layout Guidelines

The basic PCB board layout requires separation of sensitive signal and power paths. The following checklist should be followed to get good performance for a well designed board.

- Place the power components including the input filter capacitor C_{IN} , the power MOSFETs QL1 and QH1, and the sense resistor R_{SENSE} close together to minimize the loop area for input switching current in buck operation.
- Place the power components including the output filter capacitor C_{OUT} , the power MOSFETs QL2 and QH2, and the sense resistor R_{SENSE} close together to minimize the loop area for output switching current in boost operation.
- Use a combination of bulk capacitors and smaller ceramic capacitors with low series impedance for the input and output capacitors. Place the smaller capacitors closer to the IC to provide a low impedance path for high di/dt switching currents.
- Minimize the SW1 and SW2 loop areas as these are high dv/dt nodes.
- Layout the gate drive traces and return paths as directly as possible. Layout the forward and return traces close together, either running side by side or on top of each other on adjacent layers to minimize the inductance of the gate drive path.
- Use Kelvin connections to R_{SENSE} for the current sense signals CS and CSG and run lines in parallel from the R_{SENSE} terminals to the IC pins. Avoid crossing noisy areas such as SW1 and SW2 nodes or high-side gate drive traces. Place the filter capacitor for the current sense signal as close to the IC pins as possible.
- Place the C_{IN} , C_{OUT} , and R_{SENSE} ground pins as close as possible with thick ground trace and/or planes on multiple layers.
- Place the VCC bypass capacitor close to the controller IC, between the VCC and PGND pins. A 1- μ F ceramic capacitor is typically used.
- Place the BIAS bypass capacitor close to the controller IC, between the BIAS and PGND pins. A 0.1- μ F ceramic capacitor is typically used.
- Place the BOOT1 bootstrap capacitor close to the IC and connect directly to the BOOT1 to SW1 pins.
- Place the BOOT2 bootstrap capacitor close to the IC and connect directly to the BOOT2 to SW2 pins.
- Bypass the V_{IN} pin to AGND with a low ESR ceramic capacitor located close to the controller IC. A 0.1 μ F ceramic capacitor is typically used. When using external BIAS, use a diode between input rails and V_{IN} pins to prevent reverse conduction when $V_{IN} < VCC$.
- Connect the feedback resistor divider between the C_{OUT} positive terminal and AGND pin of the IC. Place the components close to the FB pin.
- Use care to separate the power and signal paths so that no power or switching current flows through the AGND connections which can either corrupt the COMP, SLOPE, or SYNC signals, or cause dc offset in the FB sense signal. The PGND and AGND traces can be connected near the PGND pin, near the VCC capacitor PGND connection, or near the PGND connection of the CS, CSG pin current sense resistor.
- When using the average current loop, divide the overall capacitor (C_{IN} or C_{OUT}) between the two sides of the sense resistor to ensure small cycle-by-cycle ripple. Place the average current loop filter capacitor close to the IC between the ISNS(+) and ISNS(-) pins.

11.2 Layout Example

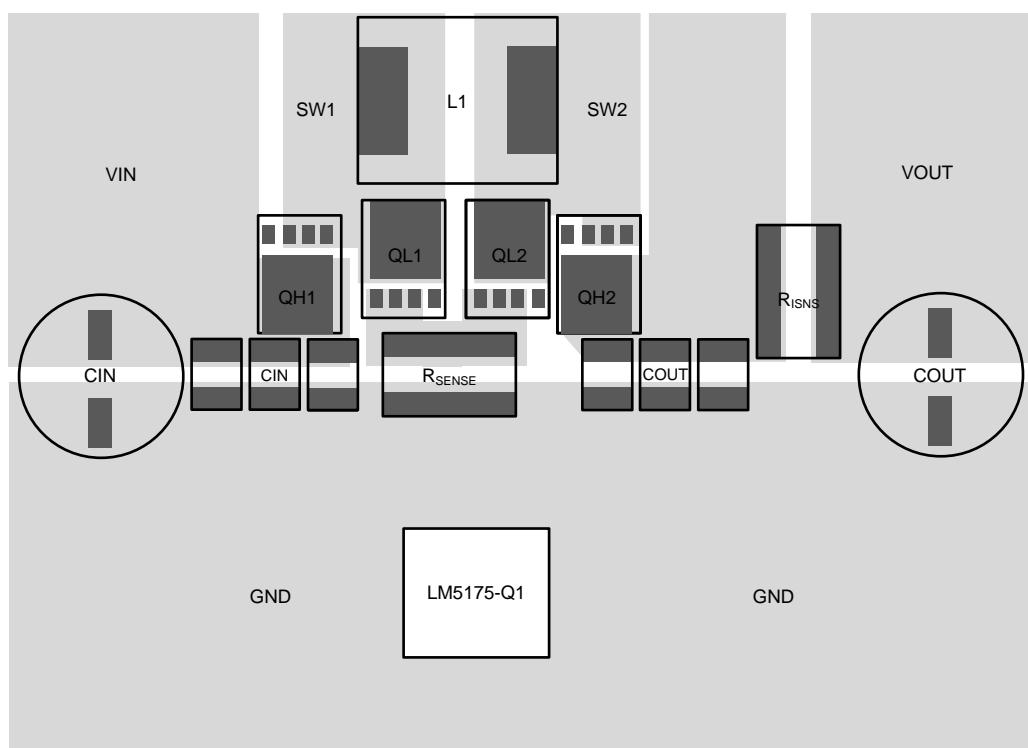


Figure 29. LM5175-Q1 Power Stage Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

Please visit TI homepage for latest technical document including application notes, user guides, and reference designs.

IC Package Thermal Metrics application report, [SPRA953](#).

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.

Webench is a registered trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Package Option Addendum

13.1.1 Packaging Information

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾	Op Temp (°C)	Device Marking ⁽⁴⁾⁽⁵⁾
LM5175QPWPRQ1	PREVIEW	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	LM5175Q
LM5175QPWPTQ1	PREVIEW	HTSSOP	PWP	28	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	LM5175Q

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5175QPWPRQ1	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	LM5175Q	Samples
LM5175QPWPTQ1	ACTIVE	HTSSOP	PWP	28	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	LM5175Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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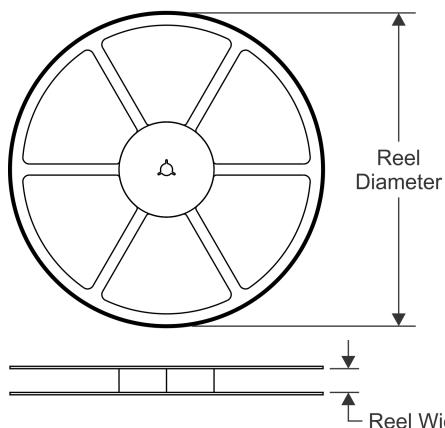
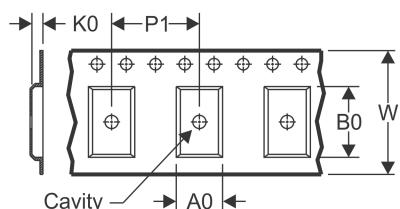
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OTHER QUALIFIED VERSIONS OF LM5175-Q1 :

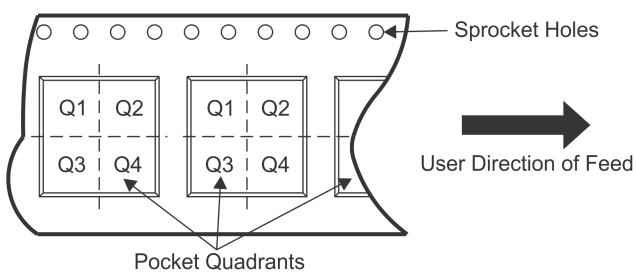
- Catalog: [LM5175](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

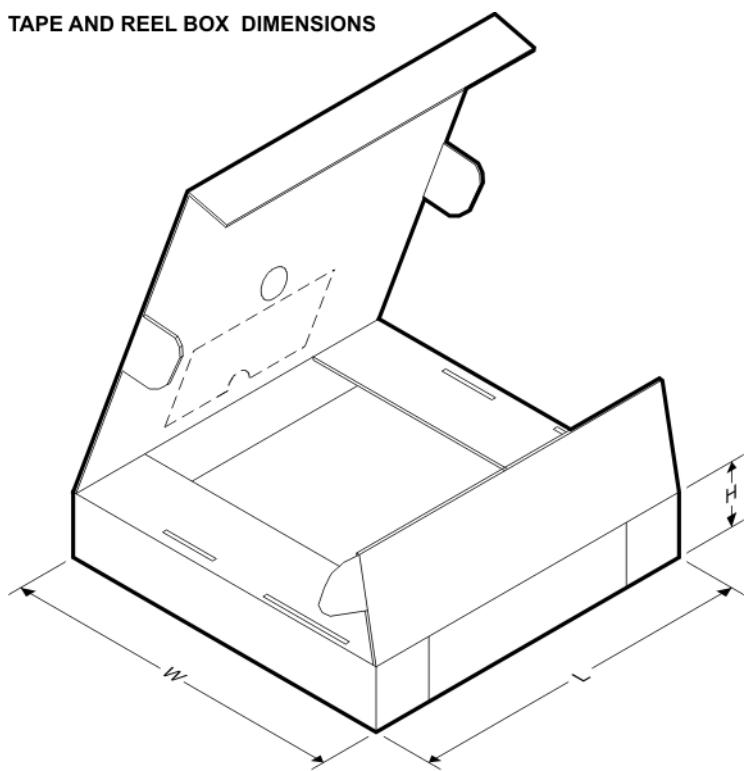
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5175QPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
LM5175QPWPTQ1	HTSSOP	PWP	28	250	180.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5175QPWPRQ1	HTSSOP	PWP	28	2000	367.0	367.0	38.0
LM5175QPWPTQ1	HTSSOP	PWP	28	250	213.0	191.0	55.0

PWP (R-PDSO-G28)

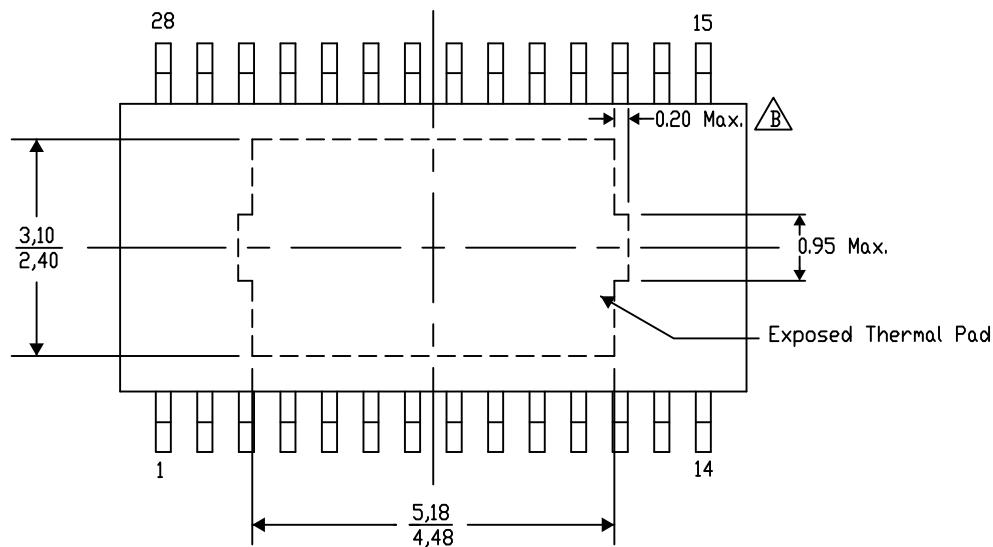
PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-38/AO 01/16

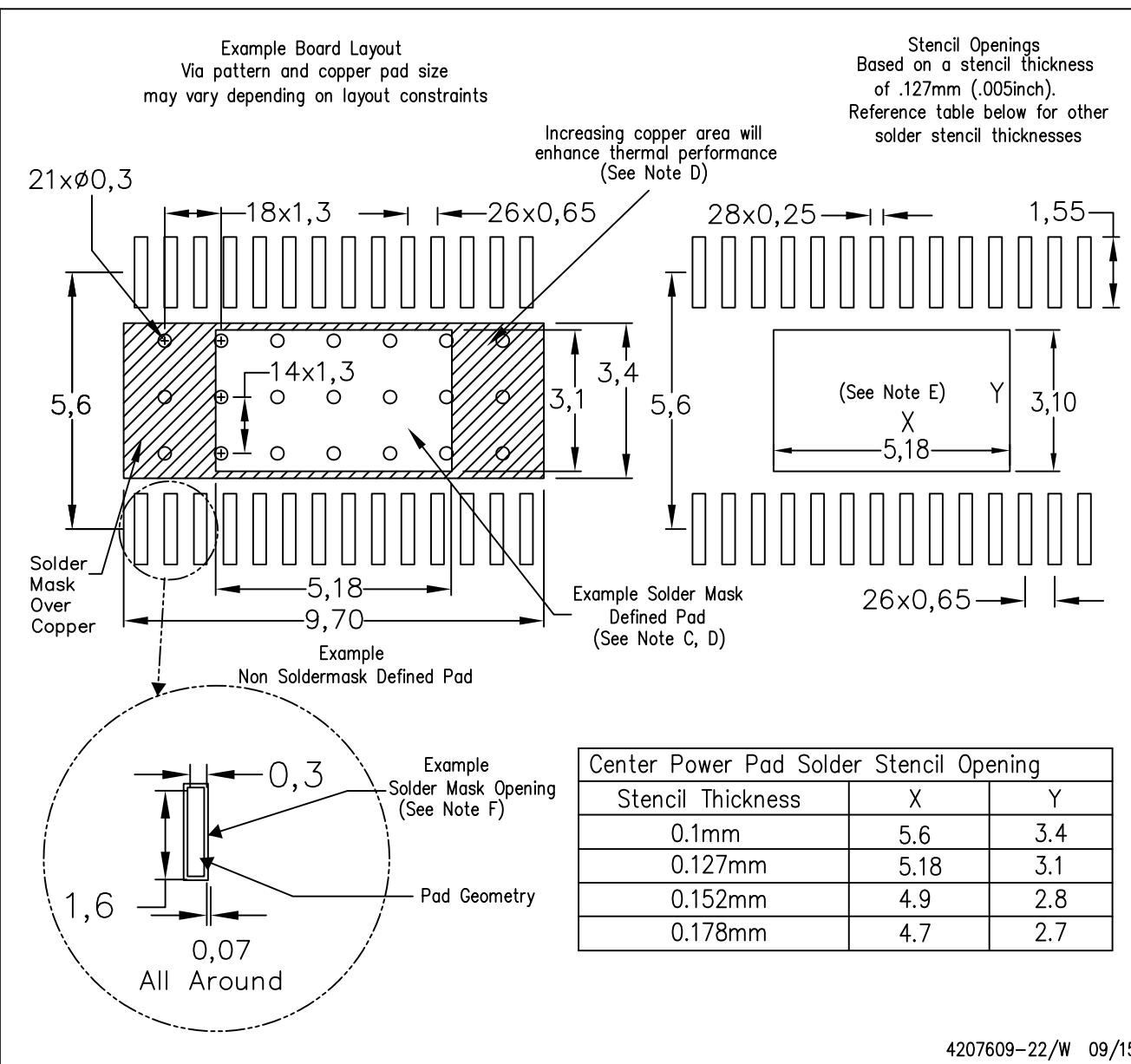
NOTE: A. All linear dimensions are in millimeters

 Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G28)

PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
- For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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