Application Report
SPRAC15–March 2016

Validating High Speed and Full Speed USB on the TMS320C5545 Device

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ABSTRACT

This application report describes the process to validate electrical requirements of high and full speed USB operations on the TMS320C5545 device.

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1 Introduction

The device high-speed electrical test procedure is comprised of a series of tests and related procedures developed by the USB 2.0 compliance committee to verify electrical requirements of high-speed USB operations designed to meet USB 2.0 specification. This application report outlines the test setup and captures the results of the series tests performed on the C5545Device.

2 Test Setup

Table 1 lists the test instruments used to perform the outlined series of tests.

Table 1. Texas Instruments

Type	Manufacturer	Product	Use
USB high-speed electrical test tool to be loaded on a test bed computer	USB-IF	USBHSET	To enumerate and send command
Oscilloscope	Tektronix	CSA 7404B	To measure USB signals
Differential probe	Tektronix	P6247	Signal quality/receiver sensitivity tests
Single-ended FET probe	Tektronix	P6245	Packet parameters/CHIRP timings
Measurement application (USB test software that is part of the scope application)	Tektronix	TDSUSBF	USB compliance test software specifically used for USB
Test fixture	Tektronix	TDSUSBF	For USB test
Pattern Generator	Agilent	81130A	To generate serial test data for receiver sensitivity test
Digital Multi-meter	Fluke	Fluke 45 Series	Measure voltage and current DP and
DM lines			
Test board	TI/Spectrum Digital	EVM	Test board used for C5545 USB validation

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2.1 Test Fixture

Figure 1 provides the test setup created for validating these tests.

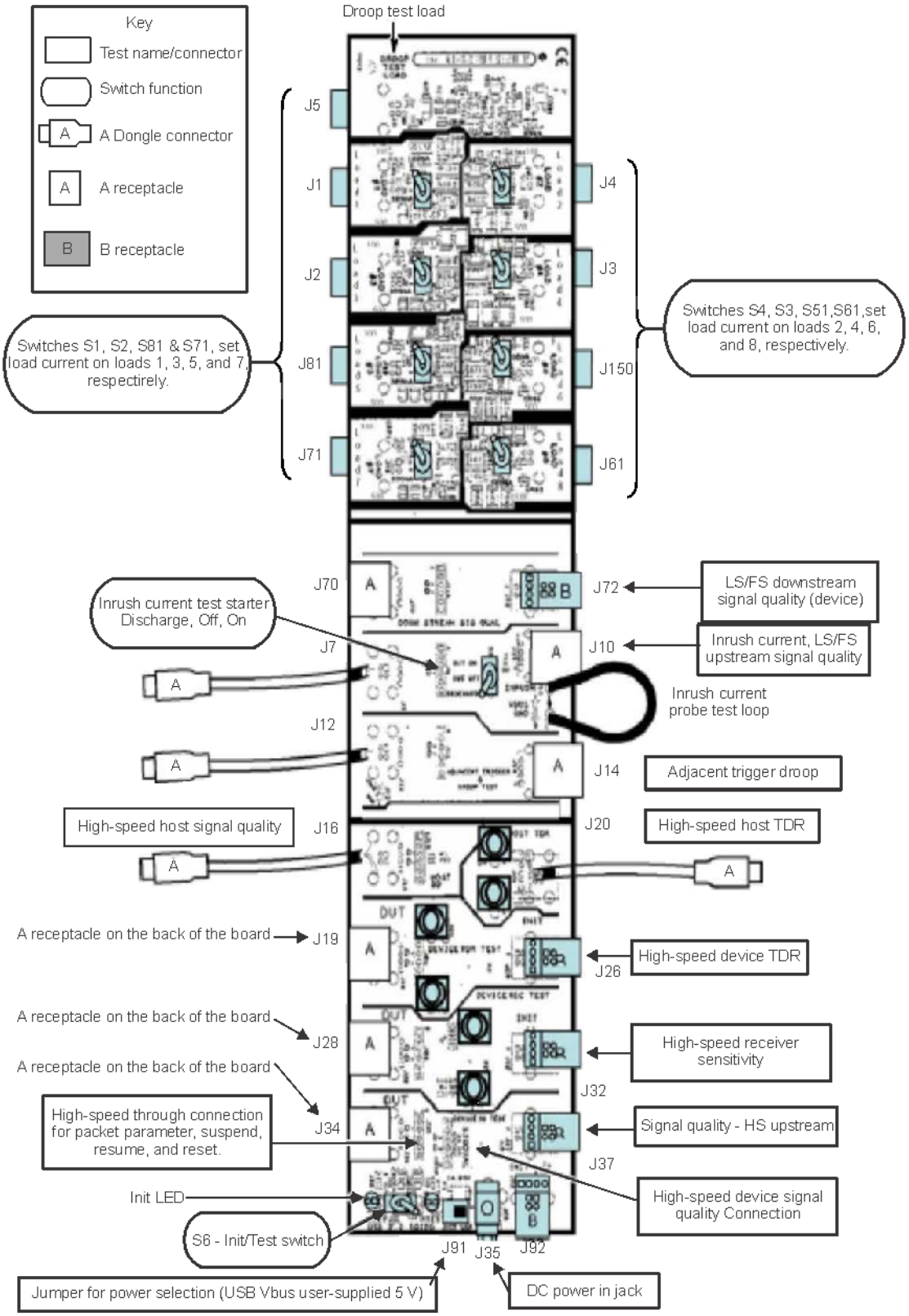

Figure 1. Test Fixture

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2.2 Test Setup USB High Speed Tests

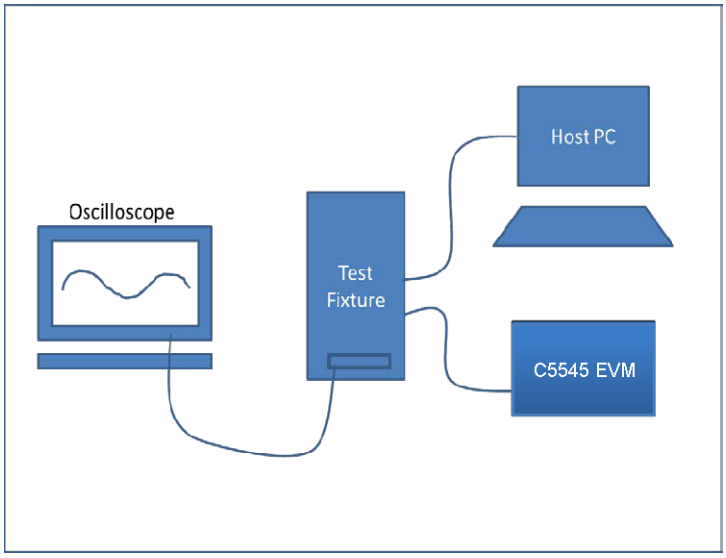

Figure 2. Test Setup

2.3 Test Condition

2.3.1 Power Supply

Table 2 mentions that voltages were supplied to USB during this tests.

Table 2. USB Power Supplies

Parameters		NOM	Unit
USB_VDD1P3	Supply voltage, Digital USB	1.3	V
USB_VDDA1P3	Supply voltage, 1.3 V Analog USB	1.3	V
USB_VDDA3P3	Supply voltage, I/O, 3.3 V Analog USB PHY	3.3	V

2.4 Test Items

Table 3 captures compliance tests and the results for each test that is performed. Further details on the tests are discussed in the following sections.

Table 3. USB Compliance Test Results

Test No	Test Items	Result
	High Speed Signal Quality Test	
USB_EL_2	HS Transmitter data rate 480 Mb/s ± 0.05%	PASSED
USB_EL_4	Signal quality test measured at the near end	PASSED
USB_EL_6	10% to 90% differential rise and fall time > 500ps	PASSED
USB_EL_7	Monotonic data transitions over the vertical openings in the appropriate EYE Pattern	PASSED
	Device Packet Parameters	
USB_EL_21	Synchronization (SYNC) field	PASSED
USB_EL_22	Inter-packet gap (delay between Host and device packet)	PASSED
USB_EL_25	End of packet (EOP) field	PASSED
	Chirp Timings	
USB_EL_28	Chirp reset time	PASSED

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Table 3. USB Compliance Test Results (continued)

Test No	Test Items	Result
USB_EL_29	Chirp-K duration	PASSED
USB_EL_31	Delay between last Host chirp and device disconnect 1.5 K pull-up resistor and enable termination	PASSED
Device Suspend/Resume/Reset Timing		
USB_EL_27	Chirp handshake generation while Host performing reset in the middle of idle (non-suspend HS mode)	PASSED
USB_EL_28	Chirp-K duration when reset is invoked from a suspended state	PASSED
USB_EL_38	Chirp reset time when reset is applied from a suspend state	PASSED
USB_EL_39	Device support for suspend state	PASSED
USB_EL_40	Device transitioning from suspend state to HS operation due to reaching the EOF	PASSED
Device SE0_NAK		
USB_EL_9	Test_SE0_NAK (controller responds to any valid IN token with a NAK)	PASSED
Device Receiver Sensitivity		
USB_EL_16	Device receiver level	PASSED
USB_EL_17	Device squelch level	PASSED
USB_EL_18	Device capability for locking PLL with 12-bit SYNC field	PASSED

The tests were performed with the below mentioned supply voltages.

Table 4. USB Supply Voltages

Parameters		NOM	Unit
USB_VDD1P3	Supply voltage, Digital USB	1.3	V
USB_VDDA1P3	Supply voltage, 1.3 V Analog USB	1.3	V
USB_VDDA3P3	Supply voltage, I/O, 3.3 V Analog USB PHY	3.3	V

3 USB High Speed Tests

This section provides information on the procedures followed to perform USB high speed tests and captures respective test results.

3.1 Device High-Speed Signal Quality (EL_2, EL_4, EL_5, EL_6, EL_7)

3.1.1 Procedure

The following EL_2, EL_4, EL_5, EL_6, EL_7 test procedures were followed:

Determine if the device under test incorporates a captive cable, or it has a normal series B or mini-B receptacle. Captive cable designs require the signal quality measurement to be made at the far end (hsfe). Detachable cable designs require the measurement to be made at the near end (hsne).

1. Turn on the oscilloscope and allow about 20 minutes for warm up.
2. Launch the TDSUSB software application on the oscilloscopes.
3. Press the Default Setup button on the oscilloscope front panel.
4. Select File → recall default in the applications menu bar.
5. Select the High Speed tab within the Measurement select menu of the USB2.0 compliance test application.
6. Select the High Speed Signal Quality tests → Eye Diagram, Signal Rate, Rise time, Fall Time, and EOP within the Signal Quality area of the application.

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NOTE: The Monotonic property test is available but not required as it may generate false failures due to slight variations in the signal edge due to high frequency noise and/or scope quantization error.

7. Press Configure on the application screen. Select upstream and far end for devices with captive cables or near end for devices without a captive cable.
8. Press the icon. Verify that the oscilloscope display is NOT reporting “clipping”. If it is, adjust the vertical amplitude until the “clipping” message does not appear. Do not press OK on the screen until the correct waveform is displayed.
9. Attach the USB cable to the designated power supply port of the compliance test fixture.
10. Verify that red Power LED and the red Init LED are lit.
11. Connect the upstream facing port of the device under test to USB connector of the Device SQ segment of the test fixture. Connect the Init port of the test fixture to a high-speed capable port of the test bed computer. Apply power to the device.
12. Attach the differential probe to of the test fixture. Ensure that the + polarity on the probe lines up with D+ on the fixture.
13. Invoke the High-speed Electrical Test Tool software on the High-speed Electrical Test Bed computer. The main menu appears and shows the USB2.0 host controller.
14. Select Device and click TEST to enter the HS Electrical Test Tool application → Device Test menu. The device under test should be enumerated with the device’s VID shown together with the root port in which it is connected.
15. Place the Test Switch (S6) in the TEST position. Verify that the red TEST LED is lit.
16. Using the oscilloscope, verify that test packets are being transmitted from the port under test. Adjust the trigger level as necessary. If a steady trigger cannot be obtained by adjusting the trigger level, try a slight change to the trigger hold off.
17. Once the test packet is displayed properly, press OK in the application dialog box.
18. The Tektronix USB application generally triggers and displays the correct test packet without the need to place cursors. Should cursors be required they can be enabled from the application by selecting, File → Preferences → Advanced and clicking the option “Packet Identification by user using Cursors”.
19. If cursors measurement is enabled (see step 17) on the oscilloscope, place the two vertical cursors around one test packet. Place one cursor just before the sync field (about one bit time) and the other cursor just (about one bit time) after the EOP (END OF PACKET). Press OK on the USB2 application dialog box to begin acquisition and analysis of the test packet.
20. Verify that the Signal Eye, EOP Width, Rise and fall time and Signaling Rate all pass. The results displayed on oscilloscope can also be recorded to an HTML report located on the oscilloscope hard drive at the following path: C:\TekApplications\tdsusb2\report.
21. Save all the report files created during the tests. The report contains the test result in EL_2, EL_4 or EL_5, EL_6 and EL_7.

NOTE: EL_4 and EL_5 requirements are mutually exclusive. If EL_4 is tested then EL_5 is not applicable, and vice versa.

22. Return the Test switch (S6) of the test fixture to the Normal position and verify the Red TEST LED is not lit. Recycle power of the device to prepare for subsequent tests.

3.1.2 C5545 Test Result - Device High-Speed Signal Quality (EL_2, EL_4, EL_5, EL_6, EL_7)

Signal Quality Test Results in Tek Format:

- **Device ID:** fsfe_001
- **Device Description:** High Speed, Near End Device, Up Stream Testing, Tier 1
- **Date:** Tue Nov 10 18:23:14 PST 2015
- **Overall Result:** Pass [(1)]

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(1) The Overall Result for this test is Pass, because one or more individual status of the measurements is Pass. For this test, the recommended configuration for USB2 testing (as per USB-IF) is on Tier 1.

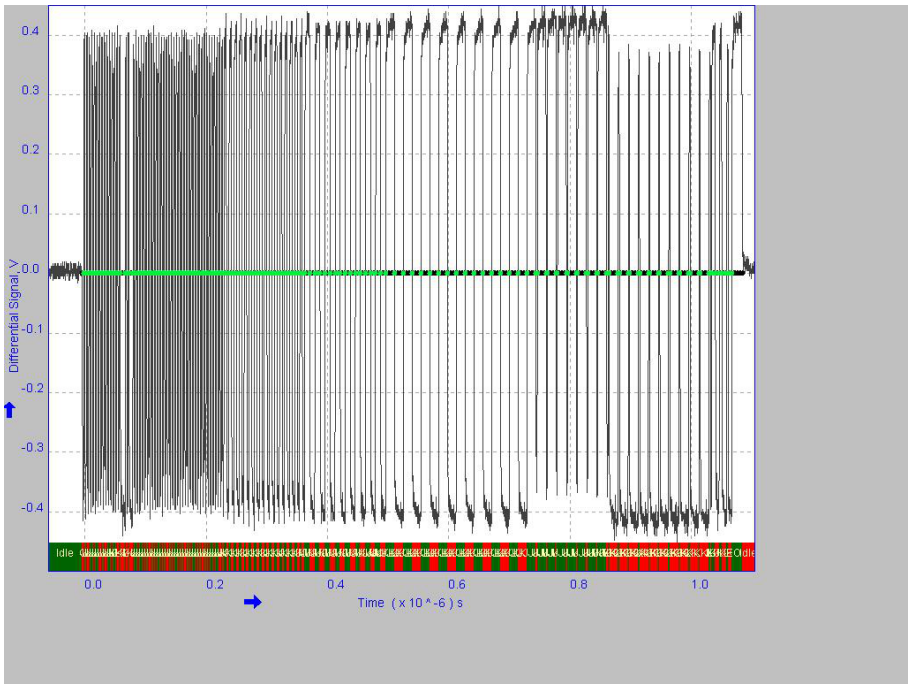

Figure 3. Waveform Plot

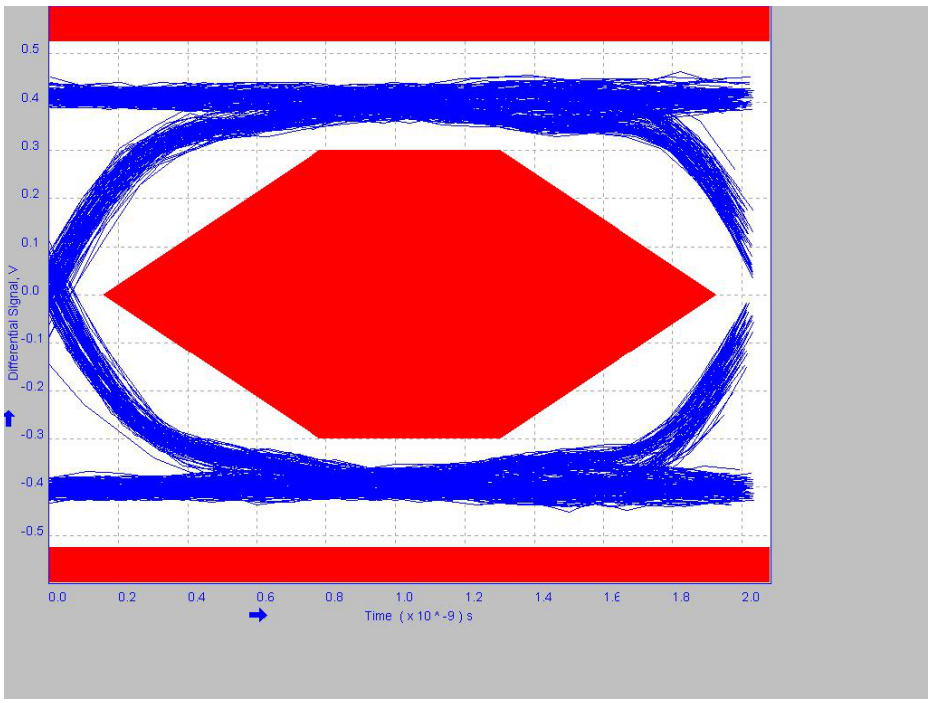

Figure 4. Eye Diagram

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Table 5. Results Based on USB-IF/Waiver Limits

Measurement Name	Minimum	Maximum	Mean	pk-pk	Standard Deviation	RMS	Population	Status
Eye Diagram Test	–	–	–	–	–	–	–	Pass
Signal Rate	469.0949 Mbps	493.1868 Mbps	479.9827 Mbps	0.0000 bps	5.683001 Mbps	480.1009 Mbps	513	Pass
EOP Width	–	–	16.78347 ns	–	–	–	1	Pass
EOP Width (Bits)	–	–	8.055774	–	–	–	1	Pass
Rise Time	696.9763 ps	1.190298 ns	937.9351 ps	493.3215 ps	110.9619 ps	944.4150 ps	107	Pass
Fall Time	670.6193 ps	1.117810 ns	900.2827 ps	447.1904 ps	96.44541 ps	905.3860 ps	107	Pass

Additional Information:

- Consecutive Jitter range: -63.29 ps to 79.47 ps RMS Jitter 30.28 ps
- KJ Paired Jitter range: -32.12 ps to 47.75 ps RMS Jitter 14.29 ps
- JK Paired Jitter range: -30.82 ps to 35.69 ps RMS Jitter 13.18 ps

3.2 Device Packet Parameters (EL_21, EL_22, EL_25)

3.2.1 Procedure

The following EL_21, EL_22, EL_25 test procedures were followed:

1. Connect the Init port of the Device Signal Quality test fixture into a high-speed capable port of the test bed computer.
2. Connect the upstream facing port of the device under test to the USB connector of the Device SQ segment of the test fixture. Connect the Init port of the test fixture to a high-speed capable port of the test bed computer. Apply power to the device. Verify that the device enumerates properly.

NOTE: The use of the Signal Quality segment of the compliance test fixture makes it possible to trigger on packets generated by the device because the differential probe is located closer to the device transmitter, hence the device packets are larger in amplitude.

3. Attach the differential probe to the fixture near the device connector. Ensure that the + polarity on the probe lines up with the D+ on the fixture.
4. Use the oscilloscope to verify that the Start Of Frame (SOF) packets are being transmitted on the port under test.
5. Select Packet Parameter measurement from the High-Speed tab and configure the device for EL_21, EL_22, and EL_25. Run the measurements.
6. Use the oscilloscope to verify that the SOF packets are being transmitted on the port under test.
7. In the HS Electrical Test Tool application → Device Test menu of the High-speed Electrical Test Tool application software, ensure that the device under test is selected (highlighted). Select SINGLE STEP SET FEATURE from the Device Command window and click EXECUTE once.
8. From the application menu, select Results → Summary. Click any of the test result buttons to get the details of that test.
9. The results consist of EL_22 inter-packet gap between the second (from host) and the third (from device in response to the host's) packets are shown on the oscilloscope. The second (of lower amplitude) is from the host and the third (of higher amplitude) is a device's response.
10. Select Packet Parameter measurement from the High-Speed tab and configure for device EL_22 and run the measurements.
11. Ensure that the oscilloscope is armed. In the HS Electrical Test Tool application → Device Test menu, click Step once. This is the second step of the two-step Single Step Set Feature command. The oscilloscope capture should appear as follows:

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12. The results consist of EL_22 inter-packet gap between the first (from host) and the second (from device in respond to the host's) packets shown on the oscilloscope. The first (of lower amplitude) is from the host and the second (of higher amplitude) is a device's response.
13. Detach the differential probe from the Device High-Speed Signal Quality test fixture.

3.2.2 C5545 Test Result - Device PP EL_21, EL_22, EL_25 Testing

Packet Parameter Test Results in Tek Format

- **Device ID:** fsfe_001
- **Device Description:** High Speed, Device, Device PP EL_21, EL_23, EL_25 Testing
- **Date:** Tue Nov 10 18:33:09 PST 2015
- **Overall Result:** Pass

Table 6. Test Result PP EL_21,EL_23, EL_25

Measurement Name	Measurement Value (bits)	USB Limits (bits)	Status
Sync Field	32	32	Pass
EOP Width	8.068833	7.5 to 8.5	Pass
Inter-Packet Gap	8	8 and 192	Pass

Additional Information: EOP Width in time is 16.81007 nS

Packet Parameter Test Results in Tek Format

- **Device ID:** fsfe_001
- **Device Description:** High Speed, Device, Device PP EL_22 Testing, Dummy Device
- **Date:** Tue Nov 10 18:38:09 PST 2015
- **Overall Result:** Pass

Table 7. Test Result PP EL_22

Measurement Name	Measurement Value (bits)	USB Limits (bits)	Status
Inter-Packet Gap	8	8 and 192	Pass

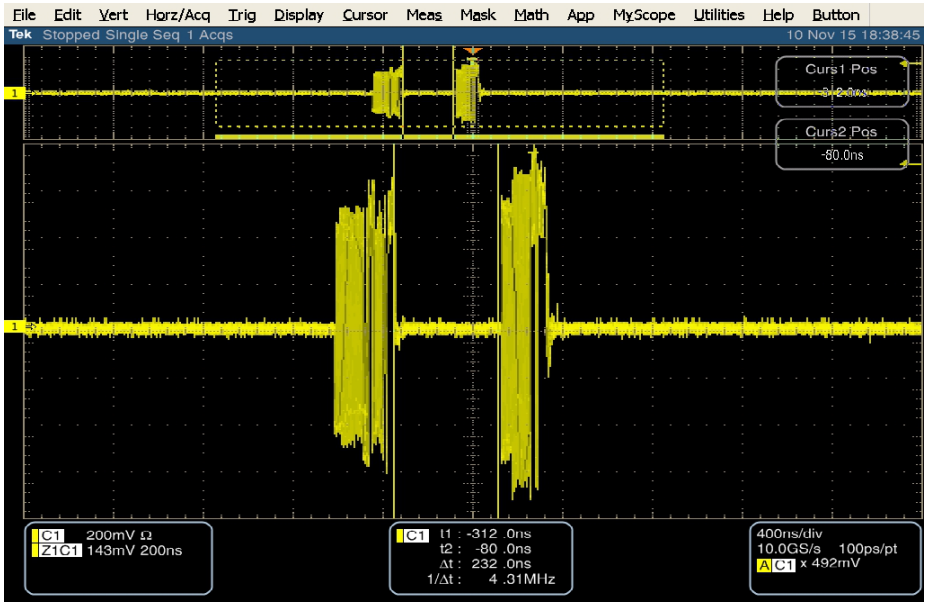

Figure 5. Test Result Capture - PP EL_22 - 1

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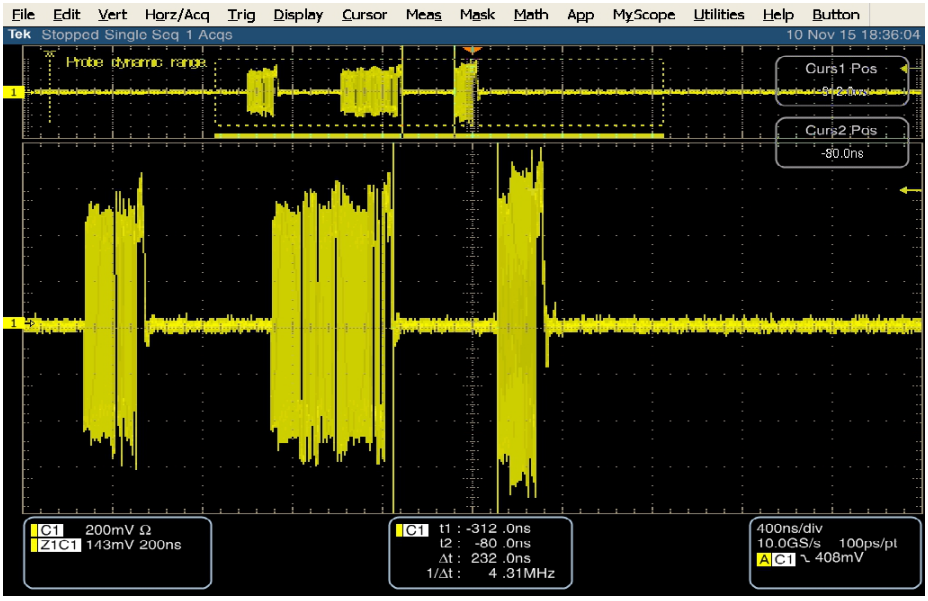

Figure 6. Test Result Capture - PP EL_22 - 2

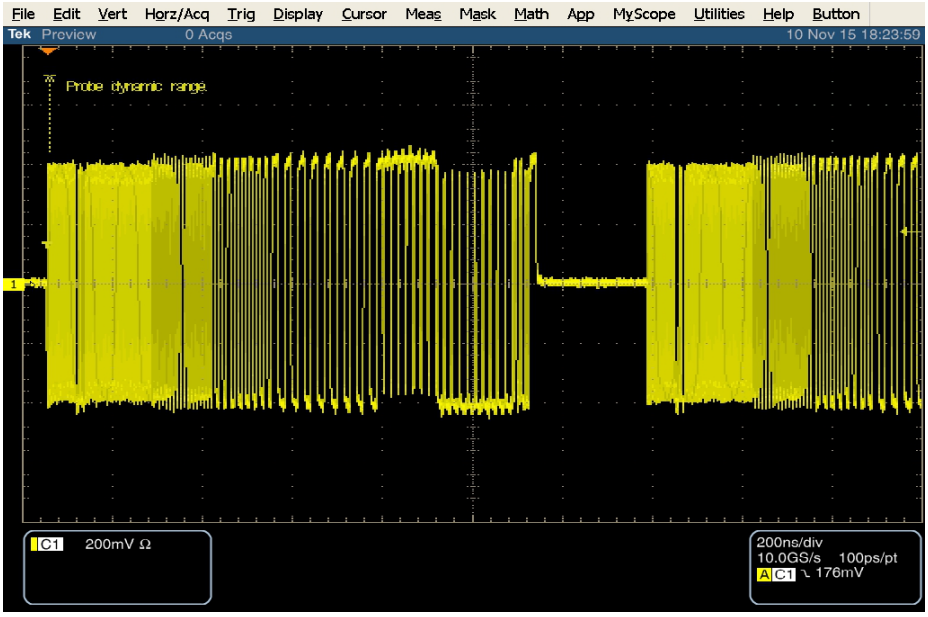

Figure 7. Test Result Capture - PP EL_22 - 3

3.3 Device CHIRP Timing (EL_28, EL_29, EL_31)

3.3.1 Procedure

The following EL_28, EL_29, EL_31 test procedures were followed:

1. Connect J34 of the Device SQ segment of the test fixture into the upstream facing port of the device under test. Connect the INIT port of the test fixture to a high-speed capable port of the test bed computer. Apply power to the device.
2. Connect Channel 2 and Channel 3 FET probes to the test fixture. Connect Channel 2 to D- and Channel 3 to D+. Connect the probe grounds.

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3. Launch the TDSUSB software application on the oscilloscopes.
4. Select File → Recall default in the applications menu bar.
5. Select the High Speed tab within the USB2.0 compliance test application.
6. Click the Chirp button on the application and select the Device option EL_28, EL_29, EL_31. Click Run.
7. Connect the upstream facing port of the device under test into the TEST port of the test fixture.
8. Click Enumerate Bus and capture the CHIRP handshake. The results can be viewed on the results panel.

NOTE: Instead of enumerating the device, an alternative method to generate the chirp signal, is to disconnect and reconnect the unit under test (device) to the port.

9. The EL_28 checks the devices CHIRP-K latency in response to the reset from the host port. The time should be between 2.5 µs and 6.0 ms.

NOTE: The test specification rev 1.0 contains an error regarding EL_28 at the time this test procedure was written. It states that the measurement time must be 2.5 µs to 3.0 ms, which is incorrect. The specification requires the CHIRP-K latency to be between 2.5 µs and 6.0 ms.

10. The EL_29 checks the device's CHIRP-K duration. The assertion time should be between 1.0 ms and 7.0 ms.
11. Following the host assertion of Chirp K-J-K-J-K-J, the device must respond by turning on its high-speed terminations. This is evident by a drop of amplitude of the alternate Chirp-K and Chirp-J sequence from the 800 mV nominal to the 400 mV nominal. Measure the time from the beginning of the last J in the Chirp K-J-K-J-K-J (3 pairs of Chirp-K-J's) to the time when the device turns on the high-speed terminations. It should be less than or equal to 500 µs. This is EL_31.
12. In addition to turning on its high-speed terminations, the device must also disconnect the D+ pull-up resistor in response to the host's assertion of Chirp K-J-K-J-K-J. The evidence is a slight drop of the D+ level during the Chirp-K from the host. Measure the time from the beginning of the last J in the Chirp K-J-K-J-K-J (3 pairs of Chirp-K-J's) to the time when the D+ pull-up resistor is disconnected. Verify that this is less than or equal to 500 µs. Record the measurement in EL_31.

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3.3.2 5545 Test Result – Device CHIRP Timing (EL_28, EL_29, EL_31)

Chirp-Test Results in Tek Format

- **Device ID:** fsfe_001
- **Device Description:** High Speed, Device EL_28, EL_29, EL_31 Testing
- **Date:** Tue Nov 10 18:53:34 PST 2015
- **Overall Result:** Pass

Table 8. Test Result - EL_28, EL_29, EL_31

Measurement Name	Measurement Value	USB Limits	Status
Chirp Reset Time	685.3299 µS	2.500000 uS to 6.000000 mS	Pass
Chirp-K Duration	1.099955 mS	2.500000 uS to 6.000000 mS	Pass

Additional Information:

- Chirp-K Amplitude: 1.094356 V
- USB Specification Limits: Amplitude approximately 800.0000 mV

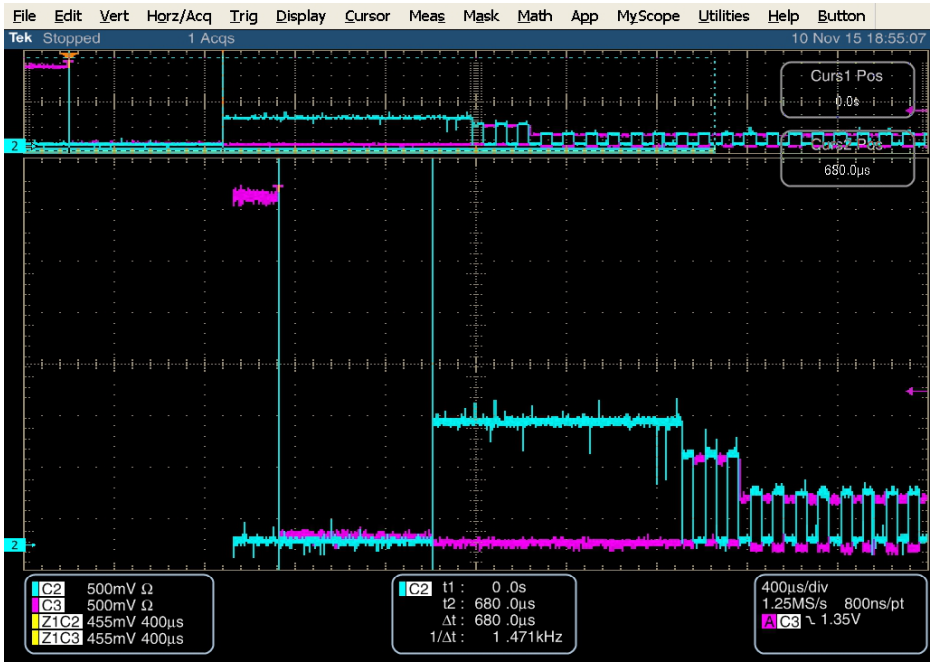

Figure 8. Test Result Capture - Chirp Timing

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3.4 Device Suspend, Resume, Reset Timing (EL_27, EL_28, EL_38, EL_39, EL_40)

3.4.1 Procedure

The following EL_27, EL_28, EL_38, EL_39, EL_40 test procedure was followed:

1. Plug the Init port of the test fixture of High Speed Signal Quality test section into a high-speed capable port of the test bed computer.
2. Connect the device under test into the Test port of the test fixture. Click Enumerate Bus to enumerate the newly connected device. The device under test should be enumerated with the device's VID shown together with the root port in which it is connected.
3. Connect Channel 2 and Channel 3 FET probes to the test fixture. Connect Channel 2 to D- and Channel 3 to D+. Connect the probe grounds.
4. Select the High Speed measurement tab → More button → Suspend measurement.
5. Set the input Signal Direction and run the measurements.
6. On the HS Electrical Test Tool application → Device Test menu, select SUSPEND from the Device Command dropdown menu. Click EXECUTE once to place the device into suspend.
7. The result contains EL_38, which is the time interval from the end of last SOF packet issued by the host to when the device attached its full speed pull-up resistor on D+. This is the time between the END of the last SOF packet and the rising edge transition to full speed J-state. The time should be between 3.000 ms and 3.125 ms. The following steps verify the Resume response of the device under test:
   (a) Select the High Speed measurement tab → More button → Resume measurement.
   (b) Set the input Signal Direction and run the measurements
   (c) On the HS Electrical Test Tool application → Device Test menu, select RESUME from the Device Command dropdown menu. Click EXECUTE once to resume the device from suspend.
8. The result consists of the time between the falling edge of D+ and the First SOF, which should not exceed 3.0 ms. The device should resume the HS operation, which is indicated by the presence of HS SOF packets (with 400 mV nominal amplitudes) following the K State driven by the host controller. This is EL_40.

The following steps verify that the device resumes back to back to high-speed operation after being reset from high-speed operation.

1. Select the High-Speed measurement tab → More button → Reset High Speed measurement.
2. On the HS Electrical Test Tool application → Device Test menu, select RESET from the Device Command dropdown menu. Click EXECUTE once to reset the device operating in high-speed.

The results contain the time between the beginning of the last SOF before the reset and the start of the device chirp-K. The device should transmit a chirp handshake following the reset. It should be between 3.1 ms and 6 ms. this is EL_27. The following steps verify the device's chirp response after being reset from suspend.

1. Select the High-Speed measurement tab → More button → Reset from Suspend measurement.
2. On the HS Electrical Test Tool application → Device Test menu, select SUSPEND from the Device Command dropdown menu. Click EXECUTE once to place the device into suspend.

On the HS Electrical Test Tool application → Device Test menu, select RESET from the Device Command dropdown menu. Click EXECUTE once to reset the device in suspend.

The device responds to the reset with the Chirp-K. The results contain the time between the falling edge of the D+ and the start of the device chirp-K. It should be between 2.5 µs and 6.0 ms. This is EL_28.

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3.4.2 C5545 Test Result - Device Suspend, Resume, Reset Timing (EL_27, EL_28, EL_38, EL_39, EL_40)

Suspend Test Results in Tek Format

- **Device ID:** fsfe_001
- **Device Description:** High Speed, Up Stream Testing
- **Date:** Tue Nov 10 19:21:29 PST 2015
- **Overall Result:** Pass

Table 9. Test Result - Device Suspend

Measurement Name	Suspend Time	USB Limits	Status
Suspend Test	3.000197 mS	3.000000 mS to 3.125000 mS	Pass

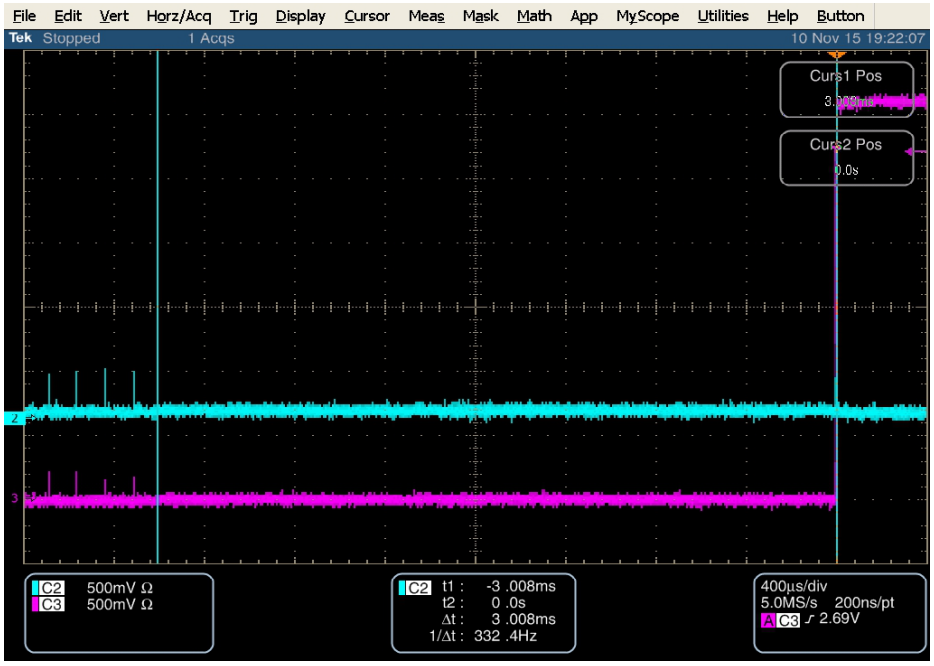

Figure 9. Test Result Capture - Suspend Timings

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Resume Test Results in Tek Format

- **Device ID:** fsfe_001
- **Device Description:** High Speed, Up Stream Testing, Dummy Device
- **Date:** Tue Nov 10 19:25:49 PST 2015
- **Overall Result:** Pass

Table 10. Test Result - Device Resume

Measurement Name	Amplitude	USB Limits	Status
Resume Test	473.6200 mV	300.0000 mV to 525.0000 mV	Pass

Additional Information: Resume Time for this test is 12.99555 µS

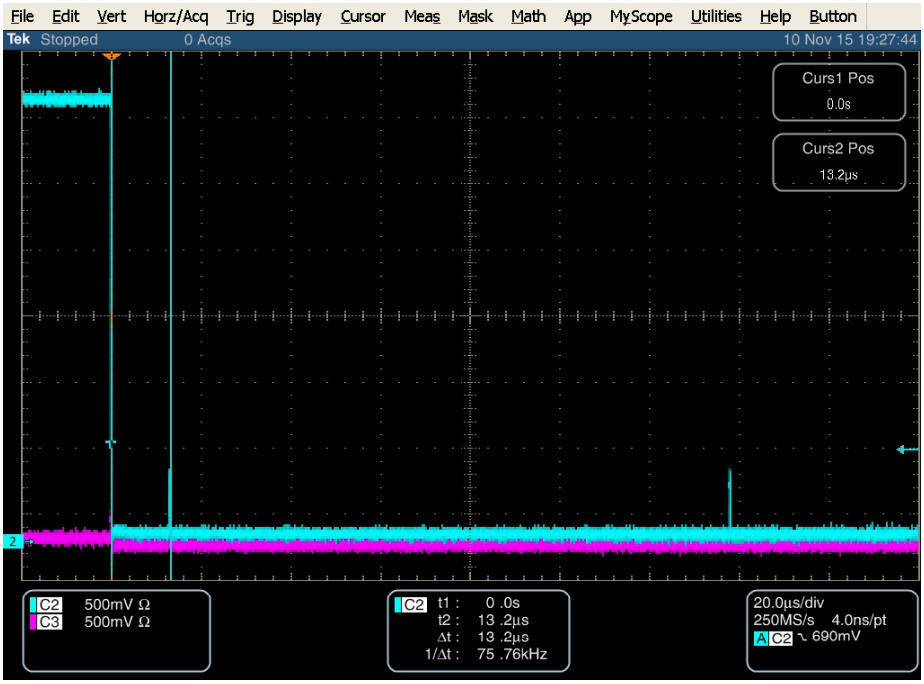

Figure 10. Test Result Capture - Resume Timings

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Reset from High Speed Test Results in Tek Format

- **Device ID:** fsfe_001
- **Device Description:** High Speed, Up Stream Testing, Dummy Device
- **Date:** Tue Nov 10 19:33:07 PST 2015
- **Overall Result:** Pass

Table 11. Reset From High Speed Test Result

Measurement Name	Reset From High Speed Time	USB Limits (bits)	Status
Reset From High Speed Test	3.100734 mS	3.100000 mS to 6.000000 mS	Pass

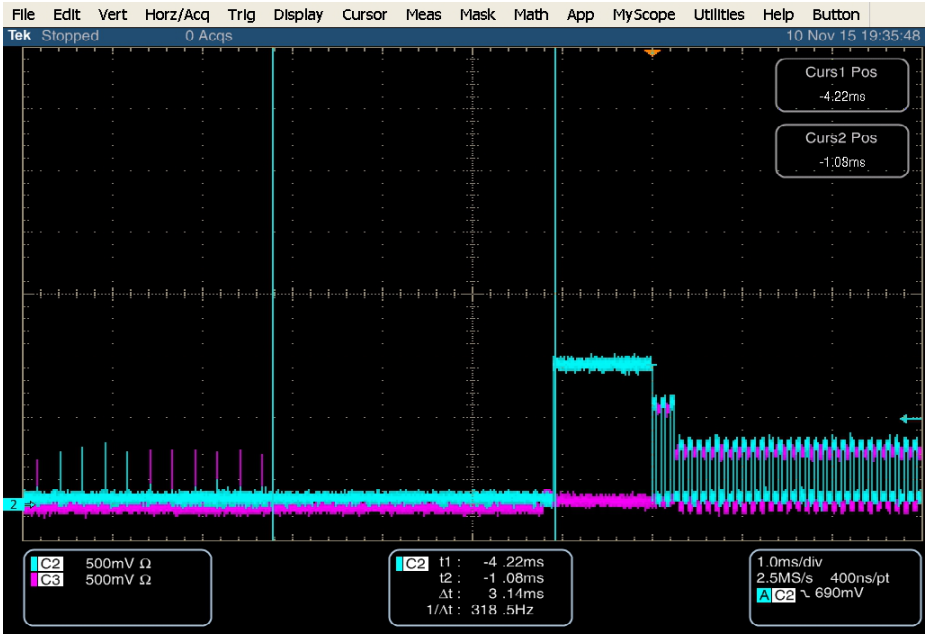

Figure 11. Test Result Capture - Reset From High Speed

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Reset from Suspend Test Results in Tek Format

- **Device ID:** fsfe_001
- **Device Description:** High Speed, Up Stream Testing, Dummy Device
- **Date:** Tue Nov 10 19:41:24 PST 2015
- **Overall Result:** Pass

Table 12. Reset From Suspend - Test Result

Measurement Name	Reset from Suspend Time	USB Limits	Status
Reset From Suspend Test	685.5412 uS	2.500000 uS to 3.000000 mS	Pass

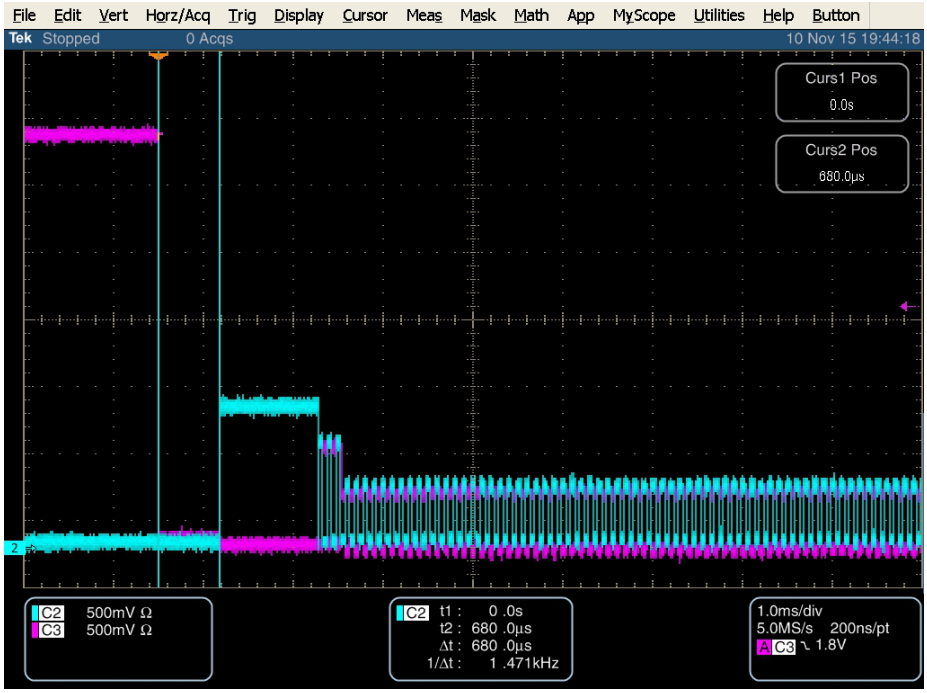

Figure 12. Test Result Capture - Reset From Suspend

3.5 Device Test J/K, SE0_NAK (EL_8, EL_9)

3.5.1 Procedure

The following EL_9 test procedures were followed:

1. Attach the USB cable to the power connector of the Device High-speed Signal Quality section of the test fixture.
2. Verify that the red Power LED is lit, and the red Test LED is off.
3. Connect the Test port of the Device High-speed Signal Quality test fixture into the upstream facing port of the device under test. Connect the Init port of the test fixture to a high-speed capable port of the test bed computer. Click Enumerate Bus to force enumeration of the newly connected device. The device under test should be enumerated with the device's VID shown together with the root port in which it is connected.
4. On the HS Electrical Test Tool application → Device Test menu, select TEST_SE0_NAK from the Device Command dropdown menu. Click EXECUTE once to place the device into TEST_SE0_NAK test mode.
5. Switch the test fixture into the TEST position. Using a DVM measure the DC voltage on the D+ line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL_9.

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6. Using a DVM measure the DC voltage on the D- line at J7 with respect to ground (pin J10 and J11 are ground pins). Record in section EL_9. Return the Test switch to the NORMAL position.
7. Remove the Device High Speed Signal Quality test fixture. Cycle the device power to prepare it for subsequent tests.

3.5.2 C5545 Test Result - Device Test J/K, SE0_NAK (EL_9)

EL_9 When either D+ or D- are not being driven, the output voltage must be 0 V ±10 mV when terminated with precision 45 Ω resistors to ground.

Table 13. Test Result - J/K, SE0_NAK

	Voltage (mV)
D+	9
D-	9

3.6 Device Receiver Sensitivity (EL_16, EL_17, EL_18)

3.6.1 Procedure

This section tests the sensitivity of the receivers on a device under test. A Tektronix DTG 5000 series instrument with DTGM21, AWG5000 series, AWG7000 series, or DG2040 Data Generator (discontinued) emulates the In command from the hub port to device address 1. The following EL_16, EL_17, EL_18 test procedures were followed:

1. Attach the USB cable to the designated power supply port to the Device Receiver test fixture J35 and verify that the red Power LED is lit. Leave the TEST switch at the INIT position. The red test LED should be off and the red INIT LED should be on.
2. Connect the Init port of the fixture to a port on the test bed computer. Connect the Test Port of the fixture to the device under test. Click the Enumerate Bus button once to force enumeration of the newly connected device. The device under test should be enumerated with the device's VID shown together with the root port in which it is connected.
3. Two sets of SMA cables are required, each with a 6dB attenuators inserted. Connect the 6dB attenuators to OUTPUT1 and OUTPUT2 of Agilent 81130A Pulse/Pattern Generator. Connect OUTPUT 1 to SMA1 (D+), and OUTPUT 2 to SMA2 (D-) of the Device Receiver Sensitivity test fixture using the SMA cables.
4. Connect the differential probe to the test fixture at J25. From the TDSUSB application, select Measurement → Select. Click on the High Speed tab and click Receiver Sensitivity.
5. The pattern generator generates IN packets (of compliant amplitude) with a 12-bit SYNC field.
6. On the HS Electrical Test Tool application → Device Test menu, select TEST_SE0_NAK from the Device Command dropdown menu. Click EXECUTE once to place the device into TEST_SE0_NAK test mode.
7. Place the test fixture Test Switch S6 into the TEST position. This switches in the data generator in place of the host controller. The data generator emulates the IN packets from the host controller.
8. Verify that all packets from the data generator are NAK'd by the port under test. Record the Pass/Fail in EL_18.
9. Using pattern generator set IN-ADD1.PDA setup file, follow the procedure mentioned in appendix B section of document "Device HS Test for Agilent Infiniium 54846Revision 1.1" located at http://www.agilent.com/home.
10. Verify that all packets are NAK'd while signaling is at this amplitude.
11. Reduce the amplitude of the data generator packets in 50 mV steps (on the generator before the attenuator) while monitoring the NAK response from the device on the oscilloscope. The adjustment should be made to both channels such that Channel 0 and Channel 1 are matched, as indicated by the data generator readout. Reduce the amplitude until the NAK packets begins to become intermittent. At this point, increase the amplitude such that the NAK packet is not intermittent. This is just above the minimum receiver sensitivity levels before squelch.

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12. Measure the Zero to Positive Peak of the packet from the data generator using the cursors. The peak should be taken at the plateaus of the wider pulses to avoid inflated reading due to overshoots. Press the record button on the TDSUSB application corresponding to the receiver sensitivity level and record the measurement in EL_17 of appendix A.
13. Measure the Zero to Negative Peak of the packet from the data generator as using the cursors. The peak should be taken at the plateaus of the wider pulses to avoid inflated reading due to overshoots. Record the measurement in EL_17. As long as the receiver continues to NAK the data generator packet above ± 150 mV, the device is considered to have passed the test. Record PASS/FAIL in EL_17.
14. Now further reduce the amplitude of the packet from the data generator in small steps, still maintaining the balance between Channel 0 and Channel 1 until the receiver just cease to respond with NAK. This is the squelch level of the receiver.
15. Measure the Zero to Positive Peak of the packet from the data generator using the cursors. The measurement is best made by turning on the Fit To Screen function in the Horizontal menu of the oscilloscope to maintain sufficient sampling rate. The peak should be taken at the plateaus of the wider pulses to avoid inflated reading due to overshoots. Record the measurement in EL_16.
16. Measure the Zero to Negative Peak of the packet from the data generator using the cursors. The peak should be taken at the plateaus of the wider pulses to avoid inflated reading due to overshoots. Record the measurement in EL_16. As long as the receiver ceases to NAK the data generator packet below ± 100 mV it is considered to have passed the test. Record PASS/FAIL in EL_16.

NOTE: With certain devices, making an accurate zero-to-peak measurement of the In packet from the data generator may be difficult due to excessive reflection artifacts. Also, on devices with captive cable, the measured zero-to-peak amplitudes of the In packet at the test fixture could be considerably higher than that seen by the device receiver. In these situations, it is advisable to make the measurement near the device receiver pins on the PCB.

3.6.2 C5545 Test Result - Device Receiver Sensitivity (EL_16, EL_17, EL_18)

Receiver-Sensitivity Test Results in Tek Format

- **Device ID:** fsfe_001
- **Device Description:** High Speed, Dummy Device
- **Date:** Fri Dec 04 18:05:33 PST 2015
- **Overall Result:** Pass [(1)]

[(1)] Device has passed all the tests.

Table 14. Receiver Sensitivity Test Results

Measurement Name	Positive Peak	Negative Peak	USB Limits (bits)	USB-IF Waiver	Status
Receiver Level	188.0 mV	188.0 mV	Must receive <= 150 mV	Must receive <= 200 mV	Pass
Squelch Level	188.0 mV	188.0 mV	Must not respond < 100 mB	Must not respond < 50 mV	Pass
EL_18 Level	–	–	Device should respond with minimum 12 bit SYNC field	–	Pass

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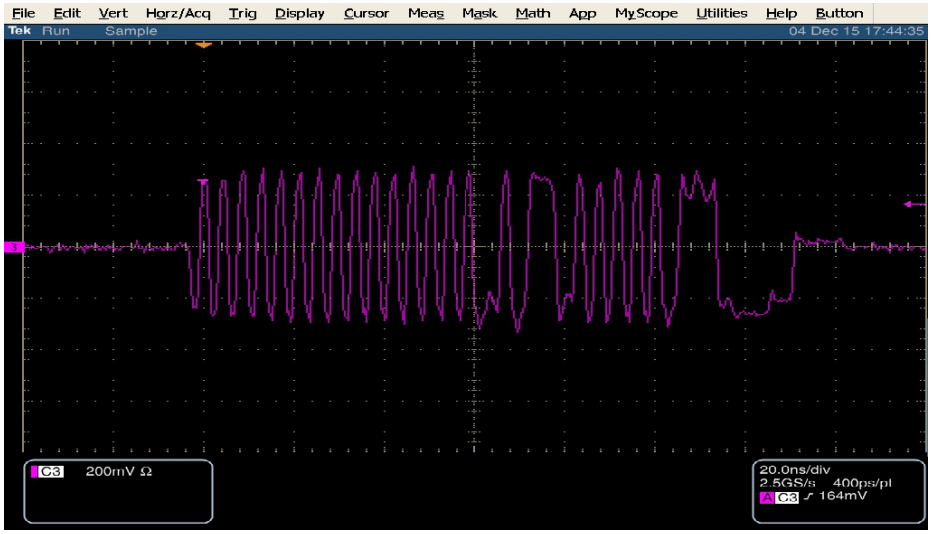

Figure 13. Receiver Sensitivity Test - 1

Figure 14. Receiver Sensitivity Test - 2

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4 FULL Speed Tests

4.1 Full-Speed Upstream Signal Quality Testing

4.1.1 Test Setup

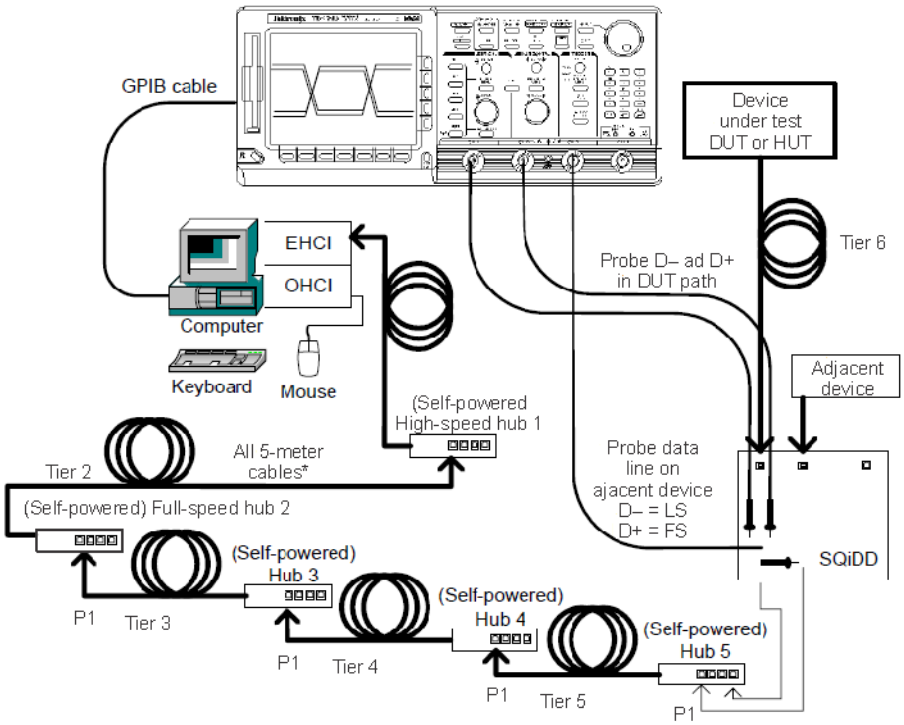

Figure 15. Device and Hub Upstream Signaling Test and Receiver Test Schematic

4.1.2 Procedure

Check the following test setup, plug in the device to tier 5 hub.

1. Ensure signal path compensation has been run on the scope recently (within 4 hours).
2. Start MatLab script.
3. Start GPIB DAQ.
4. Get zeroes.
5. Scope must be triggering in order to get zeros (typically ranges between 50 mV–150 mV) and DUT must be unplugged.
6. Attach the HS Hubs to the EHCI controller as shown in Figure 15. Hub #1 is required to be a High Speed Hub for USBHSET to work properly. Hub #2 is required to be a Full Speed Hub to ensure the DUT/HUT operates at Full Speed when testing a High Speed capable device. Each hub below Hub #1 should be attached to port 1 of the upstream hub, with the exception of the HUT, if testing a hub. This will make it easier to identify the device under test from the enumerated device list provided by HSET. Verify in Device Manager that all hubs enumerate properly.
7. On the Oscilloscope recall Setup for Upstream Low Speed or Upstream Full Speed (Setup 1 or Setup 2, respectively).
8. Connect probes:

   (a) Channel 1 D-, Channel 2 D+

   (i) If running Upstream low speed test connect Channel 3 to D

   (ii) If running Upstream Full speed test connect Channel 3 to D+

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9. Plug in the adjacent device to SQiDD board section 2. Plug the SQiDD board section 2 into port 1 of Hub 5. Verify that the adjacent device enumerates properly. The adjacent (trigger qualifier) device should always be attached to port 1 of the same hub that the DUT or HUT is attached to with the DUT/HUT attached to any of the remaining ports. This makes it easier to identify the DUT/HUT in the enumeration list in HSET.
10. Start HSET.
11. Plug in DUT to SQiDD board section 1 (using a known good 5 meter cable if testing FS SQ). Connect the other side of the SQiDD board to hub 5, any port except port 1.
12. Select device in USBHSET
13. When the Device Test screen appears, click the enumerate button. This forces a complete
14. Enumeration of the tree. All devices attached to the EHCI host controller should appear in the device enumeration list.
15. The highlighted device in this example is the device under test. Otherwise, you will need to know theVID/PID of the device under test to determine which device in the list is the DUT/HUT. This is difficult if you are testing a device that has the same VID/PID as another device in the tree itself.
16. Ensure that the DUT/HUB enumerates reliably on tier 6 by clicking Enumerate Bus several times. The Enumerate Bus button will be grayed out during the enumeration sequence. The device should show up each time (as verified by VID/PID). Again, it should be at the bottom of the list if the tree is connected properly.
17. If the device doesn't show up each time you click Enumerate Bus, move the DUT/HUT and the adjacent device up one tier and repeat step 14. After determining the tier that the device reliably enumerates on, proceed. The device must reliably enumerate on Tier 6 to pass. Reliable enumeration on Tier 4 or Tier 5 will result in a pass with waiver, if no other problems are encountered.
18. Select the DUT/HUT in the enumeration list by clicking on it.
19. Select the LOOP DEVICE DESCRIPTOR option in the Device Command pull down menu as shown.
20. Check the scope to make sure waveform has been captured
21. Use vertical cursor to select an upstream signal packet. The scope cursors should bracket the DUT/HUT upstream packet. The left-most cursor should be placed approximately 1 bit time to the left of the first sync bit and the right-most cursor should be placed approximately 1 bit time to the right of the EOP rising edge. This will include idle bus voltage levels (D+ at 3.3 V nominal).
22. In The GIP DAQ Program, select:
    (a) GPIB DAQ auto → USB (Low or Full Speed) Upstream Signal →tier* (*choose the number of the tier where the DUT reliably enumerates as described in steps 14 and 15)
    (b) After save, press Enter in the MatLab command prompt window.
    (c) Plots are displayed and results are on the MatLab command prompt window.
    (d) If needed, save results to floppy.
    (e) To exit the test, click the Return to Main button on the Device Test screen.

Reporting Results:

- Eye: pass/fail
- Cross Over: pass/fail
- EOP: pass/fail
- Receivers:
- Signal Rate: 1.5 Mb/sec or 12 Mb/sec
- Jitter:

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4.1.3 C5545 Validation - Full-Speed Upstream Signal Quality Test

Signal Quality Test Results in Tek Format

- **Device ID:** fsfe_001
- **Device Description:** Full Speed, Far End Device, Up Stream Testing, Tier 6
- **Date:** Tue Dec 08 18:37:57 PST 2015
- **Overall Result:** Pass [(1)]

(1) The Overall Result for this test is Pass, because individual status of the measurements is Pass and it is performed on Tier 6 (as per USB-IF).

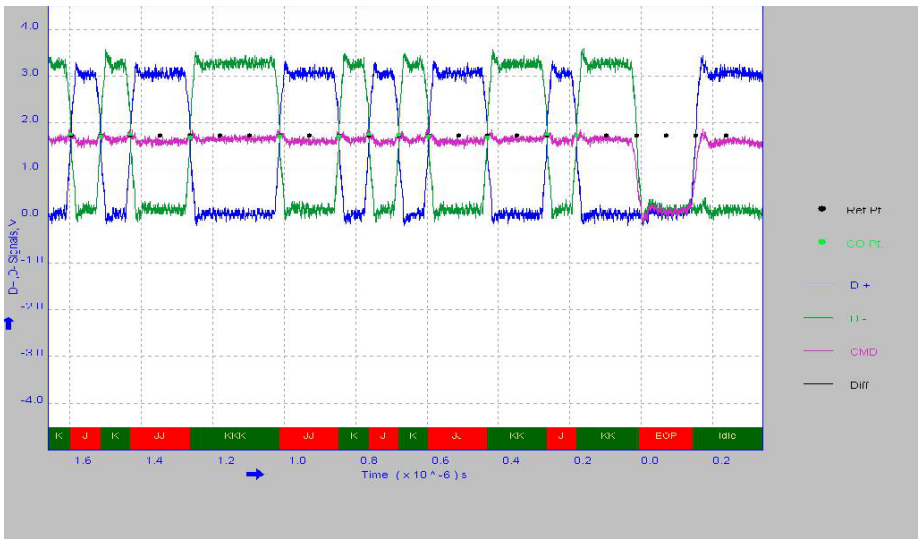

Figure 16. Waveform Plot

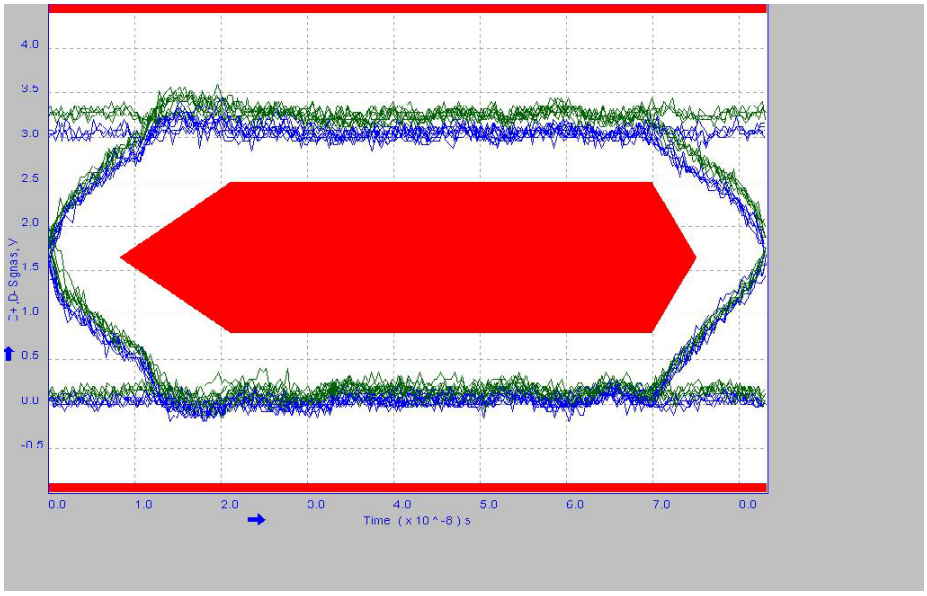

Figure 17. Eye Diagram

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Table 15. Device Full Speed Test Result

Measurement Name	Minimum	Maximum	Mean	pk-pk	Standard Deviation	RMS	Population	Status
Eye Diagram Test	-	-	-	-	-	-	-	Pass
Signal Rate	11.92098 Mbps	12.11632 Mbps	12.00678 Mbps	0.0000 bps	61.57303 kbps	12.00881Mbps	17	Pass
Crossover Voltage	1.673333 V	1.760000 V	1.722341 V	86.66667 mV	25.59332 mV	1.722516 V	12	Pass
EOP Width	-	-	165.4823 ns	-	-	-	1	Pass
Consecutive Jitter	-481.4617 ps	607.7540 ps	0.0000s	1.089216 ns	331.3928 ps	315.9706 ps	11	Pass
Paired JK Jitter	-257.8431 ps	58.82353 ps	-67.25490 ps	316.6667 ps	133.5509 ps	137.0835 ps	5	Pass
Paired KJ Jitter	-435.2941 ps	258.8235 ps	-164.7059 ps	694.1176 ps	296.8310 ps	305.3023 ps	4	Pass

Additional Information:

- Rise Time: Min: 22.512 ns Max: 23.785 ns Mean: 23.045 ns Std: 469.09 ps RMS: 23.049 ns Population: 6
- Fall Time: Min: 22.363 ns Max: 23.004 ns Mean: 22.673 ns Std: 229.52 ps RMS: 22.674 ns Population: 6

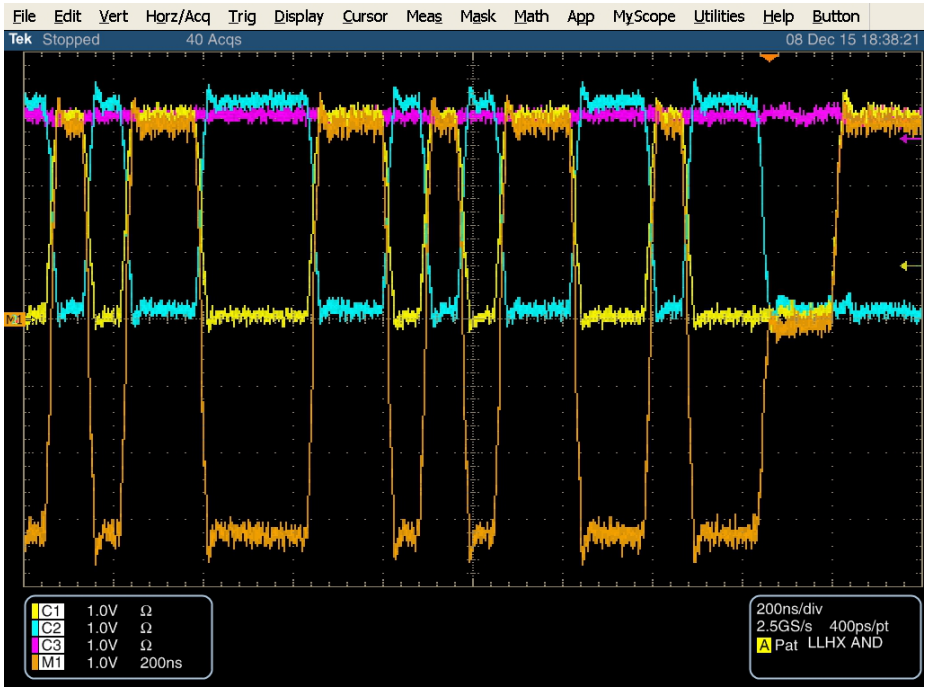

Figure 18. Test Result Capture - USB Full Speed Test

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