10-BIT, 2 ANALOG INPUT, 8 MSPS, SIMULTANEOUS SAMPLING ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **Simultaneous Sampling of Two Single-Ended Signals or One Differential Signals or Combination of Both**
- **Signal-to-Noise and Distortion Ratio: 59 dB at f_I = 2 MHz**
- **Differential Nonlinearity Error: ±1 LSB**
- **Integral Nonlinearity Error: ±1 LSB**
- **Auto-Scan Mode for Two Inputs**
- **3-V or 5-V Digital Interface Compatible**
- **Low Power: 216 mW Max at 5 V**
- **Power Down: 1 mW Max**
- **5-V Analog Single Supply Operation**
- **Internal Voltage References . . . 50 PPM/°C and ±5% Accuracy**
- **Glueless DSP Interface**
- **Parallel μC/DSP Interface**

APPLICATIONS

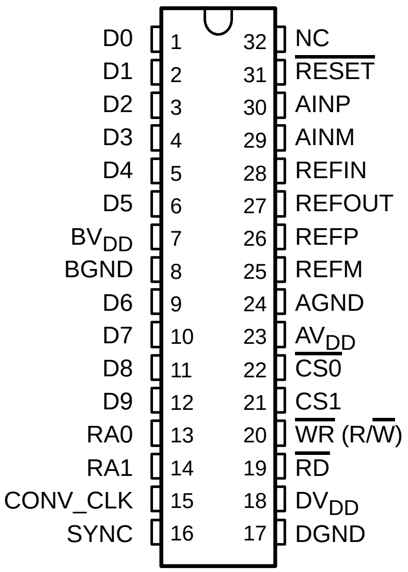
- **Radar Applications**
- **Communications**
- **Control Applications**
- **High-Speed DSP Front-End**
- **Automotive Applications**

DESCRIPTION

The THS1009 is a CMOS, low-power, 10-bit, 8 MSPS analog-to-digital converter (ADC). The speed, resolution, bandwidth, and single-supply operation are suited for applications in radar, imaging, high-speed acquisition, and communications. A multistage pipelined architecture with output error correction logic provides for no missing codes over the full operating temperature range. Internal control registers allow for programming the ADC into the desired mode. The THS1009 consists of two analog inputs, which are sampled simultaneously. These inputs can be selected individually and configured to single-ended or differential inputs. Internal reference voltages for the ADC (1.5 V and 3.5 V) are provided. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application.

The THS1009C is characterized for operation from 0°C to 70°C, and the THS1009I is characterized for operation from –40°C to 85°C.

DA PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGED DEVICE
	TSSOP (DA)
0°C to 70°C	THS1009CDA
–40°C to 85°C	THS1009IDA

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		UNITS
Supply voltage range	DGND to DV_{DD}	–0.3 V to 6.5 V
	BGND to BV_{DD}	–0.3 V to 6.5 V
	AGND to AV_{DD}	–0.3 V to 6.5 V
Analog input voltage range		AGND –0.3 V to AV_{DD} + 1.5 V
Reference input voltage		–0.3 V + AGND to AV_{DD} + 0.3 V
Digital input voltage range		–0.3 V to BV_{DD}/DV_{DD} + 0.3 V
Operating virtual junction temperature range, T_J		–40°C to 150°C
Operating free-air temperature range, T_A	THS1009C	0 to 70°C
	THS1009I	–40°C to 85°C
Storage temperature range, T_{stg}		–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

POWER SUPPLY		MIN	NOM	MAX	UNIT
Supply voltage	AV_{DD}	4.75	5	5.25	V
	DV_{DD}	4.75	5	5.25	
	BV_{DD}	3		5.25	

ANALOG AND REFERENCE INPUTS	MIN	NOM	MAX	UNIT
Analog input voltage in single-ended configuration	V_{REFM}		V_{REFP}	V
Common-mode input voltage V_{CM} in differential configuration	1	2.5	4	V
External reference voltage,V_{REFP} (optional)		3.5	AV_{DD}–1.2	V
External reference voltage, V_{REFM} (optional)	1.4	1.5		V
Input voltage difference, REFP – REFM		2		V

DIGITAL INPUTS		MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}	BV_{DD} = 3.3 V	2			V
	BV_{DD} = 5.25 V	2.6			V
Low-level input voltage, V_{IL}	BV_{DD} = 3.3 V			0.6	V
	BV_{DD} = 5.25 V			0.6	V
Input CONV_CLK frequency	DV_{DD} = 4.75 V to 5.25 V	0.1		8	MHz
CONV_CLK pulse duration, clock high, $t_{w(CONV\_CLKH)}$	DV_{DD} = 4.75 V to 5.25 V	62	62	5000	ns
CONV_CLK pulse duration, clock low, $t_{w(CONV\_CLKL)}$	DV_{DD} = 4.75 V to 5.25 V	62	62	5000	ns
Operating free-air temperature, T_A	THS1009CDA	0		70	°C
	THS1009IDA	–40		85	

ELECTRICAL CHARACTERISTICS

over recommended operating conditions, $AV_{DD} = DV_{DD} = 5$ V, $BV_{DD} = 3.3$ V, V_{REF} = internal voltage (unless otherwise noted)

DIGITAL SPECIFICATIONS						
PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Digital inputs						
I_{IH}	High-level input current	DV_{DD} = digital inputs	–50		50	µA
I_{IL}	Low-level input current	Digital input = 0 V	–50		50	µA
C_i	Input capacitance			5		pF
Digital outputs						
V_{OH}	High-level output voltage	$I_{OH} = –50$ µA, $BV_{DD} = 3.3$ V, 5 V	BV_{DD}–0.5			V
V_{OL}	Low-level output voltage	$I_{OL} = 50$ µA, $BV_{DD} = 3.3$ V, 5 V			0.4	V
I_{OZ}	High-impedance-state output current	CS1 = DGND, CS0 = DV_{DD}	–10		10	µA
C_O	Output capacitance			5		pF
C_L	Load capacitance at databus D0 – D9				30	pF

ELECTRICAL CHARACTERISTICS

over recommended operating conditions, $AV_{DD} = DV_{DD} = 5$ V, $BV_{DD} = 3.3$ V, $f_s = 8$ MSPS, V_{REF} = internal voltage (unless otherwise noted)

DC SPECIFICATIONS						
PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
	Resolution		10			Bits
Accuracy						
	Integral nonlinearity, INL				±1	LSB
	Differential nonlinearity, DNL				±1	LSB
	Offset error	After calibration in single-ended mode		±5		LSB
		After calibration in differential mode	–10		10	LSB
	Gain error		–10		10	LSB
Analog input						
	Input capacitance			15		pF
	Input leakage current	$V_{AIN} = V_{REFM}$ to V_{REFP}			±10	µA
Internal voltage reference						
	Accuracy, V_{REFP}		3.3	3.5	3.7	V
	Accuracy, V_{REFM}		1.4	1.5	1.6	V
	Temperature coefficient			50		PPM/°C
	Reference noise			100		µV
	Accuracy, REFOUT		2.475	2.5	2.525	V
Power supply						
I_{DDA}	Analog supply current	$AV_{DD} = DV_{DD} = 5$ V, $BV_{DD} =3.3$ V		36	40	mA
I_{DDD}	Digital supply current	$AV_{DD} = DV_{DD} = 5$ V, $BV_{DD} = 3.3$ V		0.5	3	mA
I_{DDB}	Buffer supply current	$AV_{DD} = DV_{DD} = 5$ V, $BV_{DD} = 3.3$ V		1.5	4	mA
	Power dissipation	$AV_{DD} = DV_{DD} = 5$ V, $BV_{DD} = 3.3$ V		186	216	mW
	Power dissipation in power down with conversion clock inactive	$AV_{DD} = DV_{DD} = 5$ V, $BV_{DD} = 3.3$ V			0.25	mW

ELECTRICAL CHARACTERISTICS

over recommended operating conditions, V_{REF} = internal voltage, f_S = 8 MSPS, f_I = 2 MSPS at –1 dB (unless otherwise noted)

AC SPECIFICATIONS, $AV_{DD} = DV_{DD}$ = 5 V, BV_{DD} = 3.3 V, C_L < 30 pF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise ratio + distortion	Differential mode	56	59		dB
		Single-ended mode	55	58		
SNR	Signal-to-noise ratio	Differential mode	59	61		dB
		Single-ended mode	58	60		
THD	Total harmonic distortion	Differential mode		–64		dB
		Single-ended mode		–63		
ENOB	Effective number of bits	Differential mode	9	9.5		Bits
		Single-ended mode	8.85	9.35		
SFDR	Spurious free dynamic range	Differential mode	61	65		dB
		Single-ended mode	60	64		
Analog Input						
	Full-power bandwidth with a source impedance of 150 Ω in differential configuration.	Full scale sinewave, –3 dB		96		MHz
	Full-power bandwidth with a source impedance of 150 Ω in single-ended configuration.	Full scale sinewave, –3 dB		54		MHz
	Small-signal bandwidth with a source impedance of 150 Ω in differential configuration.	100 mVpp sinewave, –3 dB		96		MHz
	Small-signal bandwidth with a source impedance of 150 Ω in single-ended configuration.	100 mVpp sinewave, –3 dB		54		MHz

TIMING REQUIREMENTS

$AV_{DD} = DV_{DD}$ = 5 V, BV_{DD} = 3.3 V, V_{REF} = internal voltage, C_L < 30 pF

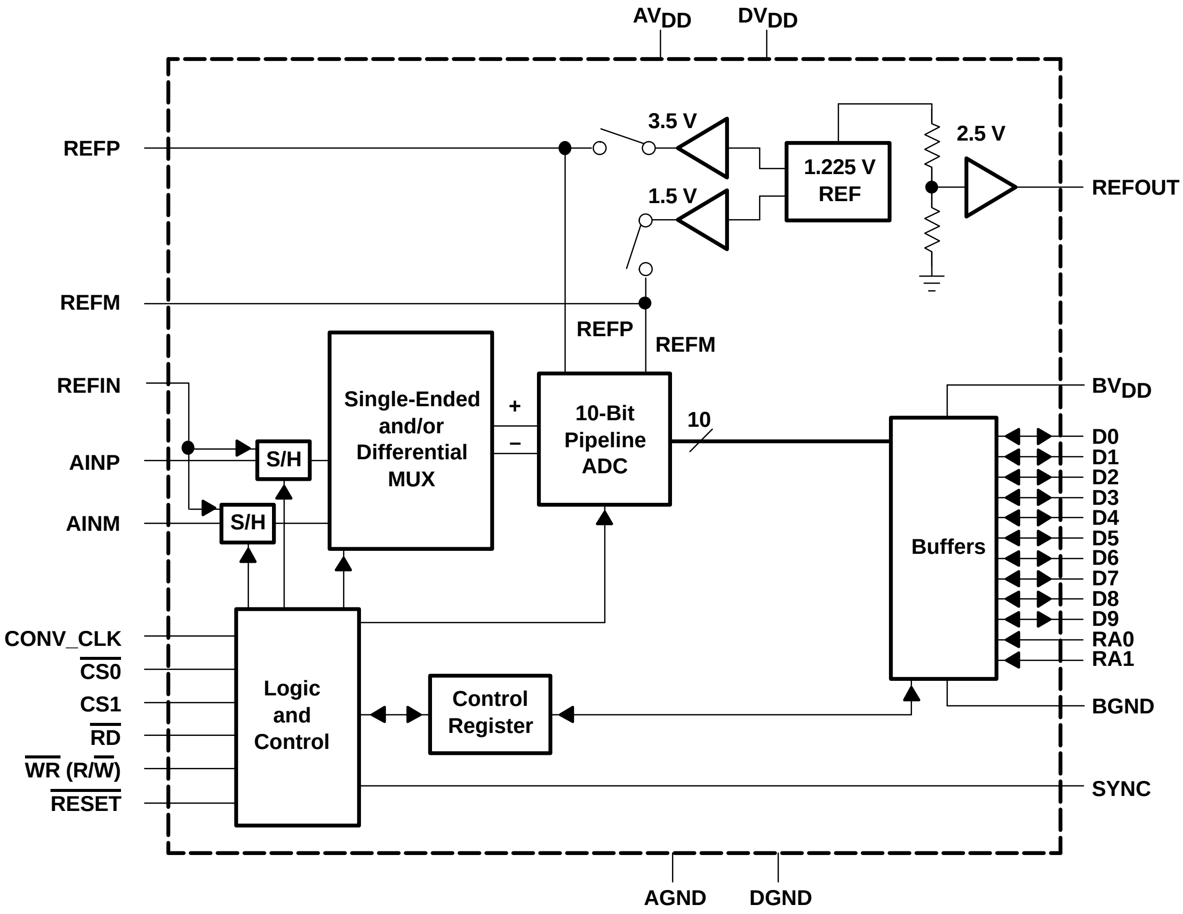
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pipe}	Latency			5		CONV CLK
$t_{su(CONV\_CLKL\text{-}READL)}$	Setup time, CONV_CLK low before CS valid		10			ns
$t_{su(READH\text{-}CONV\_CLKL)}$	Setup time, CS invalid to CONV_CLK low		20			ns
$t_{d(CONV\_CLKL\text{-}SYNCL)}$	Delay time, CONV_CLK low to SYNC low				10	ns
$t_{d(CONV\_CLKL\text{-}SYNCH)}$	Delay time, CONV_CLK low to SYNC high				10	ns

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AINP	30	I	Analog input, single-ended or positive input of differential channel A
AINM	29	I	Analog input, single-ended or negative input of differential channel A
AV_{DD}	23	I	Analog supply voltage
AGND	24	I	Analog ground
BV_{DD}	7	I	Digital supply voltage for buffer
BGND	8	I	Digital ground for buffer
CONV_CLK	15	I	Digital input. This input is the conversion clock input.
$\overline{\text{CS0}}$	22	I	Chip select input (active low)
CS1	21	I	Chip select input (active high)
SYNC	16	O	Synchronization output. This signal indicates in a multichannel operation that data of channel A is brought to the digital output and can therefore be used for synchronization.
DGND	17	I	Digital ground. Ground reference for digital circuitry.
DV_{DD}	18	I	Digital supply voltage
D0 – D9	1–6, 9–12	I/ O/Z	Digital input, output; D0 = LSB
RA0	13	I	Digital input. RA0 is used as an address line (RA0) for the control register. This is required for writing to control register 0 and control register 1. See Table 7.
RA1	14	I	Digital input. RA1 is used as an address line (RA1) for the control register. This is required for writing to control register 0 and control register 1. See Table 7.
NC	32	O	Not connected
REFIN	28	I	Common-mode reference input for the analog input channels. It is recommended that this pin be connected to the reference output REFOUT.
REFP	26	I	Reference input, requires a bypass capacitor of 10 μF to AGND in order to bypass the internal reference voltage. An external reference voltage at this input can be applied. This option can be programmed through control register 0. See Table 8.
REFM	25	I	Reference input, requires a bypass capacitor of 10 μF to AGND in order to bypass the internal reference voltage. An external reference voltage at this input can be applied. This option can be programmed through control register 0. See Table 8.
$\overline{\text{RESET}}$	31	I	Hardware reset of the THS1009. Sets the control register to default values.
REFOUT	27	O	Analog fixed reference output voltage of 2.5 V. Sink and source capability of 250 μA. The reference output requires a capacitor of 10 μF to AGND for filtering and stability.
$\overline{\text{RD}}$(1)	19	I	The $\overline{\text{RD}}$ input is used only if the $\overline{\text{WR}}$ input is configured as a write only input. In this case, it is a digital input, active low as a data read select from the processor. See timing section.
$\overline{\text{WR}}$ (R/$\overline{\text{W}}$)(1)	20	I	This input is programmable. It functions as a read-write input (R/$\overline{\text{W}}$) and can also be configured as a write-only input ($\overline{\text{WR}}$), which is active low and used as data write select from the processor. In this case, the $\overline{\text{RD}}$ input is used as a read input from the processor. See timing section.

(1) The start-conditions of $\overline{\text{RD}}$ and $\overline{\text{WR}}$ (R/W) are unknown. The first access to the ADC has to be a write access to initialize the ADC.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION
vs
SAMPLING FREQUENCY (SINGLE-ENDED)

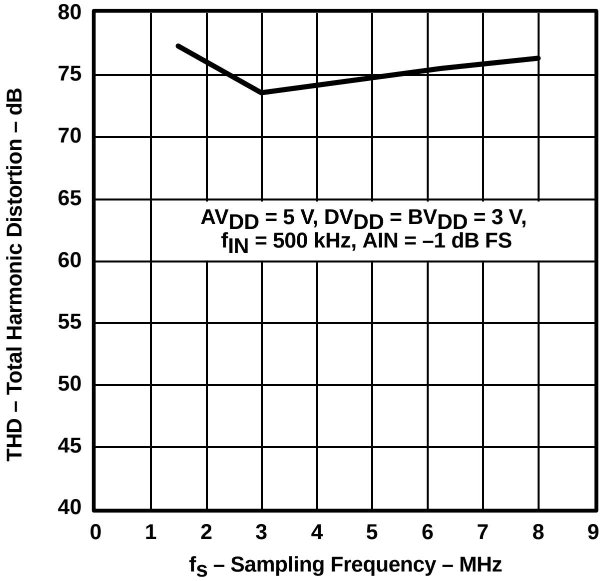


Figure 1

SIGNAL-TO-NOISE AND DISTORTION
vs
SAMPLING FREQUENCY (SINGLE-ENDED)

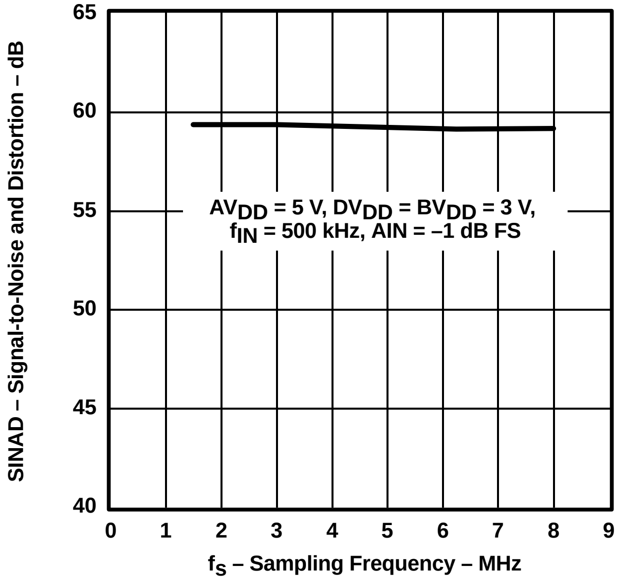


Figure 2

SPURIOUS FREE DYNAMIC RANGE
vs
SAMPLING FREQUENCY (SINGLE-ENDED)

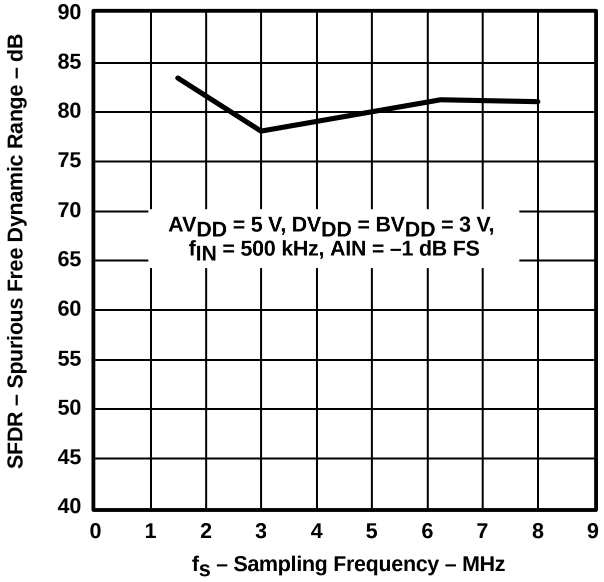


Figure 3

SIGNAL-TO-NOISE
vs
SAMPLING FREQUENCY (SINGLE-ENDED)

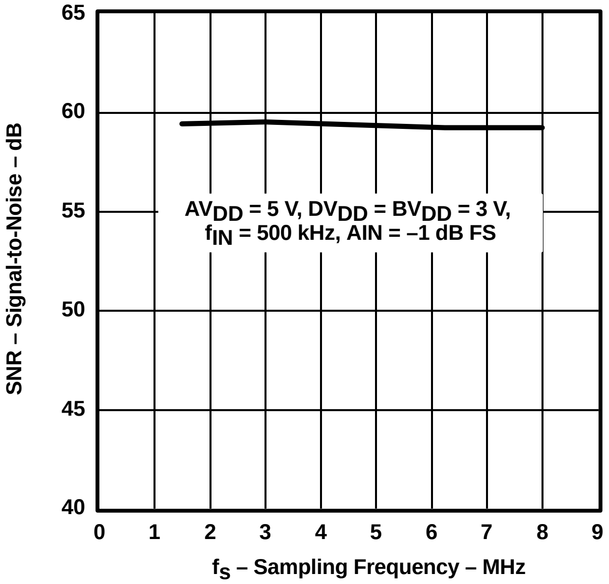


Figure 4

TYPICAL CHARACTERISTICS

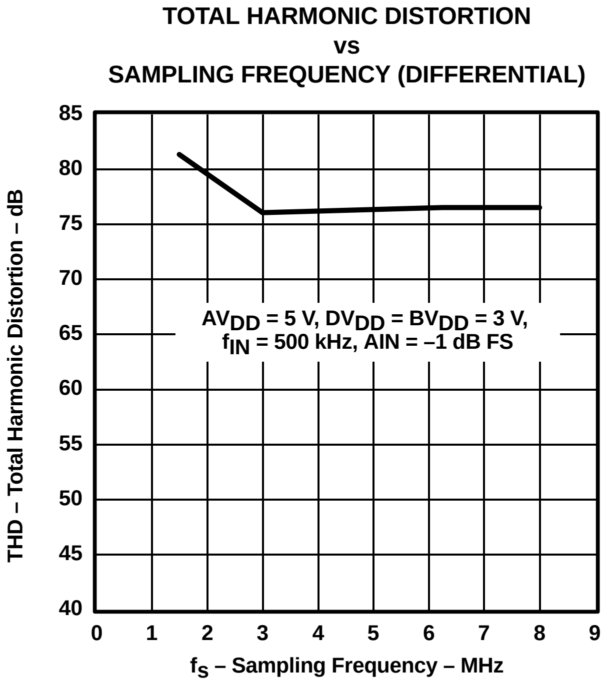


Figure 5

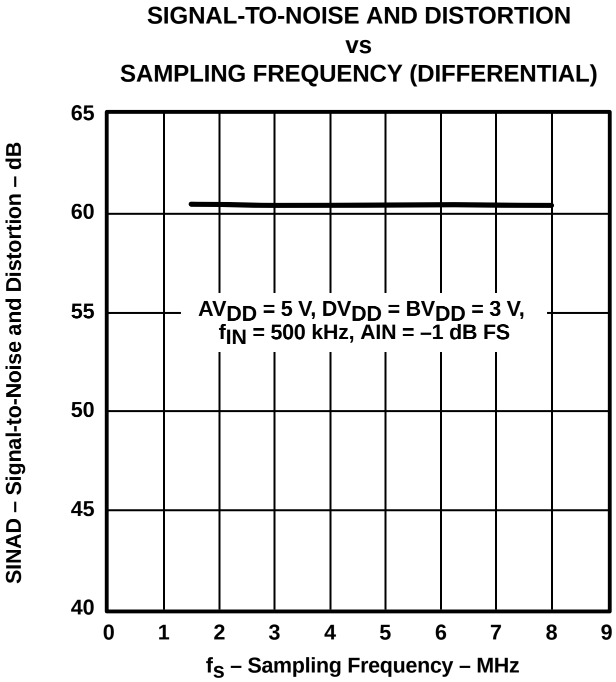


Figure 6

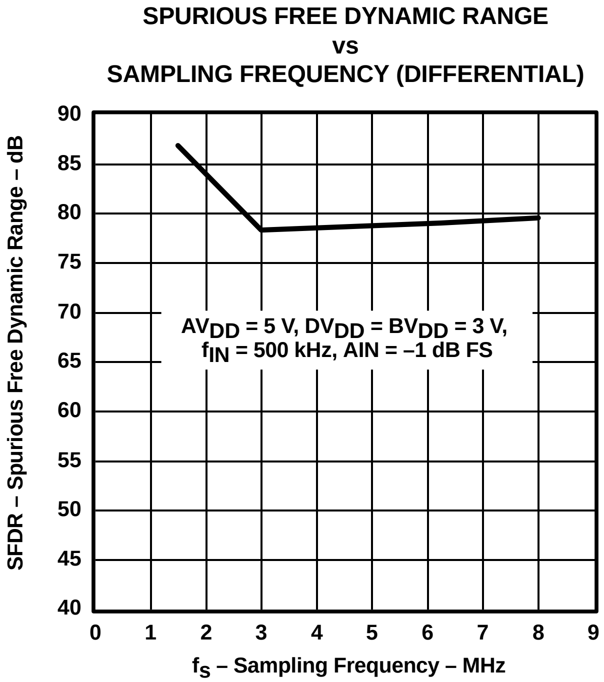


Figure 7

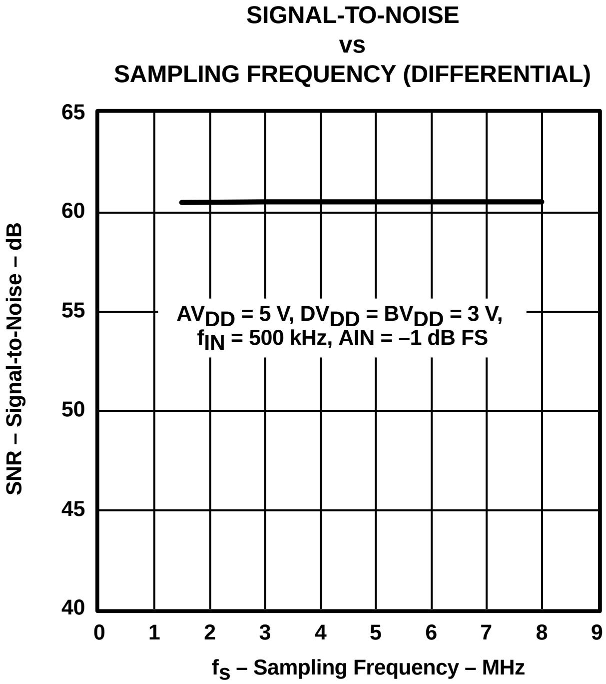


Figure 8

TYPICAL CHARACTERISTICS

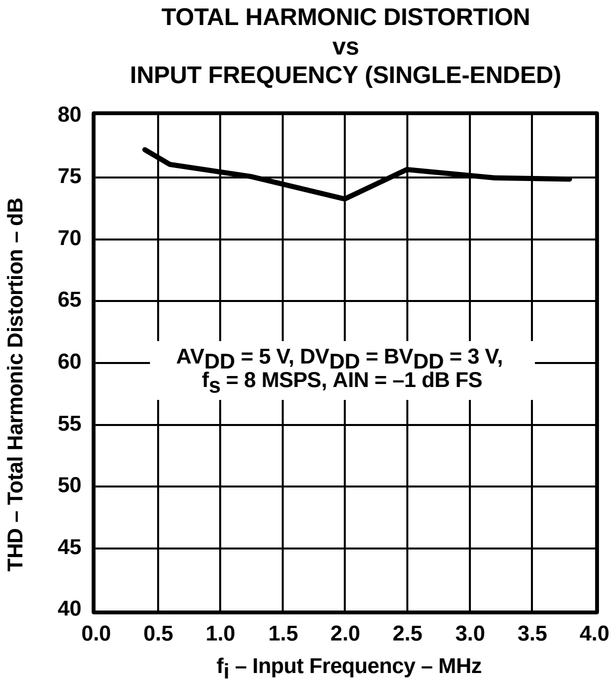


Figure 9

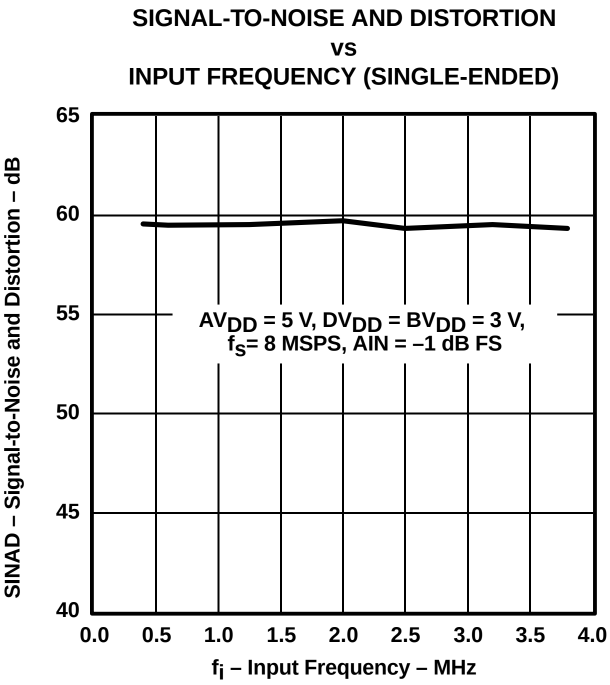


Figure 10

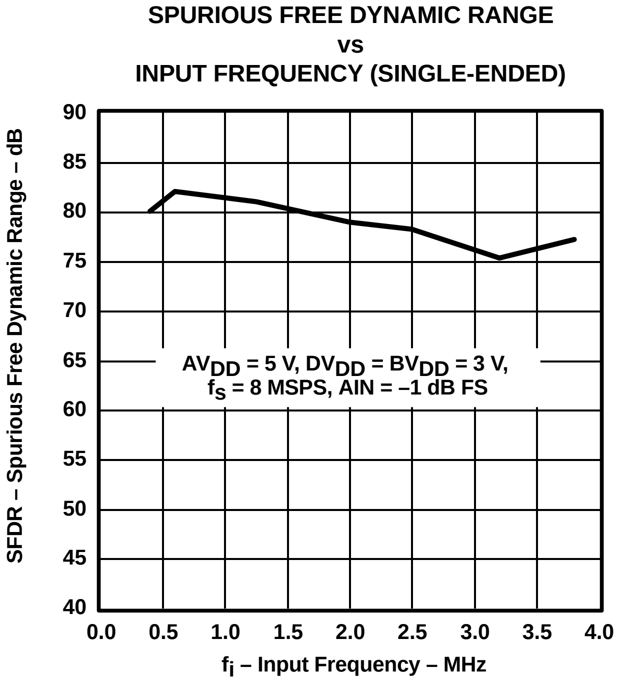


Figure 11

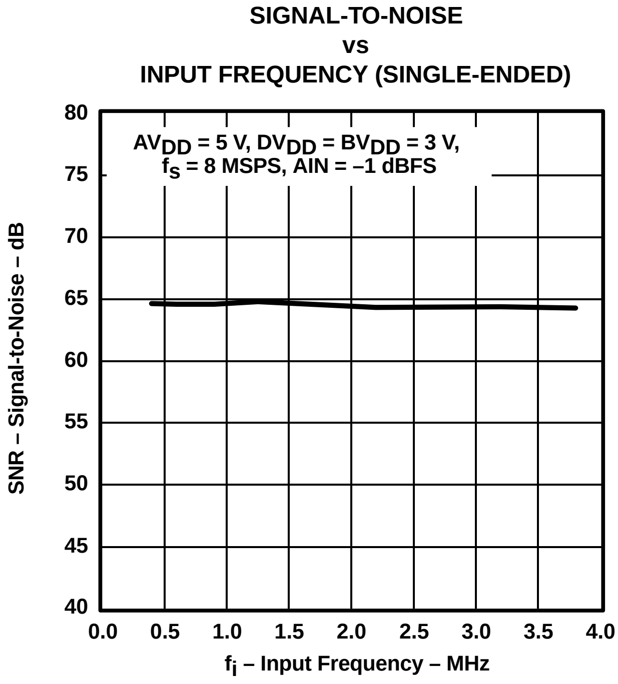


Figure 12

TYPICAL CHARACTERISTICS

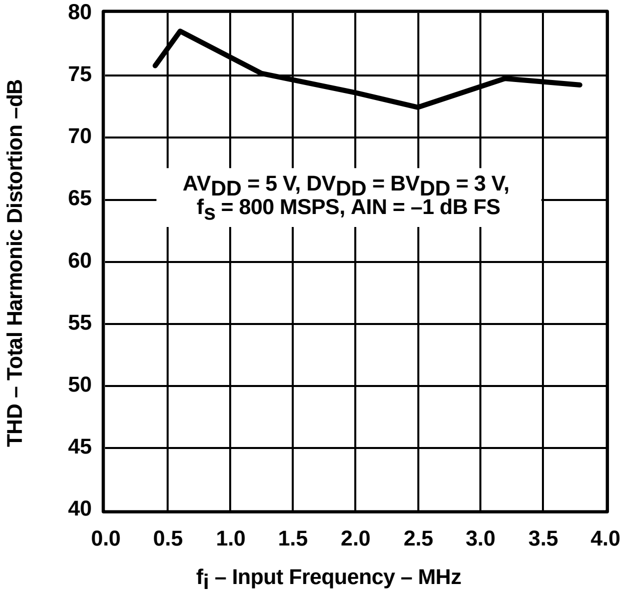

TOTAL HARMONIC DISTORTION
vs
INPUT FREQUENCY (DIFFERENTIAL)

Figure 13

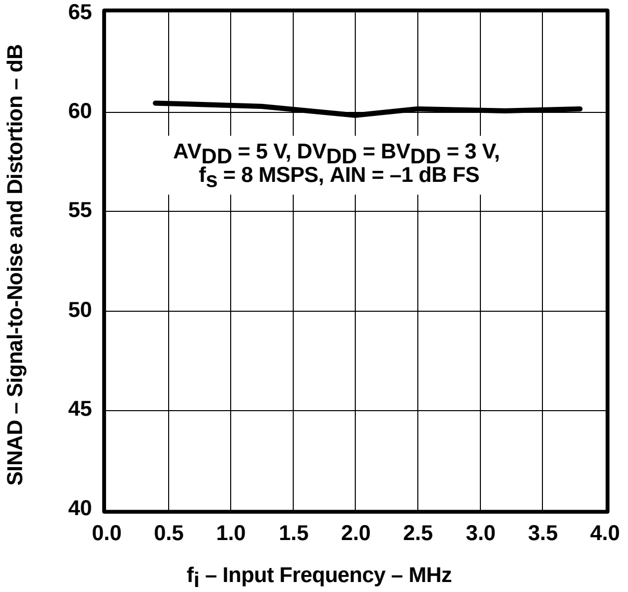

SIGNAL-TO-NOISE AND DISTORTION
vs
INPUT FREQUENCY (DIFFERENTIAL)

Figure 14

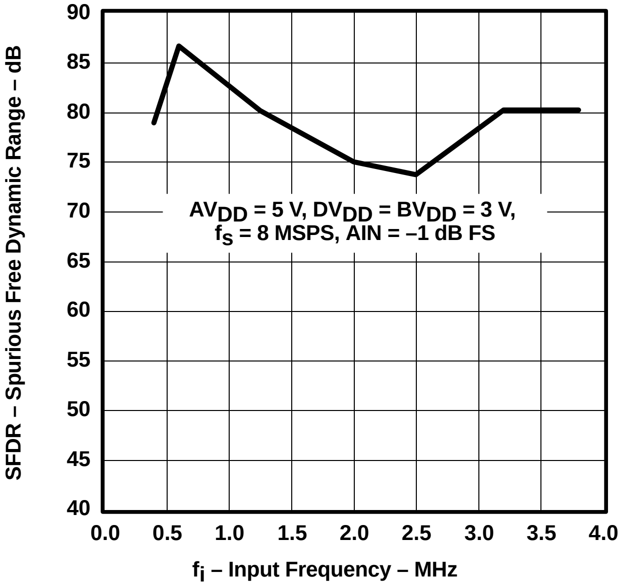

SPURIOUS FREE DYNAMIC RANGE
vs
INPUT FREQUENCY (DIFFERENTIAL)

Figure 15

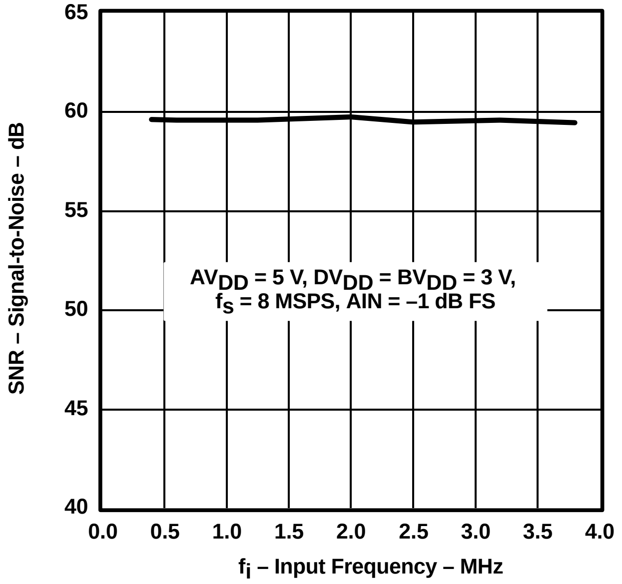

SIGNAL-TO-NOISE
vs
INPUT FREQUENCY (DIFFERENTIAL)

Figure 16

TYPICAL CHARACTERISTICS

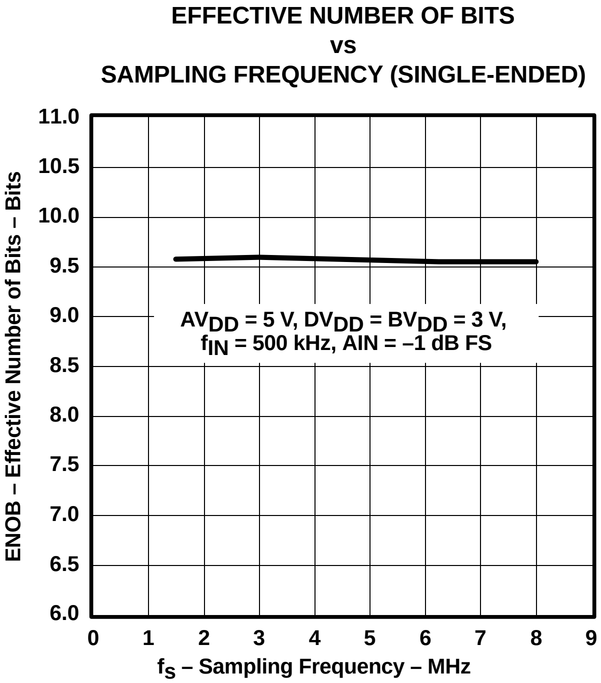


Figure 17

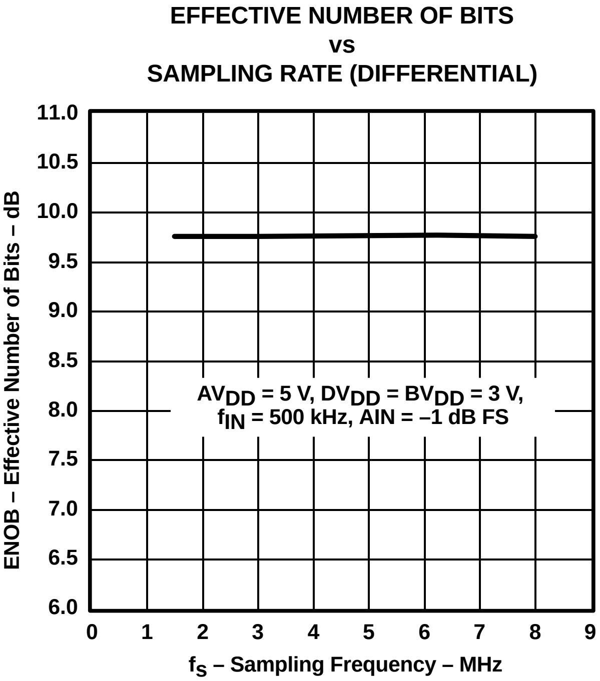


Figure 18

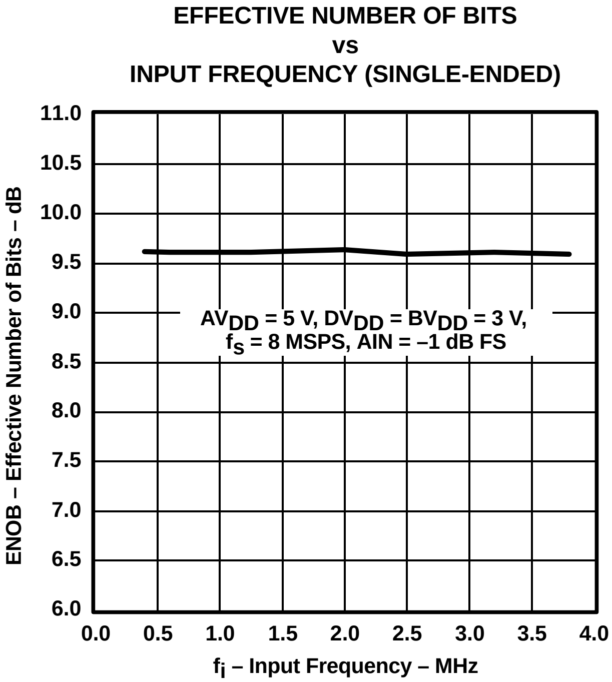


Figure 19

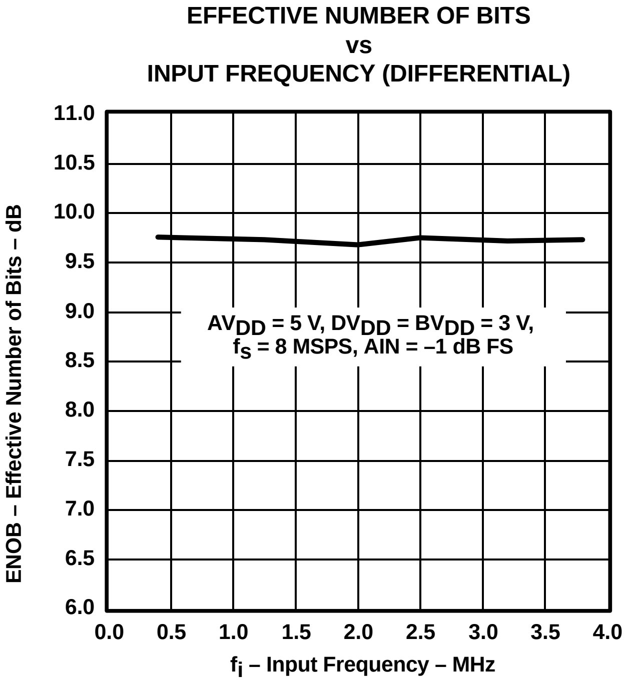


Figure 20

TYPICAL CHARACTERISTICS

DIFFERENTIAL NONLINEARITY
vs
ADC CODE

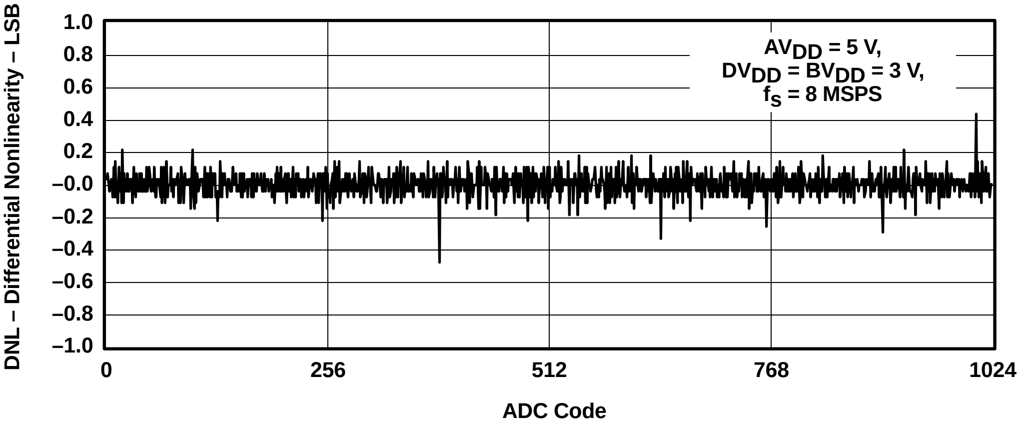


Figure 21

INTEGRAL NONLINEARITY
vs
ADC CODE

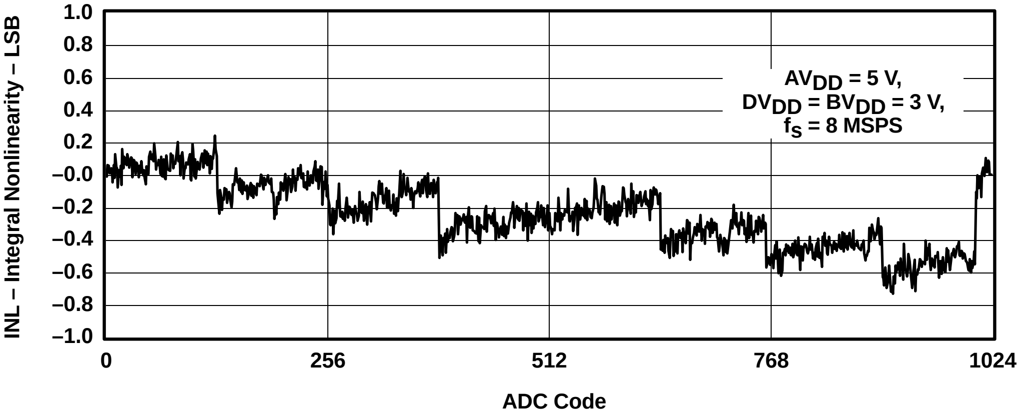


Figure 22

TYPICAL CHARACTERISTICS

FAST FOURIER TRANSFORM (4096 Points)
(SINGLE-ENDED)
vs
FREQUENCY

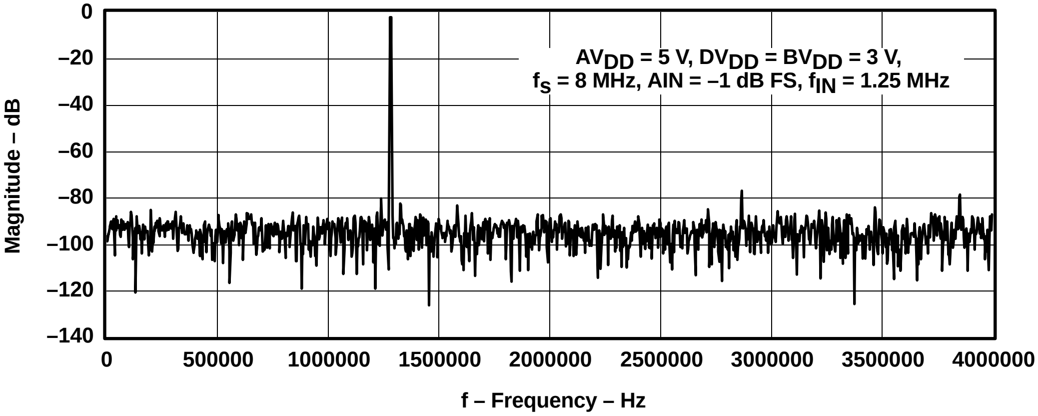


Figure 23

FAST FOURIER TRANSFORM (4096 Points)
(DIFFERENTIAL)
vs
FREQUENCY

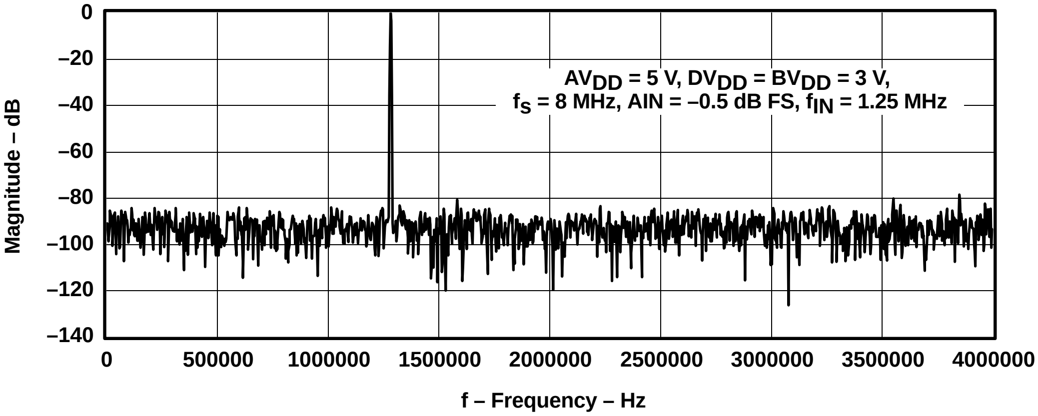


Figure 24

DETAILED DESCRIPTION

Reference Voltage

The THS1009 has a built-in reference, which provides the reference voltages for the ADC. VREFP is set to 3.5 V and VREFM is set to 1.5 V. An external reference can also be used through two reference input pins, REFP and REFM, if the reference source is programmed as external. The voltage levels applied to these pins establish the upper and lower limits of the analog inputs to produce a full-scale and zero-scale reading respectively.

Analog Inputs

The THS1009 consists of two analog inputs, which are sampled simultaneously. These inputs can be selected individually and configured as single-ended or differential inputs. The desired analog input channel can be programmed.

Converter

The THS1009 uses a 10-bit pipelined multistaged architecture which achieves a high sample rate with low power consumption. The THS1009 distributes the conversion over several smaller ADC sub-blocks, refining the conversion with progressively higher accuracy as the device passes the results from stage to stage. This distributed conversion requires a small fraction of the number of comparators used in a traditional flash ADC. A sample-and-hold amplifier (SHA) within each of the stages permits the first stage to operate on a new input sample while the second through the eighth stages operate on the seven preceding samples.

Conversion

An external clock signal with a duty cycle of 50% has to be applied to the clock input (CONV_CLK). A new conversion is started with every falling edge of the applied clock signal. The conversion values are available at the output with a latency of 5 clock cycles.

SYNC

In multichannel mode, the first SYNC signal is delayed by [7+ (# Channels Sampled)] cycles of the CONV_CLK after a SYNC reset. This is due to the latency of the pipeline architecture of the THS1009.

Sampling Rate

The maximum possible conversion rate per channel is dependent on the selected analog input channels. Table 1 shows the maximum conversion rate for the different combinations.

Table 1. Maximum Conversion Rate in Continuous Conversion Mode

CHANNEL CONFIGURATION	NUMBER OF CHANNELS	MAXIMUM CONVERSION RATE PER CHANNEL
1 single-ended channel	1	8 MSPS
2 single-ended channels	2	4 MSPS
1 differential channel	1	8 MSPS

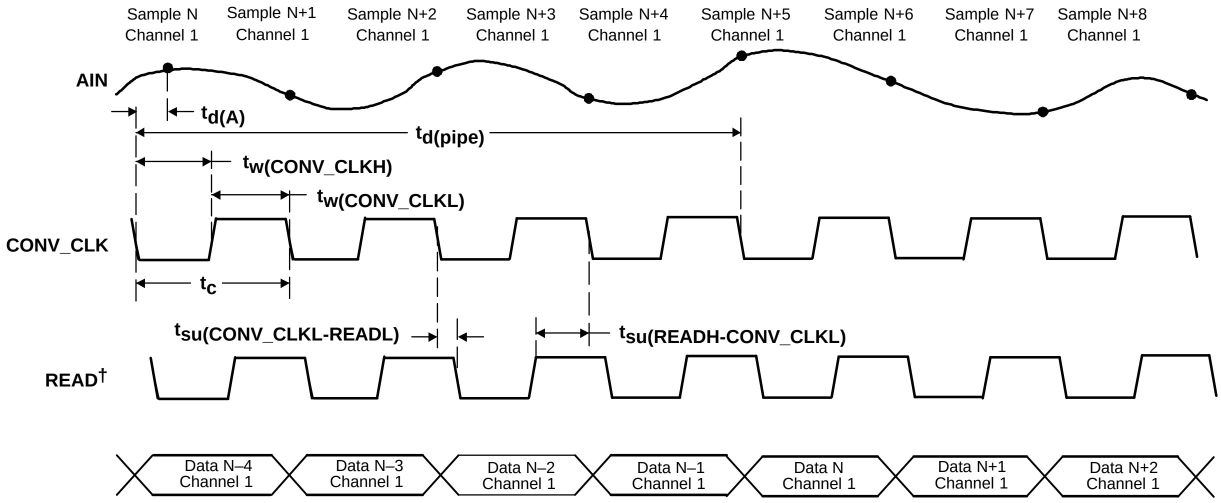
The maximum conversion rate per channel, fc, is given by:

$$\text{fc} = \frac{8\ \text{MSPS}}{\#\ \text{channels}}$$

Continuous Conversion Mode

During conversion the ADC operates with a free running external clock signal applied to the input CONV_CLK. With every falling edge of the CONV_CLK signal a new converted value is available to the databus with the corresponding read signal. The THS1009 offers up to two analog inputs to be selected. It is important to provide the channel information to the system; this means knowing which channel is available to the databus. To maintain this channel integrity, the THS1009 has an output signal SYNC, which is always active low if the data of channel 1 is applied to the databus.

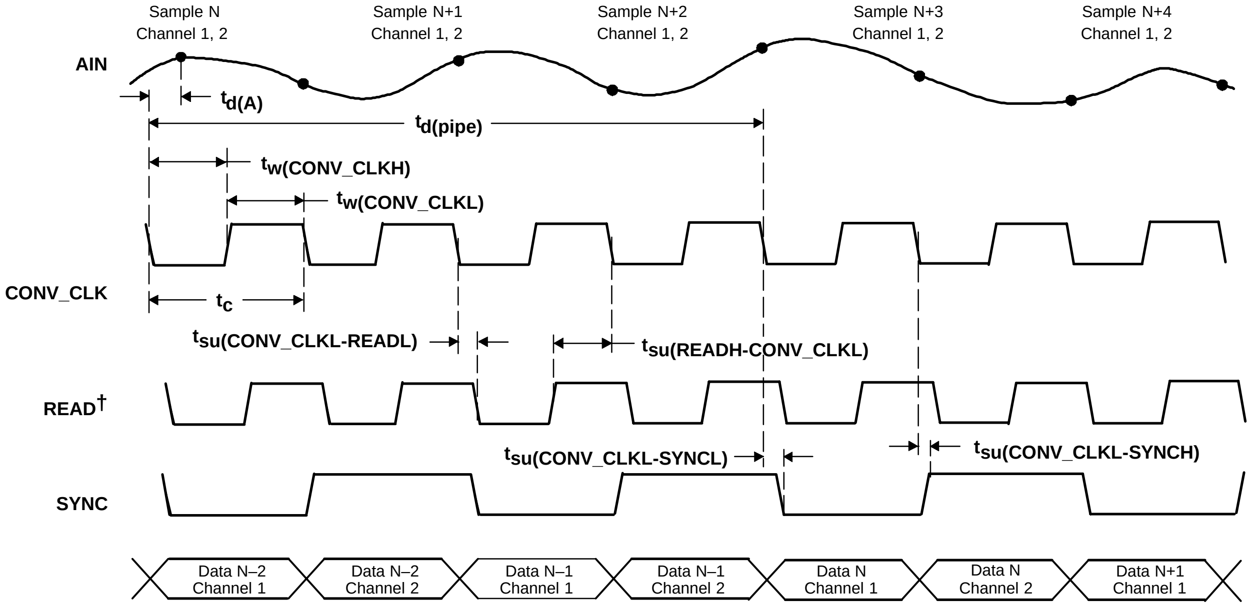
Figure 25 shows the timing of the conversion when one analog input channel is selected. The maximum throughput rate is 8 MSPS in this mode. The signal SYNC is disabled for the selection of one analog input since this information is not required for one analog input. There is a certain timing relationship required for the read signal with respect to the conversion clock. This can be seen in Figure 26 and the timing specification. A more detailed description of the timing is given in the section timing and signal description of the THS1009.



†READ is the logical combination from $\overline{CS0}$, CS1 and $\overline{RD}$

Figure 25. Conversion Timing in 1-Channel Operation

Figure 27 shows the conversion timing when two analog input channels are selected. The maximum throughput rate per channel is 4 MSPS in this mode. The data flow in the bottom of the figure shows the order the converted data is available to the data bus. This can be seen in Figure 26 and Table 2. A more detailed description of the timing is given in the section timing and signal description of the THS1009.



†READ is the logical combination from $\overline{CS0}$, CS1 and $\overline{RD}$

Figure 26. Conversion Timing in 2-Channel Operation

DIGITAL OUTPUT DATA FORMAT

The digital output data format of the THS1009 can either be in binary format or in twos complement format. The following tables list the digital outputs for the analog input voltages.

Table 2. Binary Output Format for Single-Ended Configuration

SINGLE-ENDED, BINARY OUTPUT	
ANALOG INPUT VOLTAGE	DIGITAL OUTPUT CODE
AIN = V_{REFP}	3FFh
AIN = (V_{REFP} + V_{REFM})/2	200h
AIN = V_{REFM}	000h

Table 3. Twos Complement Output Format for Single-Ended Configuration

SINGLE-ENDED, TWOS COMPLEMENT	
ANALOG INPUT VOLTAGE	DIGITAL OUTPUT CODE
AIN = V_{REFP}	1FFh
AIN = (V_{REFP} + V_{REFM})/2	000h
AIN = V_{REFM}	200h

Table 4. Binary Output Format for Differential Configuration

DIFFERENTIAL, BINARY OUTPUT	
ANALOG INPUT VOLTAGE	DIGITAL OUTPUT CODE
V_{in} = AINP – AINM V_{REF} = V_{REFP} – V_{REFM}	
V_{in} = V_{REF}	3FFh
V_{in} = 0	200h
V_{in} = $-V_{REF}$	000h

Table 5. Twos Complement Output Format for Differential Configuration

DIFFERENTIAL, BINARY OUTPUT	
ANALOG INPUT VOLTAGE	DIGITAL OUTPUT CODE
V_{in} = AINP – AINM V_{REF} = V_{REFP} – V_{REFM}	
V_{in} = V_{REF}	1FFh
V_{in} = 0	000h
V_{in} = $-V_{REF}$	200h

ADC CONTROL REGISTER

The THS1009 contains two 10-bit wide control registers (CR0, CR1) in order to program the device into the desired mode. The bit definitions of both control registers are shown in Table 6.

Table 6. Bit Definitions of Control Register CR0 and CR1

REG	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CR0	TEST1	TEST0	SCAN	DIFF1	DIFF0	CHSEL1	CHSEL0	PD	RES	VREF
CR1	RESERVED	OFFSET	BIN/2’s	R/W	RES	RES	RES	RES	SRST	RESET

Writing to Control Register 0 and Control Register 1

The 10-bit wide control register 0 and control register 1 can be programmed by addressing the desired control register and writing the register value to the ADC. The addressing is performed with the upper bits RA0 and RA1. During this write process, the data bits D0 to D9 contain the desired control register value. Table 7 shows the addressing of each control register.

Table 7. Control Register Addressing

D0 – D9	RA0	RA1	Addressed Control Register
Desired register value	0	0	Control register 0
Desired register value	1	0	Control register 1
Desired register value	0	1	Reserved for future
Desired register value	1	1	Reserved for future

INITIALIZATION OF THE THS1009

The initialization of the THS1009 should be done according to the configuration flow shown in Figure 27.

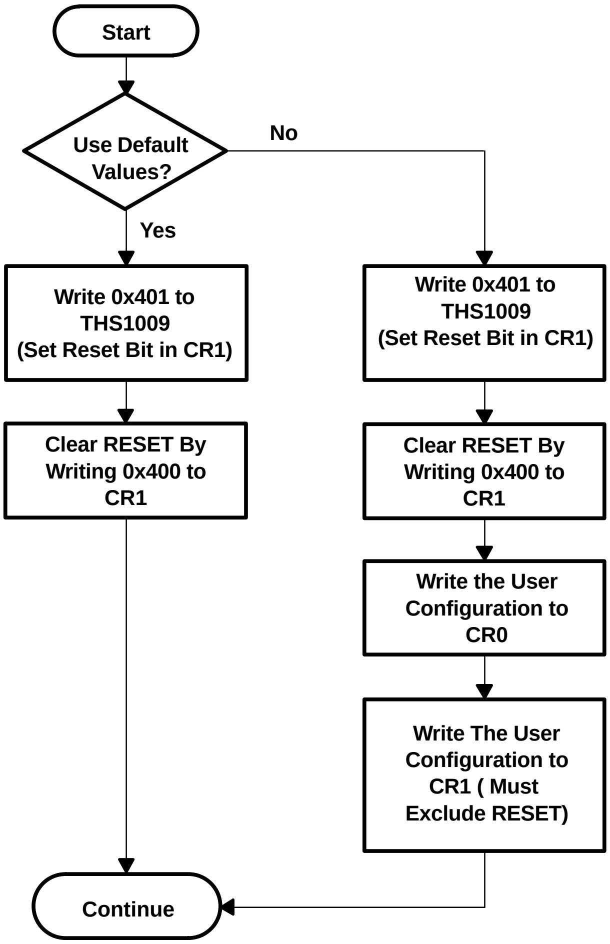


Figure 27. THS1009 Configuration Flow

ADC CONTROL REGISTERS

Control Register 0, Write Only (see Table 8)

BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	TEST1	TEST0	SCAN	DIFF1	DIFF0	CHSEL1	CHSEL0	PD	RES	VREF

Table 8. Control Register 0 Bit Functions

BITS	RESET VALUE	NAME	FUNCTION
0	0	VREF	Vref select: Bit 0 = 0 → The internal reference is used Bit 0 = 1 → The external reference voltage is used for the ADC
1	0	RES	Reserved
2	0	PD	Power down. Bit 2 = 0 → The ADC is active Bit 2 = 1 → Power down The reading and writing to and from the digital outputs is possible during power down.
3, 4	0,0	CHSEL0, CHSEL1	Channel select Bit 3 and bit 4 select the analog input channel of the ADC. Refer to Table 9.
5,6	1,0	DIFF0, DIFF1	Number of differential channels Bit 5 and bit 6 contain information about the number of selected differential channels. Refer to Table 9.
7	0	SCAN	Autoscan enable Bit 7 enables or disables the autoscan function of the ADC. Refer to Table 9.
8,9	0,0	TEST0, TEST1	Test input enable Bit 8 and bit 9 control the test function of the ADC. Three different test voltages can be measured. This feedback allows the check of all hardware connections and the ADC operation. Refer to Table 10 for selection of the three different test voltages.

ANALOG INPUT CHANNEL SELECTION

The analog input channels of the THS1009 can be selected via bits 3 to 7 of control register 0. One single channel (single-ended or differential) is selected via bit 3 and bit 4 of control register 0. Bit 5 controls the selection between single-ended and differential configuration. Bit 6 and bit 7 select the autoscan mode, if more than one input channel is selected. Table 9 shows the possible selections.

Table 9. Analog Input Channel Configurations

BIT 7 SCAN	BIT 6 DIFF1	BIT 5 DIFF0	BIT 4 CHSEL1	BIT 3 CHSEL0	DESCRIPTION OF THE SELECTED INPUTS
0	0	0	0	0	Analog input AINP (single ended)
0	0	0	0	1	Analog input AINM (single ended)
0	0	0	1	0	Reserved
0	0	0	1	1	Reserved
0	0	1	0	0	Differential channel (AINP–AINM)
0	0	1	0	1	Reserved
1	0	0	0	1	Autoscan two single ended channels: AINP, AINM, AINP, …
1	0	0	1	0	Reserved
1	0	0	1	1	Reserved
1	0	1	0	1	Reserved
1	0	1	1	0	Reserved
1	1	0	0	1	Reserved
0	0	1	1	0	Reserved
0	0	1	1	1	Reserved
1	0	0	0	0	Reserved
1	0	1	0	0	Reserved
1	0	1	1	1	Reserved
1	1	0	0	0	Reserved
1	1	0	1	0	Reserved
1	1	0	1	1	Reserved
1	1	1	0	0	Reserved
1	1	1	0	1	Reserved
1	1	1	1	0	Reserved
1	1	1	1	1	Reserved

Test Mode

The test mode of the ADC is selected via bit 8 and bit 9 of control register 0. The different selections are shown in Table 10.

Table 10. Test Mode

BIT 9 TEST1	BIT 8 TEST0	OUTPUT RESULT
0	0	Normal mode
0	1	V_{REFP}
1	0	$((V_{REFM})+(V_{REFP}))/2$
1	1	V_{REFM}

Three different options can be selected. This feature allows support testing of hardware connections between the ADC and the processor.

Control Register 1, Write Only (see Table 11)

BIT11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	1	RESERVED	OFFSET	BIN/2s	R/$\overline{W}$	RES	RES	RES	RES	SRST	RESET

Table 11. Control Register 1 Bit Functions

BITS	RESET VALUE	NAME	FUNCTION
0	0	RESET	Reset Writing a 1 into this bit resets the device and sets the control register 0 and control register 1 to the reset values. To bring the device out of RESET, a 0 has to be written into this bit.
1	0	SRST	Writing a 1 into this bit resets the sync generator. When running in multichannel mode, this must be set during the configuration cycle.
2, 3	0,0	RES	Reserved
4	1	RES	Reserved
5	1	RES	Reserved
6	0	R/$\overline{W}$	R/$\overline{W}$, RD/$\overline{WR}$ selection Bit 6 of control register 1 controls the function of the inputs $\overline{RD}$ and $\overline{WR}$. When bit 6 in control register 1 is set to 1, $\overline{WR}$ becomes a R/$\overline{W}$ input and $\overline{RD}$ is disabled. From now on a read is signalled with R/W high and a write with R/W as a low signal. If bit 6 in control register 1 is set to 0, the input $\overline{RD}$ becomes a read input and the input $\overline{WR}$ becomes a write input.
7	0	BIN/2s	Complement select If bit 7 of control register 1 is set to 0, the output value of the ADC is in twos complement. If bit 7 of control register 1 is set to 1, the output value of the ADC is in binary format. Refer to Table 2 through Table 5.
8	0	OFFSET	Offset cancellation mode Bit 8 = 0 → normal conversion mode Bit 8 = 1 → offset calibration mode If a 1 is written into bit 8 of control register 1, the device internally sets the inputs to zero and does a conversion. The conversion result is stored in an offset register and subtracted from all conversions in order to reduce the offset error.
9	0	RESERVED	Always write 0.

TIMING AND SIGNAL DESCRIPTION OF THE THS1009

The reading from the THS1009 and writing to the THS1009 is performed by using the chip select inputs ($\overline{\text{CS0}}$, CS1), the write input $\overline{\text{WR}}$ and the read input $\overline{\text{RD}}$. The write input is configurable to a combined read/write input (R/$\overline{\text{W}}$). This is desired in cases where the connected processor consists of a combined read/write output signal (R/$\overline{\text{W}}$). The two chip select inputs can be used to interface easily to a processor.

Reading from the THS1009 takes place by an internal $\overline{\text{RD}}_{\text{int}}$ signal, which is generated from the logical combination of the external signals $\overline{\text{CS0}}$, CS1 and $\overline{\text{RD}}$ (see Figure 28). This signal is then used to strobe out the words and to enable the output buffers. The last external signal (either $\overline{\text{CS0}}$, CS1 or $\overline{\text{RD}}$) to become valid makes $\overline{\text{RD}}_{\text{int}}$ active while the write input ($\overline{\text{WR}}$) is inactive. The first of those external signals switching to its inactive state deactivates $\overline{\text{RD}}_{\text{int}}$ again.

Writing to the THS1009 takes place by an internal $\overline{\text{WR}}_{\text{int}}$ signal, which is generated from the logical combination of the external signals $\overline{\text{CS0}}$, CS1 and $\overline{\text{WR}}$. This signal strobes the control words into the control registers 0 and 1. The last external signal (either $\overline{\text{CS0}}$, CS1 or $\overline{\text{WR}}$) to become valid switches $\overline{\text{WR}}_{\text{int}}$ active while the read input (RD) is inactive. The first of those external signals going to its inactive state deactivates $\overline{\text{WR}}_{\text{int}}$ again.

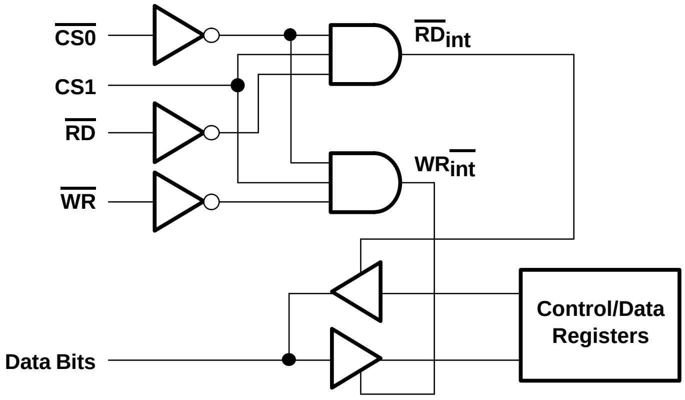


Figure 28. Logical Combination of $\overline{\text{CS0}}$, CS1, $\overline{\text{RD}}$, and $\overline{\text{WR}}$

Read Timing (using $\overline{\text{RD}}$, $\overline{\text{RD}}$-controlled)

Figure 29 shows the read-timing behavior when the $\overline{\text{WR}}$(R/$\overline{\text{W}}$) input is programmed as a write-input only. The input $\overline{\text{RD}}$ acts as the read-input in this configuration. This timing is called $\overline{\text{RD}}$-controlled because $\overline{\text{RD}}$ is the last external signal of $\overline{\text{CS0}}$, CS1, and $\overline{\text{RD}}$ which becomes valid.

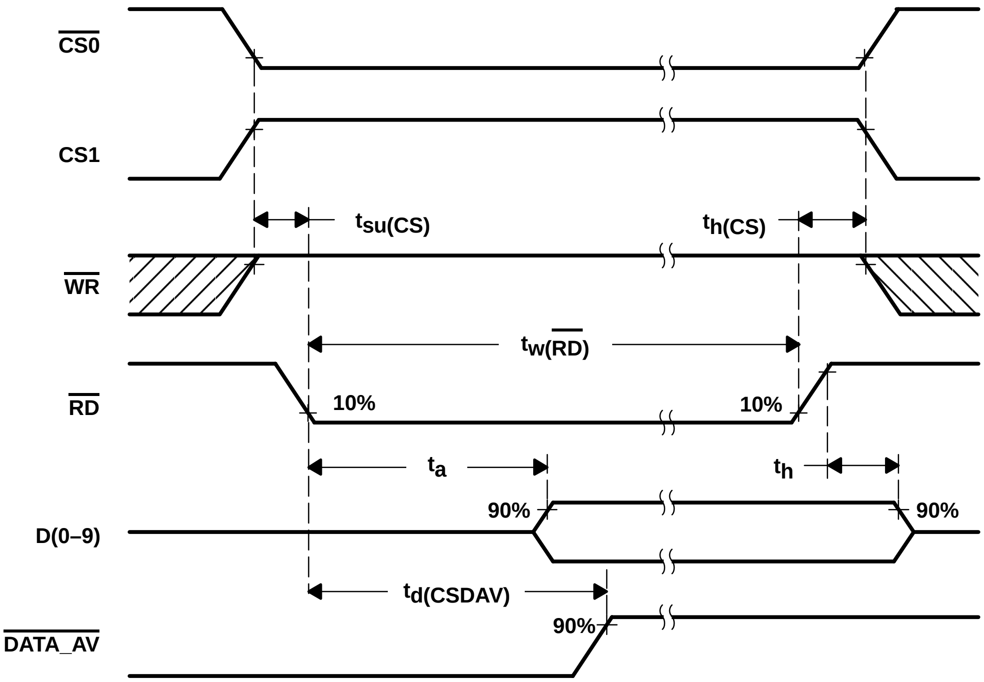


Figure 29. Read Timing Diagram Using $\overline{\text{RD}}$ ($\overline{\text{RD}}$-controlled)

Read Timing Parameter ($\overline{\text{RD}}$-controlled)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{su(CS)}$	Setup time, $\overline{\text{RD}}$ low to last CS valid	0			ns
t_a	Access time, last CS valid to data valid	0		10	ns
$t_{d(CSDAV)}$	Delay time, last CS valid to DATA_AV inactive		12		ns
t_h	Hold time, first CS invalid to data invalid	0		5	ns
$t_{h(CS)}$	Hold time, $\overline{\text{RD}}$ change to first CS invalid	5			ns
$t_{w(\overline{RD})}$	Pulse duration, $\overline{\text{RD}}$ active	10			ns

Write Timing (using $\overline{\text{WR}}$, $\overline{\text{WR}}$-controlled)

Figure 30 shows the write-timing behavior when the $\overline{\text{WR}}$(R/$\overline{\text{W}}$) input is programmed as a write input $\overline{\text{WR}}$ only. The input $\overline{\text{RD}}$ acts as the read input in this configuration. This timing is called $\overline{\text{WR}}$-controlled because $\overline{\text{WR}}$ is the last external signal of $\overline{\text{CS0}}$, CS1, and $\overline{\text{WR}}$ which becomes valid.

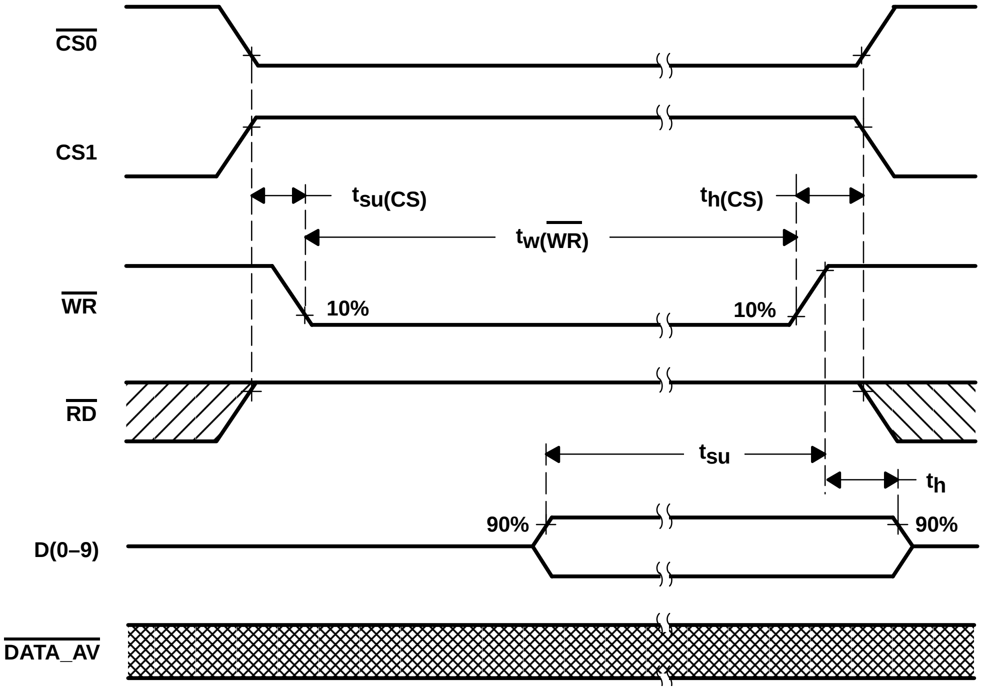


Figure 30. Write Timing Diagram Using $\overline{\text{WR}}$ ($\overline{\text{WR}}$-controlled)

Write Timing Parameter Using $\overline{\text{WR}}$ ($\overline{\text{WR}}$-controlled)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{su(CS)}$	Setup time, CS stable to last $\overline{\text{WR}}$ valid	0			ns
t_{su}	Setup time, data valid to first $\overline{\text{WR}}$ invalid	5			ns
t_h	Hold time, $\overline{\text{WR}}$ invalid to data invalid	2			ns
$t_{h(CS)}$	Hold time, $\overline{\text{WR}}$ invalid to CS change	5			ns
$t_{w(\overline{WR})}$	Pulse duration, $\overline{\text{WR}}$ active	10			ns

Read Timing (using R/$\overline{\text{W}}$, $\overline{\text{CS0}}$-controlled)

Figure 31 shows the read-timing behavior when the $\overline{\text{WR}}$(R/$\overline{\text{W}}$) input is programmed as a combined read-write input R/$\overline{\text{W}}$. The $\overline{\text{RD}}$ input has to be tied to high-level in this configuration. This timing is called $\overline{\text{CS0}}$-controlled because $\overline{\text{CS0}}$ is the last external signal of $\overline{\text{CS0}}$, CS1, and R/$\overline{\text{W}}$ which becomes valid. The reading of the data should be done with a certain timing relative to the conversion clock CONV_CLK, as illustrated in Figure 31.

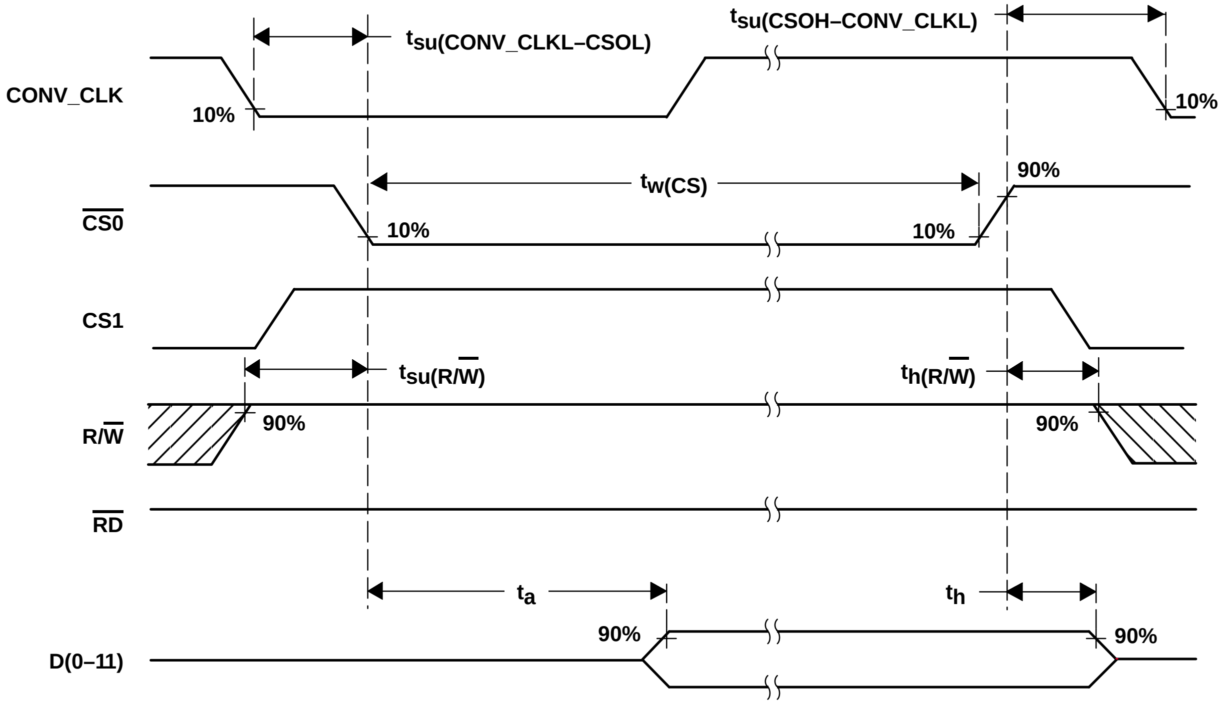


Figure 31. Read Timing Diagram Using R/$\overline{\text{W}}$ ($\overline{\text{CS0}}$-controlled)

Read Timing Parameter ($\overline{\text{CS0}}$-controlled)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{su(CONV\_CLKL–CSOL)}$	Setup time, CONV_CLK low before CS valid	10			ns
$t_{su(CSOH–CONV\_CLKL)}$	Setup time, CS invalid to CONV_CLK low	20			ns
$t_{su(R/\overline{W})}$	Setup time, R/$\overline{\text{W}}$ high to last CS valid	0			ns
t_a	Access time, last CS valid to data valid	0		10	ns
t_h	Hold time, first CS invalid to data invalid	0		5	ns
$t_{h(R/\overline{W})}$	Hold time, first external CS invalid to R/$\overline{\text{W}}$ change	5			ns
$t_{w(CS)}$	Pulse duration, CS active	10			ns

Write Timing (using R/$\overline{\text{W}}$, $\overline{\text{CS0}}$-controlled)

Figure 32 shows the write-timing behavior when the $\overline{\text{WR}}$(R/$\overline{\text{W}}$) input is programmed as a combined read-write input R/$\overline{\text{W}}$. The $\overline{\text{RD}}$ input has to be tied to high-level in this configuration. This timing is called $\overline{\text{CS0}}$-controlled because $\overline{\text{CS0}}$ is the last external signal of $\overline{\text{CS0}}$, CS1, and R/$\overline{\text{W}}$ which becomes valid. The write into the THS1009 can be performed irrespective of the conversion clock signal CONV_CLK.

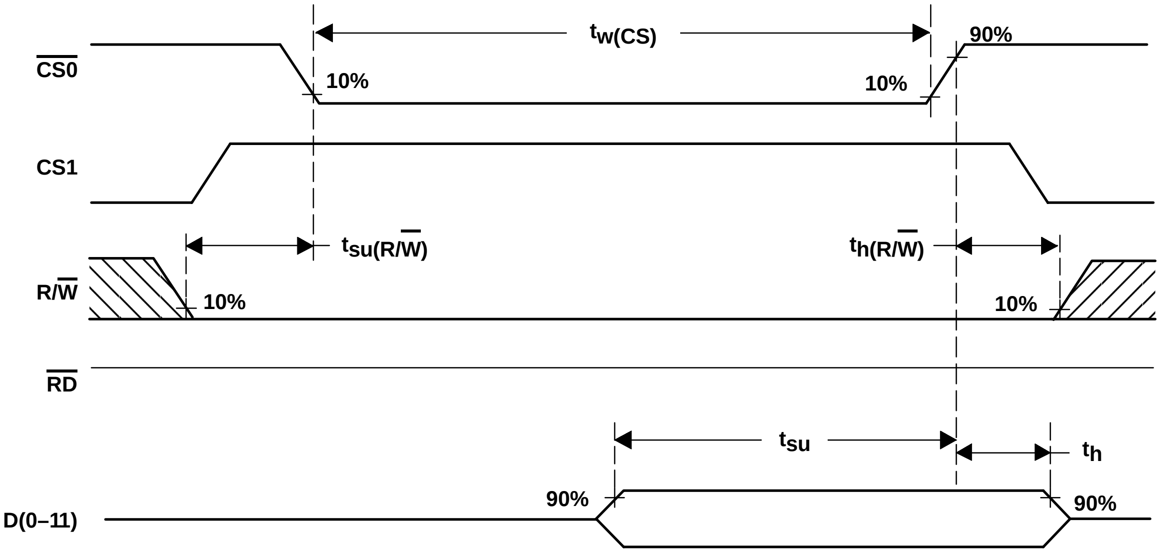


Figure 32. Write Timing Diagram Using R/$\overline{\text{W}}$ ($\overline{\text{CS0}}$-controlled)

Write Timing Parameter ($\overline{\text{CS0}}$-controlled)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{su(R/\overline{W})}$	Setup time, R/$\overline{\text{W}}$ stable to last CS valid	0			ns
t_{su}	Setup time, data valid to first CS invalid	5			ns
t_h	Hold time, first CS invalid to data invalid	2			ns
$t_{h(R/\overline{W})}$	Hold time, first CS invalid to R/$\overline{\text{W}}$ change	5			ns
$t_{w(CS)}$	Pulse duration, CS active	10			ns

ANALOG INPUT CONFIGURATION AND REFERENCE VOLTAGE

The THS1009 features two analog input channels. These can be configured for either single-ended or differential operation. Figure 33 shows a simplified model, where a single-ended configuration for channel AINP is selected. The reference voltages for the ADC itself are V_{REFP} and V_{REFM} (either internal or external reference voltage). The analog input voltage range is between V_{REFM} to V_{REFP}. This means that V_{REFM} defines the minimum voltage and V_{REFP} defines the maximum voltage, which can be applied to the ADC. The internal reference source provides the voltage V_{REFM} of 1.5 V and the voltage V_{REFP} of 3.5 V (see also section Reference Voltage). The resulting analog input voltage swing of 2 V can be expressed by:

$$V_{REFM} \le AINP \le V_{REFP} \qquad (1)$$

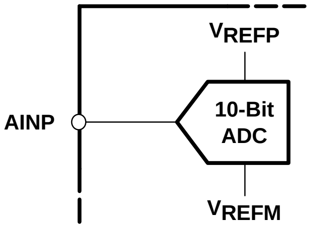


Figure 33. Single-Ended Input Stage

A differential operation is desired for many applications due to better signal-to-noise ration. Figure 34 shows a simplified model for the analog inputs AINM and AINP, which are configured for differential operation. The differential operation mode provides in terms of performance benefits over the single-ended mode and is therefore recommended for best performance. The THS1009 offers 1 differential analog input and in the single-ended mode 2 analog inputs. If the analog input architecture is differential, common-mode noise and common-mode voltages can be rejected. Additional details for both modes are given below.

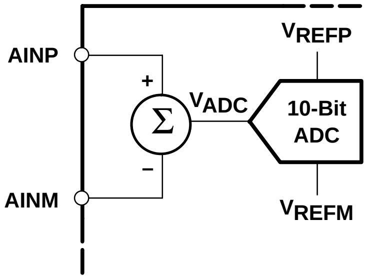


Figure 34. Differential Input Stage

In comparison to the single-ended configuration it can be seen that the voltage, V_{ADC}, which is applied at the input of the ADC is the difference between the input AINP and AINM. The voltage V_{ADC} can be calculated as follows:

$$V_{ADC} = ABS(AINP–AINM) \qquad (2)$$

An advantage to single-ended operation is that the common-mode voltage

$$V_{CM} = \frac{AINM + AINP}{2} \qquad (3)$$

can be rejected in the differential configuration, if the following condition for the analog input voltages is true:

$$AGND \le AINM,\ AINP \le AV_{DD} \qquad (4)$$

$$1\ V \le V_{CM} \le 4\ V \qquad (5)$$

SINGLE-ENDED MODE OF OPERATION

The THS1009 can be configured for single-ended operation using dc or ac coupling. In either case, the input of the THS1009 should be driven from an operational amplifier that does not degrade the ADC performance. Because the THS1009 operates from a 5-V single supply, it is necessary to level-shift ground-based bipolar signals to comply with its input requirements. This can be achieved with dc- and ac-coupling.

DC COUPLING

An operational amplifier can be configured to shift the signal level according to the analog input voltage range of the THS1009. The analog input voltage range of the THS1009 goes from 1.5 V to 3.5 V. An operational amplifier can be used as shown in Figure 35.

Figure 35 shows an example with the analog input signal in the range between –1 V and 1 V. The signal is shifted by an operational amplifier to the analog input range of the THS1009 (1.5 V to 3.5 V). The operational amplifier is configured as an inverting amplifier with a gain of –1. The required dc voltage of 1.25 V at the noninverting input is derived from the 2.5-V output reference REFOUT of the THS1009 by using a resistor divider. Therefore, the operational amplifier output voltage is centered at 2.5 V. The 10 µF tantalum capacitor is required for bypassing REFOUT. REFIN of the THS1009 must be connected directly to REFOUT in single-ended mode. The use of ratio matched, thin-film resistor networks minimizes gain and offset errors.

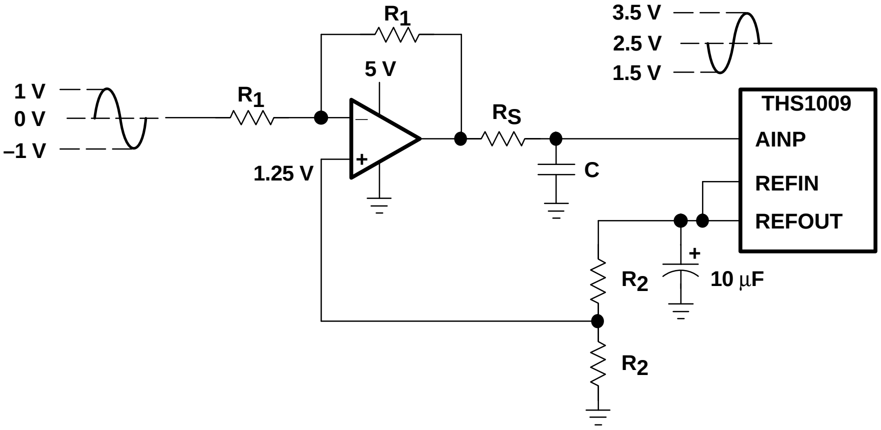


Figure 35. Level-Shift for DC-Coupled Input

DIFFERENTIAL MODE OF OPERATION

For the differential mode of operation, a conversion from single-ended to differential is required. A conversion to differential signals can be achieved by using an RF-transformer, which provides a center tap. Best performance is achieved in differential mode.

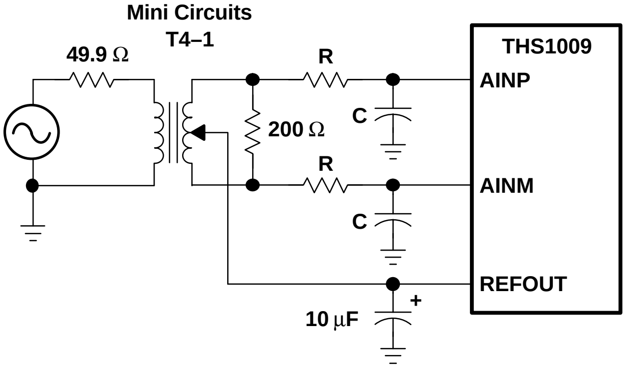


Figure 36. Transformer Coupled Input

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS1009IDA	ACTIVE	TSSOP	DA	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS1009I	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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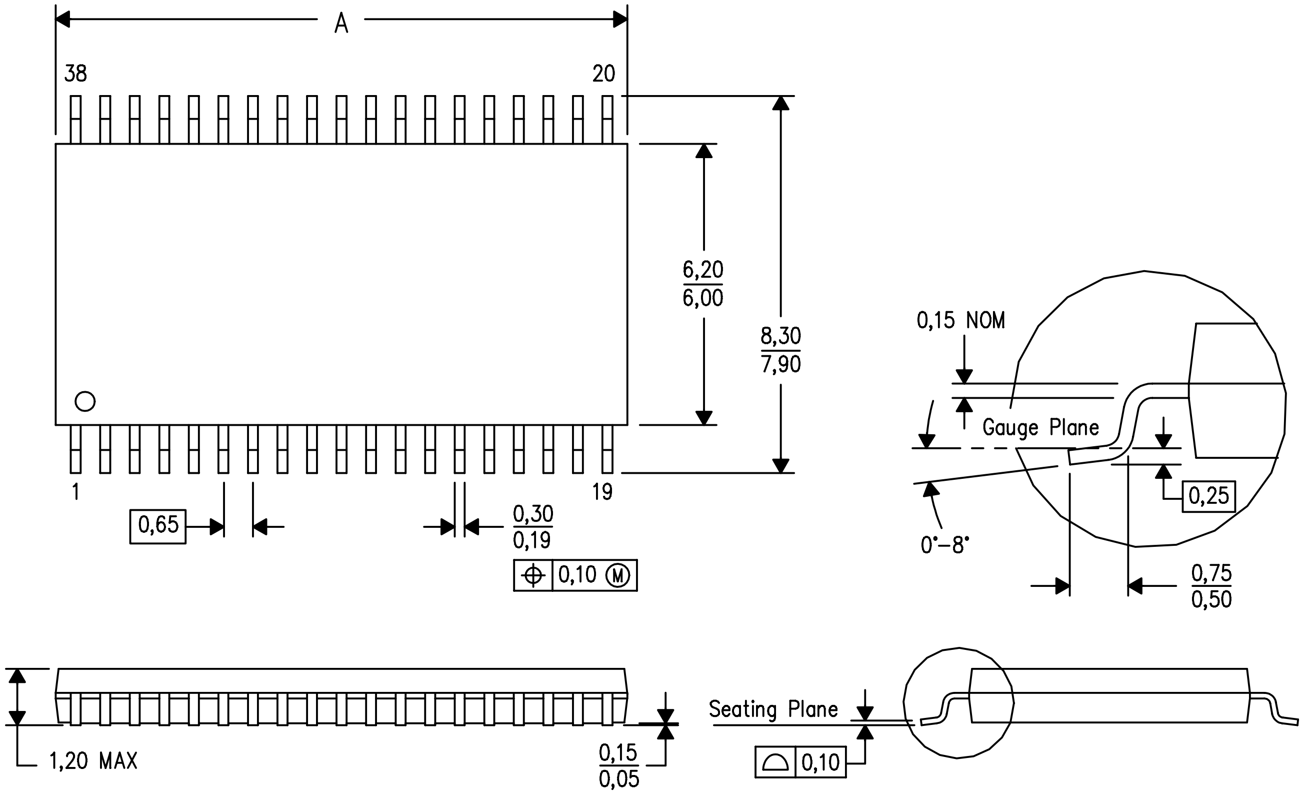
DA (R–PDSO–G**) PLASTIC SMALL–OUTLINE PACKAGE

38 PIN SHOWN



PINS ** / DIM	30	32	38
A MAX	11,10	11,10	12,60
A MIN	10,90	10,90	12,40
△D MO–153 Variation	DB–1	DC	DD–1

4040066/F 01/2009

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- △D Falls within JEDEC MO–153, except 30 pin body length.

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