ADS869x 支持可编程双极输入范围的 18 位高速单电源 SAR ADC 数据采集系统

1 特性

- 集成模拟前端的 18 位 ADC
- 高速：
  - ADS8691：1MSPS
  - ADS8695：500kSPS
  - ADS8699：100kSPS
- 可通过软件编程的输入范围：
  - 双极范围：±12.288V、±10.24V、±6.144V、±5.12V 和 ±2.56V
  - 单极范围：0V–12.288V、0V–10.24V、0V–6.144V 以及 0V–5.12V
- 5V 模拟电源：1.65V 到 5V I/O 电源
- 恒定的阻性输入阻抗 ≥ 1MΩ
- 输入过压保护：高达 ±20V
- 低漂移的片上 4.096V 基准电压
- 出色的性能：
  - DNL：±0.6 LSB；INL：±1.75 LSB
  - SNR：92.5dB；THD：–110dB
- ALARM → 每通道的高低阈值
- multiSPI™接口，支持菊花链连接
- 扩展工业温度范围：
  -40°C 至 +125°C

2 应用

- 通道隔离的可编程逻辑控制器 (PLC) 模拟输入模块
- 测试和测量
- 电池组监视

3 说明

ADS8691、ADS8695 和 ADS8699 器件属于集成数据采集系统系列，均基于逐次逼近 (SAR) 模数转换器 (ADC)。此类器件采用高速高精度 SAR ADC、集成模拟前端 (AFE) 输入驱动器电路、高达 ±20V 的过压保护电路以及一个温度漂移极低的 4.096V 片上基准。

此类器件由 5V 模拟单电源供电，但支持 ±12.288V、±6.144V、±10.24V、±5.12V 和 ±2.56V 实际双极输入范围以及 0V 至 12.288V、0V 至 10.24V、0V 至 6.144V 和 0V 至 5.12V 单极输入范围。各输入范围的增益和偏移误差均可在特定数值范围内进行调节，确保直流精度较高。通过针对器件内部寄存器进行编程可选择输入范围。该器件提供恒定阻性输入阻抗 (≥ 1MΩ)，不受所选输入范围的影响。

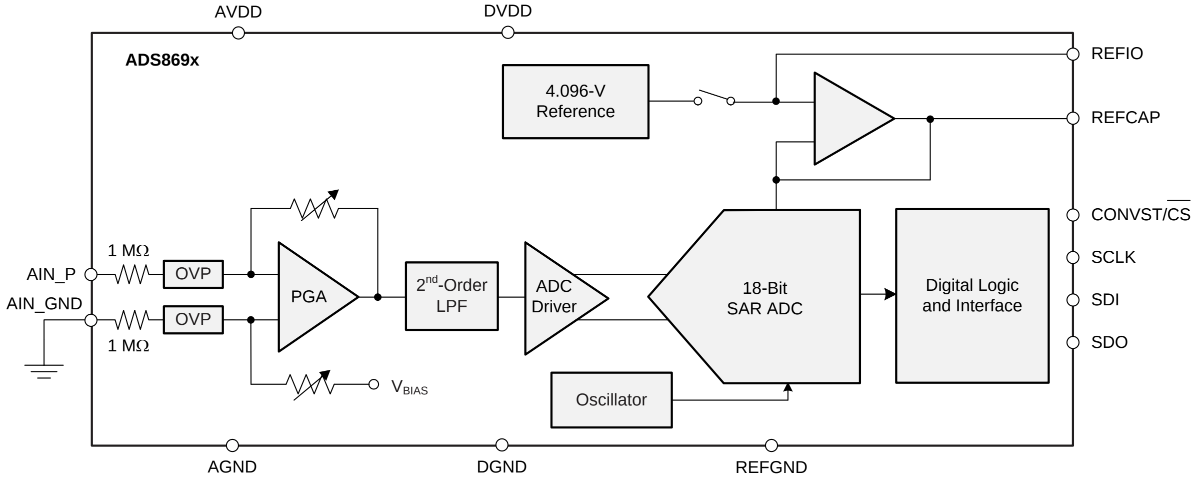
multiSPI 数字接口向后兼容传统 SPI 协议。此外，该器件的可配置 特性 便于连接各种主机控制器。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
ADS869x	TSSOP (16)	5.00mm x 4.40mm
	WQFN (16)	4.00mm x 4.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

方框图



English Data Sheet: SBAS777

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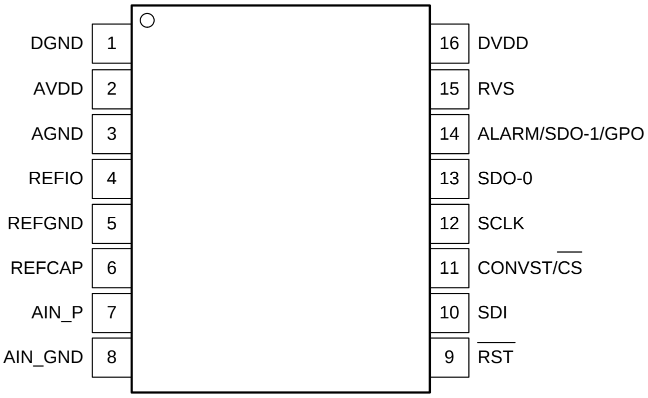
4 修订历史记录

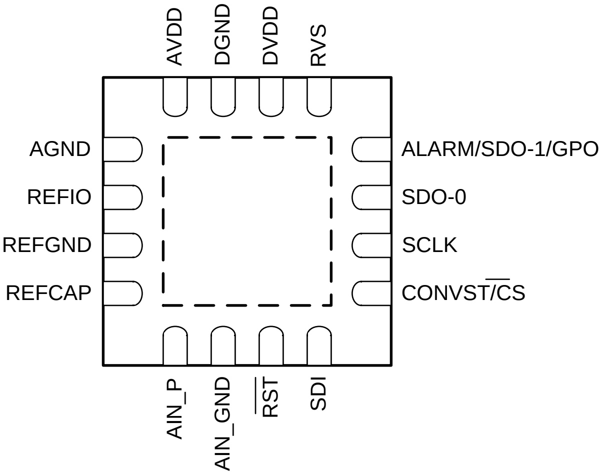
日期	修订版本	注释
2016 年 12 月	*	最初发布。

5 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View (Not to Scale)



RUM Package
16-Pin WQFN
Top View (Not to Scale)



Pin Functions

NAME	NO.		TYPE[1]	DESCRIPTION
	TSSOP	WQFN		
AGND	3	1	P	Analog ground pin. Decouple with the AVDD pin.
AIN_GND	8	6	AI	Analog input: negative. Decouple with the AIN_P pin.
AIN_P	7	5	AI	Analog input: positive. Decouple with the AIN_GND pin.
ALARM/SDO-1/GPO	14	12	DO	Multi-function output pin. Active high alarm. Data output 1 for serial communication. General-purpose output pin.
AVDD	2	16	P	Analog supply pin. Decouple with the AGND pin.
CONVST/CS	11	9	DI	Dual-functionality pin. Active high logic: conversion start input pin; a CONVST rising edge brings the device from acquisition phase to conversion phase. Active low logic: chip-select input pin; the device takes control of the data bus when CS is low; the SDO-x pins go to tri-state when CS is high.
DGND	1	15	P	Digital ground pin. Decouple with the DVDD pin.
DVDD	16	14	P	Digital supply pin. Decouple with the DGND pin.
REFCAP	6	4	AO	ADC reference buffer decoupling capacitor pin. Decouple with the REFGND pin.
REFGND	5	3	P	Reference ground pin; short to the analog ground plane. Decouple with the REFIO and REFCAP pins.
REFIO	4	2	AIO	Internal reference output and external reference input pin. Decouple with REFGND.
RST	9	7	DI	Active low logic input to reset the device.
RVS	15	13	DO	Multi-function output pin for serial interface; see the *RESET State* section. With CS held high, RVS reflects the status of the internal ADCST signal. With CS low, the status of RVS depends on the output protocol selection.
SCLK	12	10	DI	Serial communication: clock input pin for the serial interface. All system-synchronous data transfer protocols are timed with respect to the SCLK signal.
SDI	10	8	DI	Dual function: data input pin for serial communication. Chain data input during serial communication in daisy-chain mode.
SDO-0	13	11	DO	Serial communication: data output 0

(1) AI = analog input, AIO = analog input/output, DI = digital input, DO = digital output, and P = power supply.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
AIN_P, AIN_GND to GND	AVDD = 5 V(2)	–20	20	V
	AVDD = floating(3)	–11	11	
AVDD to GND or DVDD to GND		–0.3	7	V
REFCAP to REFGND or REFIO to REFGND		–0.3	5.7	V
GND to REFGND		–0.3	0.3	V
Digital input pins to GND		–0.3	DVDD + 0.3	V
Digital output pins to GND		–0.3	DVDD + 0.3	V
Temperature	Operating, T_A	–40	125	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) AVDD = 5 V offers a low impedance of < 30 kΩ.

(3) AVDD = floating with an impedance > 30 kΩ.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Analog input pins (AIN_P, AIN_GND)	±4000	V
			All other pins	±2000	
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)		±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog supply voltage	4.75	5	5.25	V
DVDD	Digital supply voltage	1.65	3.3	AVDD	V

6.4 Thermal Information

THERMAL METRIC(1)		ADS8691, ADS8695, ADS8699		UNIT
		PW (TSSOP)	RUM (WQFN)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	95.7	31.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.3	27.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.5	7.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.8	7.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	1.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

all minimum and maximum specifications are at T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 4.096 V (internal), and maximum throughput (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG INPUTS								
V_{IN}	Full-scale input span(1) (AIN_P to AIN_GND)		Input range = ±3 × V_{REF}		–12.288		12.288	V
			Input range = ±2.5 × V_{REF}		–10.24		10.24	
			Input range = ±1.5 × V_{REF}		–6.144		6.144	
			Input range = ±1.25 × V_{REF}		–5.12		5.12	
			Input range = ±0.625 × V_{REF}		–2.56		2.56	
			Input range = 3 × V_{REF}		0		12.288	
			Input range = 2.5 × V_{REF}		0		10.24	
			Input range = 1.5 × V_{REF}		0		6.144	
			Input range = 1.25 × V_{REF}		0		5.12	
AIN_P	Operating input range		Input range = ±3 × V_{REF}		–12.288		12.288	V
			Input range = ±2.5 × V_{REF}		–10.24		10.24	
			Input range = ±1.5 × V_{REF}		–6.144		6.144	
			Input range = ±1.25 × V_{REF}		–5.12		5.12	
			Input range = ±0.625 × V_{REF}		–2.56		2.56	
			Input range = 3 × V_{REF}		0		12.288	
			Input range = 2.5 × V_{REF}		0		10.24	
			Input range = 1.5 × V_{REF}		0		6.144	
			Input range = 1.25 × V_{REF}		0		5.12	
AIN_GND	Operating input range		All input ranges		–0.1	0	0.1	V
R_{IN}	Input impedance		At T_A = 25°C	Input range = ±3 × V_{REF}	1.02	1.2	1.38	MΩ
				Input range = ±1.5 × V_{REF}	1.02	1.2	1.38	
				Input range = 3 × V_{REF}	1.02	1.2	1.38	
				Input range = 1.5 × V_{REF}	1.02	1.2	1.38	
				Input range = ±2.5 × V_{REF}	0.85	1	1.15	
				Input range = ±1.25 × V_{REF}	0.85	1	1.15	
				Input range = ±0.625 × V_{REF}	0.85	1	1.15	
				Input range = 2.5 × V_{REF}	0.85	1	1.15	
				Input range = 1.25 × V_{REF}	0.85	1	1.15	
	Input impedance drift					7	25	ppm/°C
I_{IN}	Input current		With voltage at the AIN_P pin = V_{IN}	Input range = ±3 × V_{REF}		$(V_{IN} – 2.5) / R_{IN}$		µA
				Input range = ±2.5 × V_{REF}		$(V_{IN} – 2.2) / R_{IN}$		
				Input range = ±1.5 × V_{REF}		$(V_{IN} – 2.0) / R_{IN}$		
				Input range = ±1.25 × V_{REF}		$(V_{IN} – 2.0) / R_{IN}$		
				Input range = ±0.625 × V_{REF}		$(V_{IN} – 1.6) / R_{IN}$		
				Input range = 3 × V_{REF}		$(V_{IN} – 2.6) / R_{IN}$		
				Input range = 2.5 × V_{REF}		$(V_{IN} – 2.5) / R_{IN}$		
				Input range = 1.5 × V_{REF}		$(V_{IN} – 2.7) / R_{IN}$		
				Input range = 1.25 × V_{REF}		$(V_{IN} – 2.5) / R_{IN}$		
INPUT OVERVOLTAGE PROTECTION CIRCUIT								
V_{OVP}	All input ranges		AVDD = 5 V or offers low impedance < 30 kΩ, all input ranges		–20		20	V
			AVDD = floating with impedance > 30 kΩ, all input ranges		–11		11	
INPUT BANDWIDTH								
$f_{–3\ dB}$	Small-signal Input bandwidth	–3 dB	All input ranges			15		kHz
$f_{–0.1\ dB}$		–0.1 dB	All input ranges			2.5		

(1) Ideal input span, does not include gain or offset error.

Electrical Characteristics (continued)

all minimum and maximum specifications are at T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 4.096 V (internal), and maximum throughput (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE							
	Resolution			18			Bits
NMC	No missing codes			18			Bits
DNL	Differential nonlinearity(2)	All input ranges		–0.9	±0.6	1.1	LSB
INL	Integral nonlinearity(2)	ADS8691	Input range = ±3 × V_{REF}, ±2.5 × V_{REF}, ±1.5 × V_{REF}, ±1.25 × V_{REF}	–3.25	±1.75	3.25	LSB
			Input range = ±0.625 × V_{REF}	–4.25	±2.25	4.25	
			All unipolar ranges(3)	–3.5	±2	3.5	
		ADS8695, ADS8699	All input ranges	–3	±1.5	3	
E_O	Offset error(4)	At T_A = 25°C	All bipolar ranges(5)	–1	±0.2	1	mV
			All unipolar ranges(3)	–2	±0.2	2	
	Offset error drift with temperature	All input ranges		–3	±0.75	3	ppm/°C
E_G	Gain error(6)	At T_A = 25°C, all input ranges		–0.025	±0.01	0.025	%FSR
	Gain error drift with temperature(7)	All input ranges		–5	±1	5	ppm/°C
DYNAMIC CHARACTERISTICS							
SNR	Signal-to-noise ratio(8)	Input range = ±3 × V_{REF}		91	92.5		dB
		Input range = ±2.5 × V_{REF}		91	92.5		
		Input range = ±1.5 × V_{REF}		90	91.5		
		Input range = ±1.25 × V_{REF}		90	91.5		
		Input range = ±0.625 × V_{REF}		87.75	90		
		Input range = 3 × V_{REF}		89.5	91		
		Input range = 2.5 × V_{REF}		89.5	91		
		Input range = 1.5 × V_{REF}		88	91		
		Input range = 1.25 × V_{REF}		88	90		
THD	Total harmonic distortion(9)(8)	All input ranges			–110		dB
SINAD	Signal-to-noise + distortion(8)	Input range = ±3 × V_{REF}		90.9	92.5		dB
		Input range = ±2.5 × V_{REF}		90.9	92.5		
		Input range = ±1.5 × V_{REF}		89.9	91.5		
		Input range = ±1.25 × V_{REF}		89.9	91.5		
		Input range = ±0.625 × V_{REF}		87.65	90		
		Input range = 3 × V_{REF}		89.25	91		
		Input range = 2.5 × V_{REF}		89.25	91		
		Input range = 1.5 × V_{REF}		87.75	90		
		Input range = 1.25 × V_{REF}		87.75	90		
SFDR	Spurious-free dynamic range(8)	All input ranges			114		dB

(2) This specification indicates the endpoint INL, not best-fit INL.
(3) Unipolar ranges are 0 V–12.288 V, 0 V–10.24 V, 0 V–6.144 V, and 0 V–5.12 V.
(4) Measured relative to actual measured reference.
(5) Bipolar ranges are ±12.288 V, ±10.24 V, ±6.144 V, ±5.12 V, and ±2.56 V.
(6) Excludes internal reference accuracy error.
(7) Excludes internal reference temperature drift.
(8) All specifications expressed in decibels (dB) refer to the full-scale input (FSR) and are tested with a 1-kHz input signal 0.25 dB below full-scale, unless otherwise specified.
(9) Calculated on the first nine harmonics of the input frequency.

Electrical Characteristics (continued)

all minimum and maximum specifications are at T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 4.096 V (internal), and maximum throughput (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SAMPLING DYNAMICS							
t_{CONV}	Conversion time	ADS8691				665	ns
		ADS8695				1000	
		ADS8699				5000	
t_{ACQ}	Acquisition time	ADS8691		335			ns
		ADS8695		1000			
		ADS8699		5000			
f_{cycle}	Maximum throughput rate without latency	ADS8691				1000	kSPS
		ADS8695				500	
		ADS8699				100	
INTERNAL REFERENCE OUTPUT							
V_{REFIO}	On the REFIO pin (configured as an output)	At T_A = 25°C	TSSOP (PW)	4.095	4.096	4.097	V
			WQFN (RUM)	4.094	4.096	4.098	
dV_{REFIO}/dT_A	Internal reference temperature drift	TSSOP (PW)			4	7	ppm/°C
		WQFN (RUM)			5		
C_{OUT_REFIO}	Decoupling capacitor on REFIO pin			4.7			µF
V_{REFCAP}	Reference voltage to the ADC (on the REFCAP pin)	At T_A = 25°C		4.095	4.096	4.097	V
	REFCAP temperature drift				0.5	2	ppm/°C
C_{OUT_REFCAP}	Decoupling capacitor on REFCAP pin			10			µF
	Turn-on time	C_{OUT_REFCAP} = 10 µF, C_{OUT_REFIO} = 10 µF			20		ms
EXTERNAL REFERENCE INPUT							
V_{REFIO_EXT}	External reference voltage on REFIO	REFIO pin configured as an input		4.046	4.096	4.146	V
AVDD COMPARATOR							
V_{TH_HIGH}	High threshold voltage				5.3		V
V_{TH_LOW}	Low threshold voltage				4.7		V
POWER-SUPPLY REQUIREMENTS							
AVDD	Analog power-supply voltage			4.75	5	5.25	V
DVDD	Digital power-supply voltage	Operating range		1.65	3.3	AVDD	
		Supply range for specified performance		2.7	3.3	AVDD	
I_{AVDD_DYN}	Analog supply current, device converting at maximum throughput	Internal reference	ADS8691		8.2	10.5	mA
			ADS8695		5.6	7.25	
			ADS8699		4	5	
		External reference	ADS8691		7.0	8.75	
			ADS8695		4.4	5.5	
			ADS8699		2.7	3.25	
I_{AVDD_STC}	Analog supply current, device not converting	Internal reference	ADS8691		4.7	6.25	mA
			ADS8695, ADS8699		3.5	4.7	
		External reference	ADS8691		3.5	4.5	
			ADS8695, ADS8699		2.3	3	
I_{AVDD_STDBY}	Analog supply current, device in STANDBY mode	Internal reference			2.8		mA
		External reference			1.6		
I_{AVDD_PD}	Analog supply current, device in PD mode	Internal reference			10		µA
		External reference			10		
I_{DVDD_DYN}	Digital supply current, maximum throughput				0.2	0.25	mA
I_{DVDD_STDBY}	Digital supply current, device in STANDBY mode				1		µA
I_{DVDD_PD}	Digital supply current, device in PD mode				1		µA

Electrical Characteristics (continued)

all minimum and maximum specifications are at T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 4.096 V (internal), and maximum throughput (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (CMOS)						
V_{IH}	Digital high input voltage logic level	DVDD > 2.35 V	0.7 × DVDD		DVDD + 0.3	V
		DVDD ≤ 2.35 V	0.8 × DVDD		DVDD + 0.3	
V_{IL}	Digital low input voltage logic level	DVDD > 2.35 V	–0.3		0.3 × DVDD	V
		DVDD ≤ 2.35 V	–0.3		0.2 × DVDD	
	Input leakage current			100		nA
	Input pin capacitance			5		pF
DIGITAL OUTPUTS (CMOS)						
V_{OH}	Digital high output voltage logic level	I_O = 500-µA source	0.8 × DVDD		DVDD	V
V_{OL}	Digital low output voltage logic level	I_O = 500-µA sink	0		0.2 × DVDD	V
	Floating state leakage current	Only for digital output pins		1		µA
	Internal pin capacitance			5		pF
TEMPERATURE RANGE						
T_A	Operating free-air temperature		–40		125	°C

6.6 Timing Requirements: Conversion Cycle

all minimum and maximum specifications are at T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 4.096 V (internal), and maximum throughput (unless otherwise noted)

			MIN	TYP	MAX	UNIT
TIMING REQUIREMENTS						
f_{cycle}	Sampling frequency	ADS8691			1000	kSPS
		ADS8695			500	
		ADS8699			100	
t_{cycle}	ADC cycle time period		$1/f_{cycle}$			
t_{acq}	Acquisition time	ADS8691	335			ns
		ADS8695	1000			
		ADS8699	5000			
TIMING SPECIFICATIONS						
t_{conv}	Conversion time	ADS8691			665	ns
		ADS8695			1000	
		ADS8699			5000	

6.7 Timing Requirements: Asynchronous Reset

all minimum and maximum specifications are at T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 4.096 V (internal), and maximum throughput (unless otherwise noted)

		MIN	TYP	MAX	UNIT
TIMING REQUIREMENTS					
t_{wl_RST}	Pulse duration: $\overline{\text{RST}}$ high	100			ns
TIMING SPECIFICATIONS					
$t_{D\_RST\_POR}$	Delay time for POR reset: $\overline{\text{RST}}$ rising to RVS rising		20		ms
$t_{D\_RST\_APP}$	Delay time for application reset: $\overline{\text{RST}}$ rising to CONVST/$\overline{\text{CS}}$ rising			1	µs
t_{NAP_WKUP}	Wake-up time: NAP mode			20	µs
t_{PWRUP}	Power-up time: PD mode		20		ms

6.8 Timing Requirements: SPI-Compatible Serial Interface

all minimum and maximum specifications are at T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 4.096 V (internal), and maximum throughput (unless otherwise noted)

		MIN	TYP	MAX	UNIT
TIMING REQUIREMENTS					
f_{CLK}	Serial clock frequency			66.67	MHz
t_{CLK}	Serial clock time period	$1/f_{CLK}$			
t_{PH_CK}	SCLK high time	0.45		0.55	t_{CLK}
t_{PL_CK}	SCLK low time	0.45		0.55	t_{CLK}
t_{SU_CSCK}	Setup time: CONVST/$\overline{\text{CS}}$ falling to first SCLK capture edge	7.5			ns
t_{SU_CKDI}	Setup time: SDI data valid to SCLK capture edge	7.5			ns
t_{HT_CKDI}	Hold time: SCLK capture edge to (previous) data valid on SDI	7.5			ns
t_{HT_CKCS}	Delay time: last SCLK capture edge to CONVST/$\overline{\text{CS}}$ rising	7.5			ns
TIMING SPECIFICATIONS					
t_{DEN_CSDO}	Delay time: CONVST/$\overline{\text{CS}}$ falling edge to data enable			9.5	ns
t_{DZ_CSDO}	Delay time: CONVST/$\overline{\text{CS}}$ rising to SDO-x going to 3-state			10	ns
t_{D_CKDO}	Delay time: SCLK launch edge to (next) data valid on SDO-x			12	ns
t_{D_CSRVS}	Delay time: CONVST/$\overline{\text{CS}}$ rising edge to RVS falling			14	ns

6.9 Timing Requirements: Source-Synchronous Serial Interface (External Clock)

all minimum and maximum specifications are at T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 4.096 V (internal), and maximum throughput (unless otherwise noted)

		MIN	TYP	MAX	UNIT
TIMING REQUIREMENTS					
f_{CLK}	Serial clock frequency			66.67	MHz
t_{CLK}	Serial clock time period	$1/f_{CLK}$			
t_{PH_CK}	SCLK high time	0.45		0.55	t_{CLK}
t_{PL_CK}	SCLK low time	0.45		0.55	t_{CLK}
TIMING SPECIFICATIONS					
t_{DEN_CSDO}	Delay time: CONVST/$\overline{CS}$ falling edge to data enable			9.5	ns
t_{DZ_CSDO}	Delay time: CONVST/$\overline{CS}$ rising to SDO-x going to 3-state			10	ns
$t_{D\_CKRVS\_r}$	Delay time: SCLK rising edge to RVS rising			14	ns
$t_{D\_CKRVS\_f}$	Delay time: SCLK falling edge to RVS falling			14	ns
t_{D_RVSDO}	Delay time: RVS rising to (next) data valid on SDO-x			2.5	ns
t_{D_CSRVS}	Delay time: CONVST/$\overline{CS}$ rising edge to RVS displaying internal device state			15	ns

6.10 Timing Requirements: Source-Synchronous Serial Interface (Internal Clock)

all minimum and maximum specifications are at T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; AVDD = 5 V, DVDD = 3.3 V, V_{REF} = 4.096 V (internal), and maximum throughput (unless otherwise noted)

		MIN	TYP	MAX	UNIT
TIMING SPECIFICATIONS					
t_{DEN_CSDO}	Delay time: CONVST/$\overline{CS}$ falling edge to data enable			9.5	ns
t_{DZ_CSDO}	Delay time: CONVST/$\overline{CS}$ rising to SDO-x going to 3-state			10	ns
t_{DEN_CSRVS}	Delay time: CONVST/$\overline{CS}$ falling edge to first rising edge on RVS			50	ns
t_{D_RVSDO}	Delay time: RVS rising to (next) data valid on SDO-x			2.5	ns
t_{INTCLK}	Time period: internal clock	15			ns
t_{CYC_RVS}	Time period: RVS signal	15			ns
t_{WH_RVS}	RVS high time	0.4		0.6	t_{INTCLK}
t_{WL_RVS}	RVS low time	0.4		0.6	t_{INTCLK}
t_{D_CSRVS}	Delay time: CONVST/$\overline{CS}$ rising edge to RVS displaying internal device state			15	ns

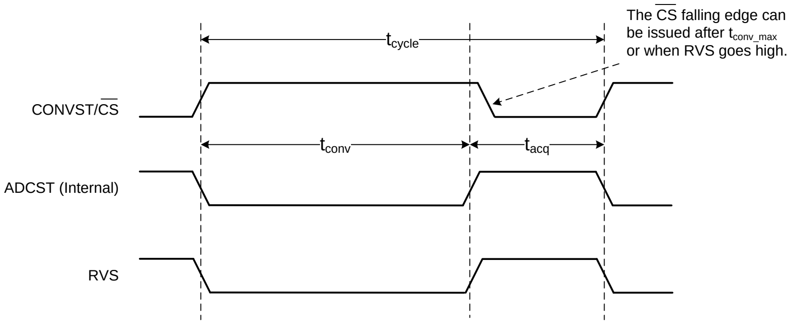


Figure 1. Conversion Cycle Timing Diagram

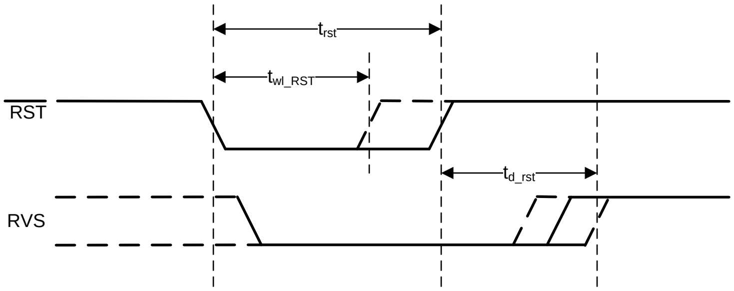


Figure 2. Asynchronous Reset Timing Diagram

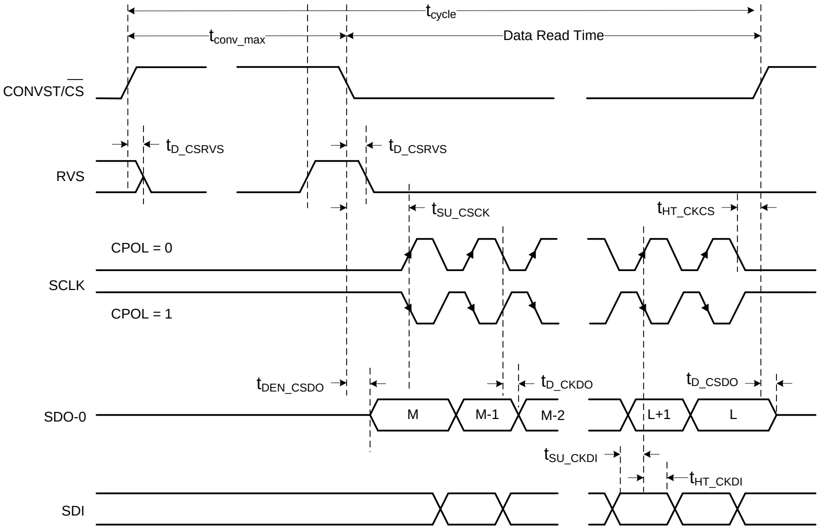


Figure 3. Standard SPI Interface Timing Diagram for CPHA = 0

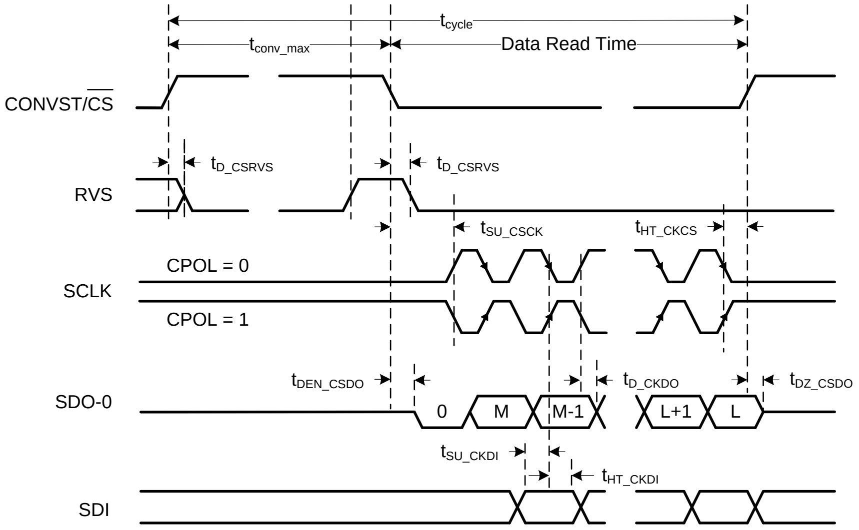


Figure 4. Standard SPI Interface Timing Diagram for CPHA = 1

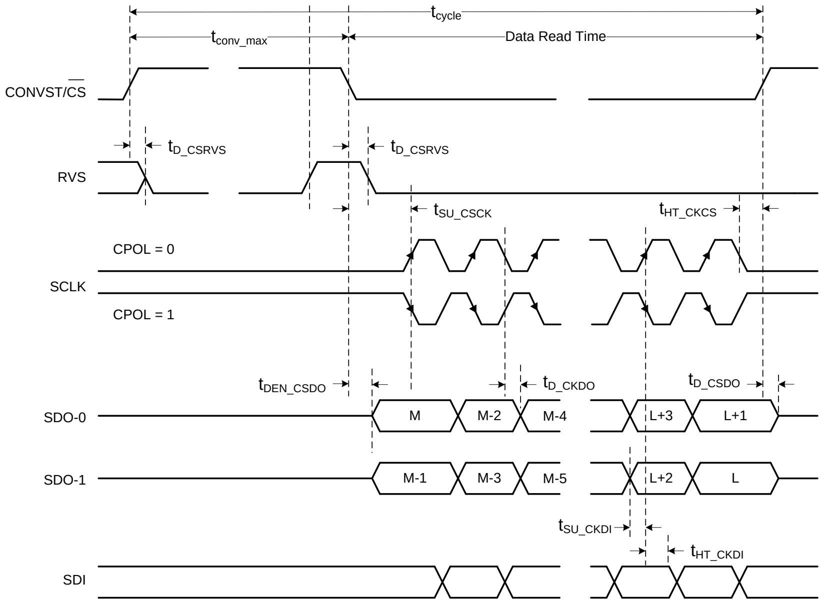


Figure 5. multiSPI Interface Timing Diagram for Dual SDO-x and CPHA = 0

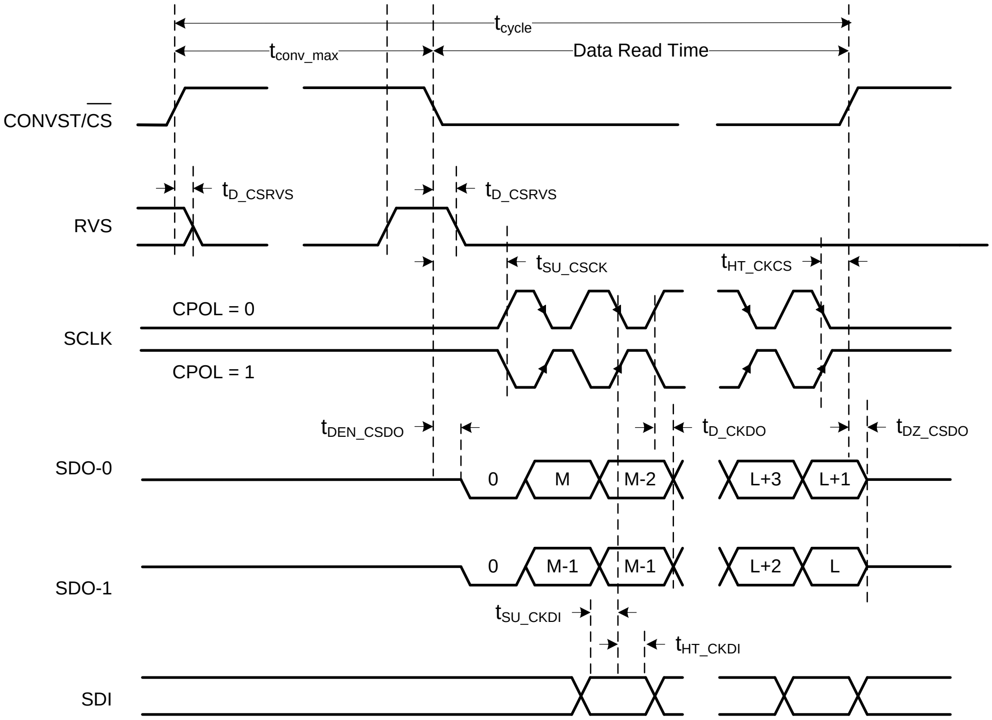


Figure 6. multiSPI Interface Timing Diagram for Dual SDO-x and CPHA = 1

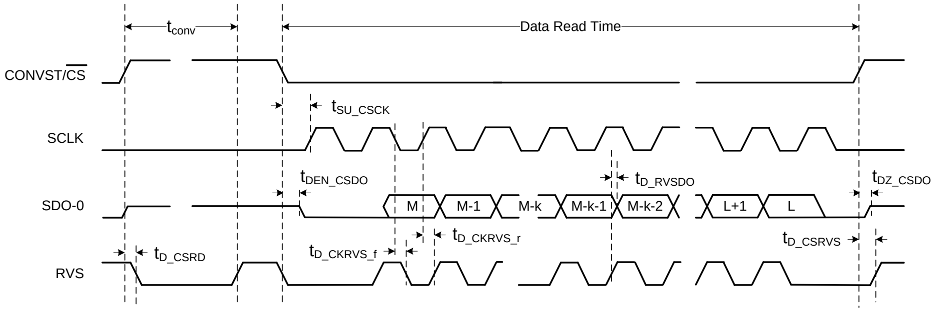


Figure 7. multiSPI Source-Synchronous External Clock Serial Interface Timing Diagram

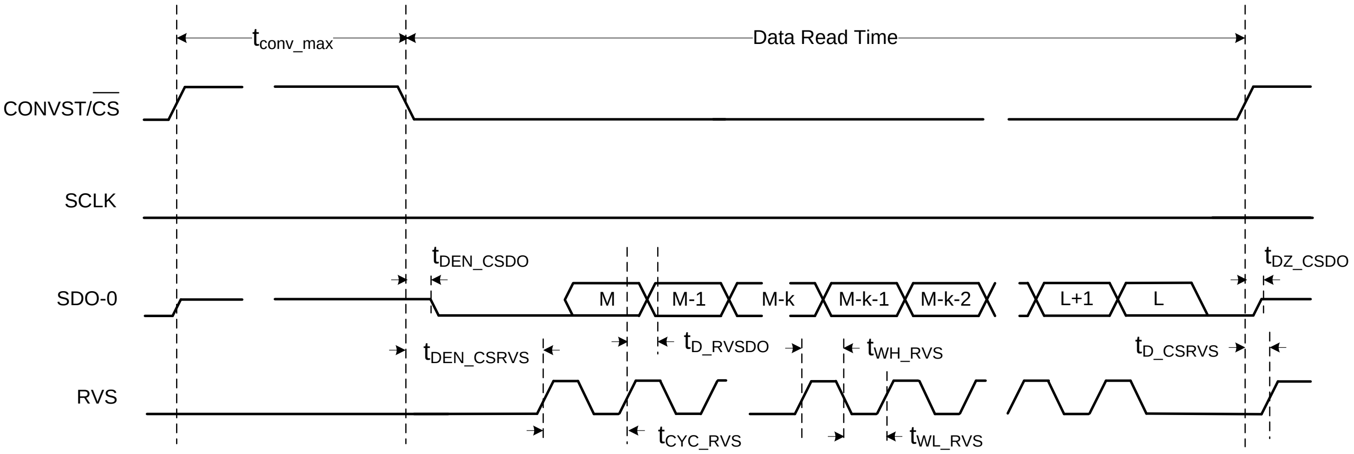


Figure 8. multiSPI Source-Synchronous Internal Clock Serial Interface Timing Diagram

6.11 Typical Characteristics

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, V_{REF} = 4.096 V (internal), and maximum throughput (unless otherwise noted)

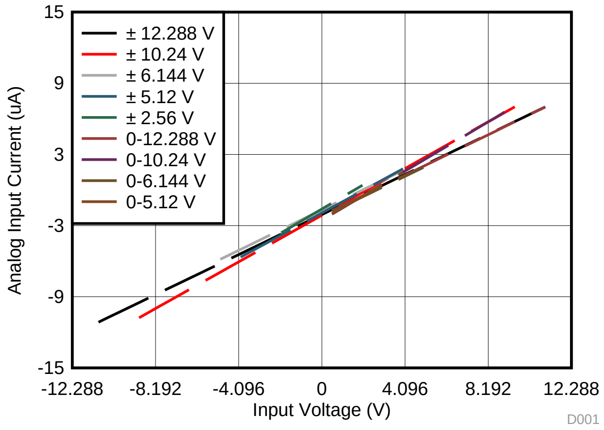
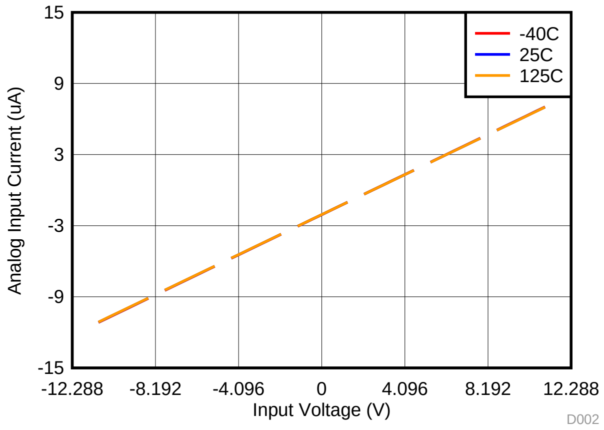


Figure 9. Input I-V Characteristic Across Input Ranges



Range = ±12.288 V

Figure 10. Input I-V Characteristic Across Temperature

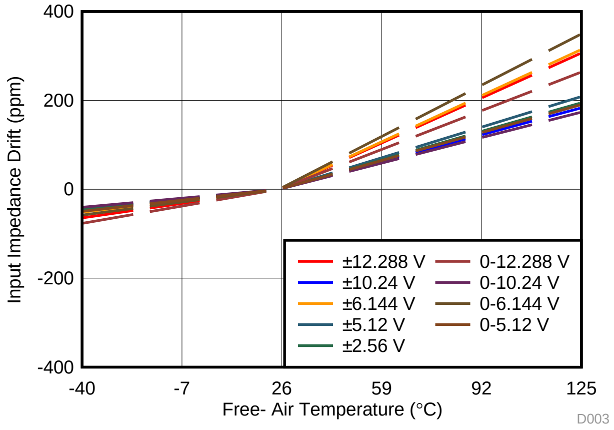
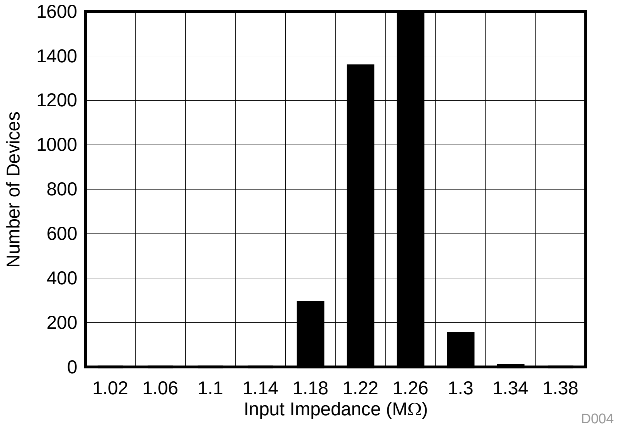
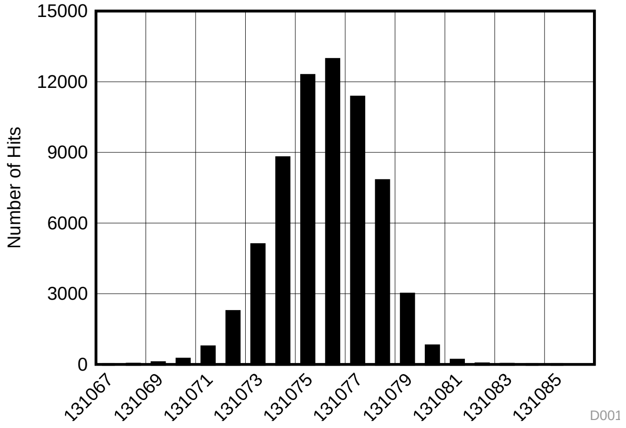


Figure 11. Input Impedance Drift vs Temperature



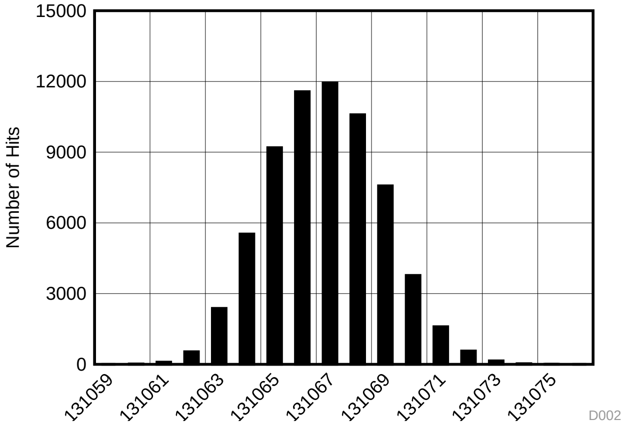
Number of samples = 3398

Figure 12. Typical Distribution of Input Impedance



Mean = 131076.2, sigma = 1.9, input = 0 V

Figure 13. DC Histogram for Mid-Scale Inputs (±12.288 V)

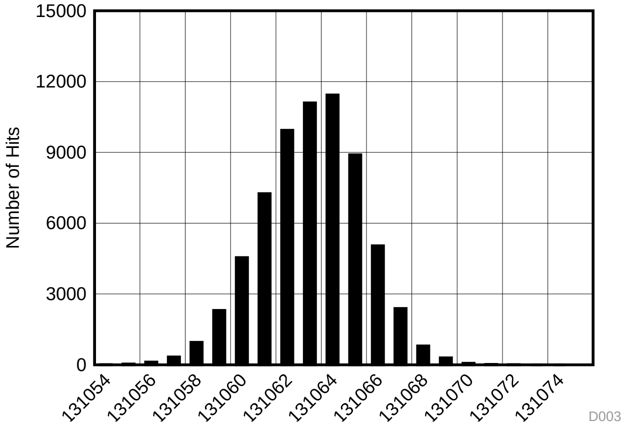


Mean = 131066.8, sigma = 2.04, input = 0 V

Figure 14. DC Histogram for Mid-Scale Inputs (±10.24 V)

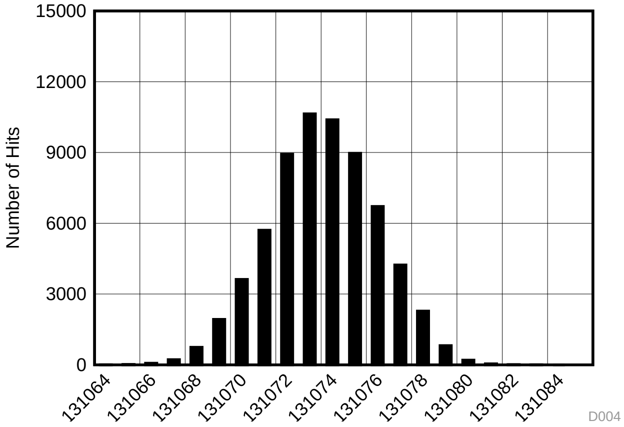
Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, V_{REF} = 4.096 V (internal), and maximum throughput (unless otherwise noted)



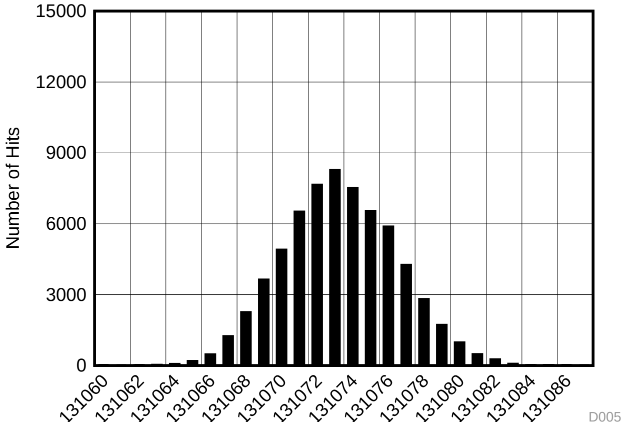
Mean = 131063.9, sigma = 2.23, input = 0 V

Figure 15. DC Histogram for Mid-Scale Inputs (±6.144 V)



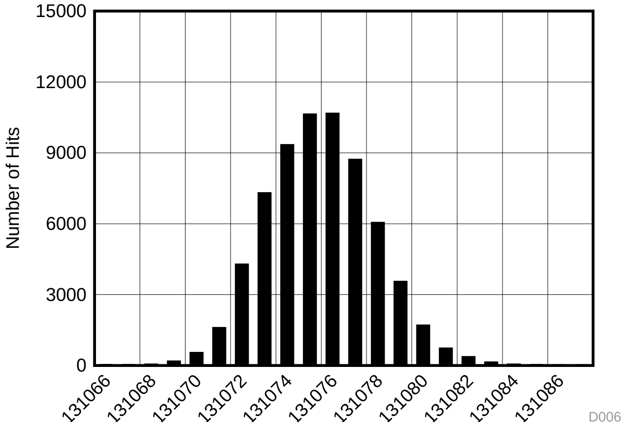
Mean = 131073.5, sigma = 2.23, input = 0 V

Figure 16. DC Histogram for Mid-Scale Inputs (±5.12 V)



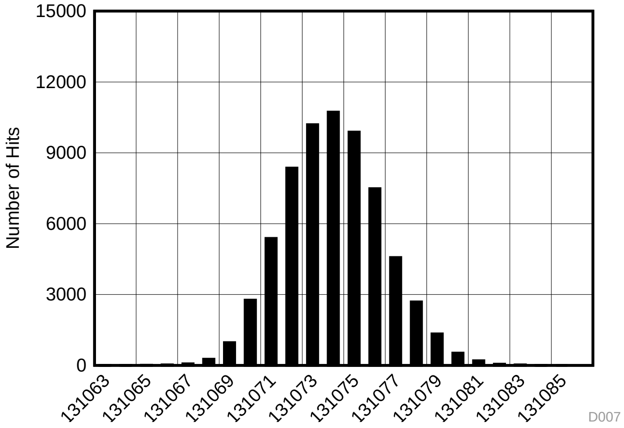
Mean = 131073, sigma = 3.24, input = 0 V

Figure 17. DC Histogram for Mid-Scale Inputs (±2.56 V)



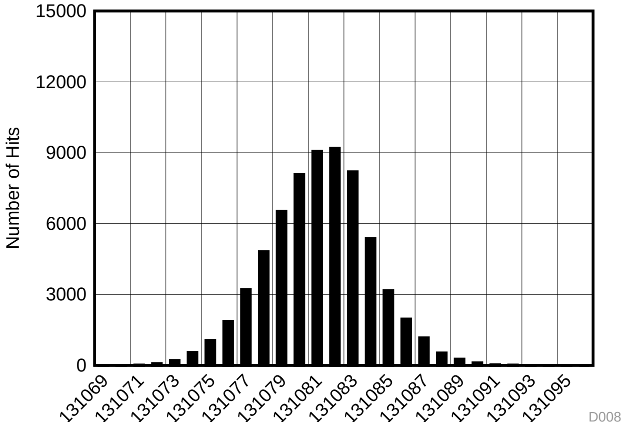
Mean = 131075.5, sigma = 2.41, input = 6.144 V

Figure 18. DC Histogram for Mid-Scale Inputs (0 V–12.288 V)



Mean = 131073.9, sigma = 2.49, input = 5.12 V

Figure 19. DC Histogram for Mid-Scale Inputs (0 V–10.24 V)

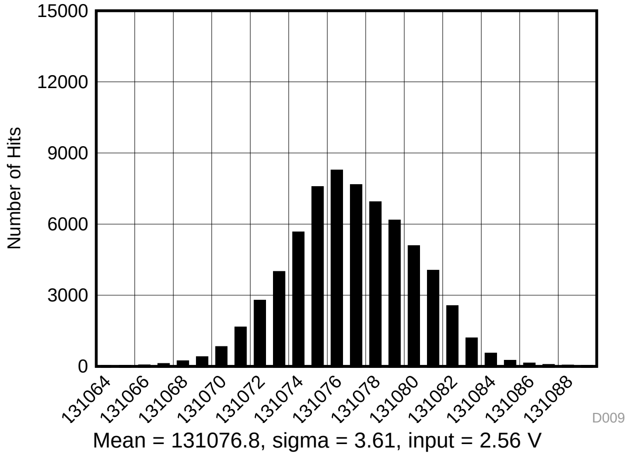


Mean = 131082, sigma = 3.17, input = 3.072 V

Figure 20. DC Histogram for Mid-Scale Inputs (0 V–6.144 V)

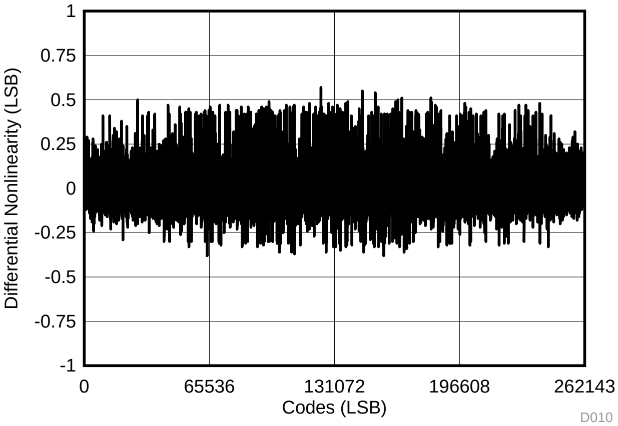
Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, V_{REF} = 4.096 V (internal), and maximum throughput (unless otherwise noted)



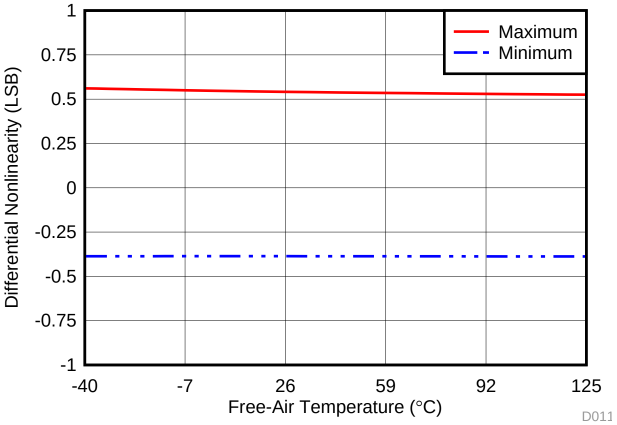
Mean = 131076.8, sigma = 3.61, input = 2.56 V

Figure 21. DC Histogram for Mid-Scale Inputs (0 V–5.12 V)



All input ranges

Figure 22. Typical DNL for All Codes



All input ranges

Figure 23. DNL vs Temperature

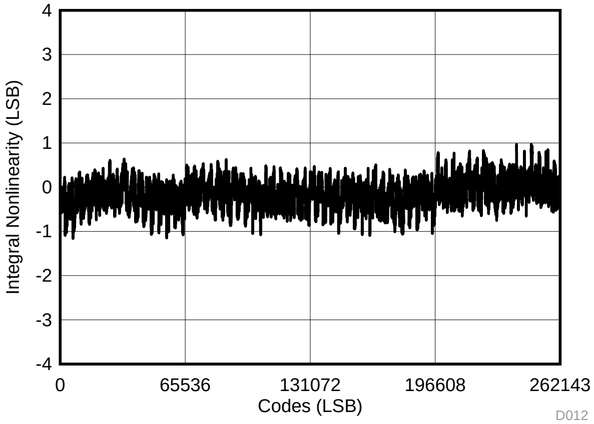


Figure 24. Typical INL for All Codes (All Bipolar Ranges)

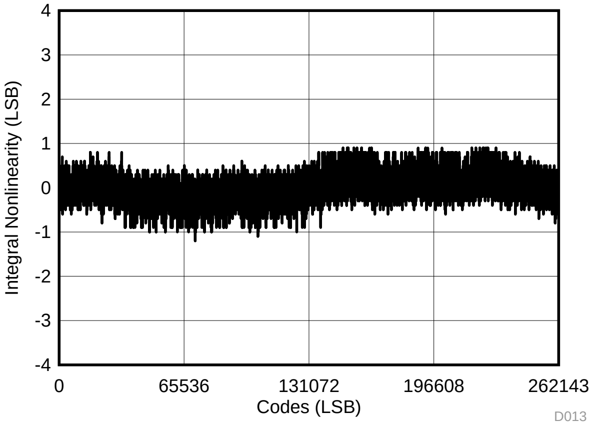


Figure 25. Typical INL for All Codes (All Unipolar Ranges)

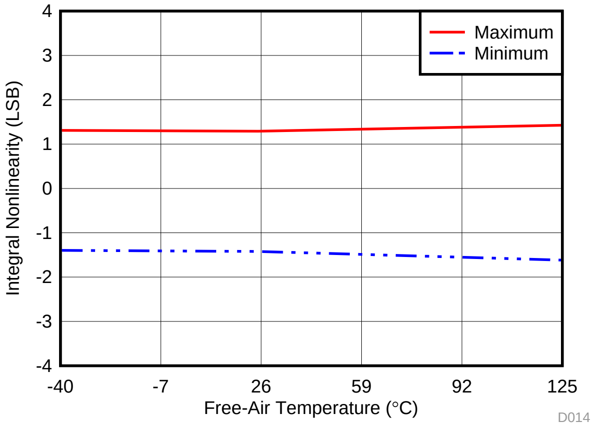


Figure 26. INL vs Temperature (All Bipolar Ranges)

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, V_{REF} = 4.096 V (internal), and maximum throughput (unless otherwise noted)

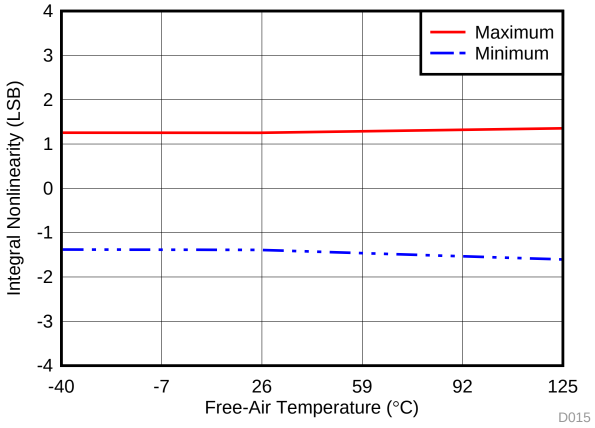


Figure 27. INL vs Temperature (All Unipolar Ranges)

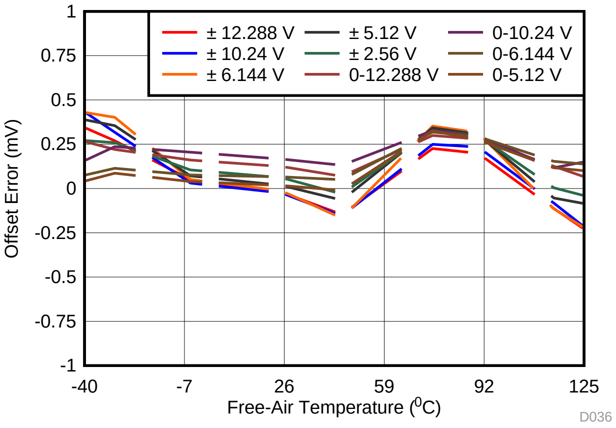


Figure 28. Offset Error vs Temperature Across Input Ranges

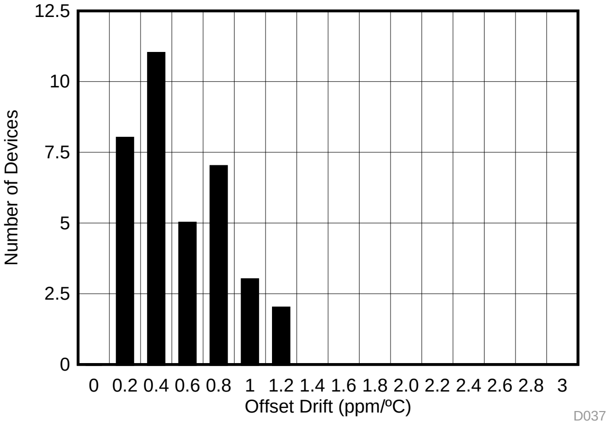


Figure 29. Typical Histogram for Offset Drift

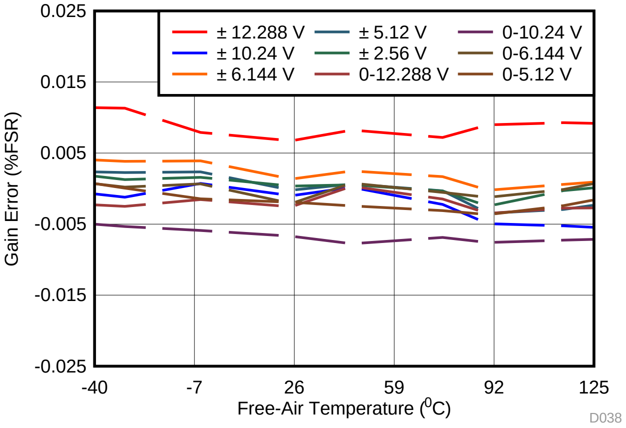


Figure 30. Gain Error vs Temperature Across Input Ranges

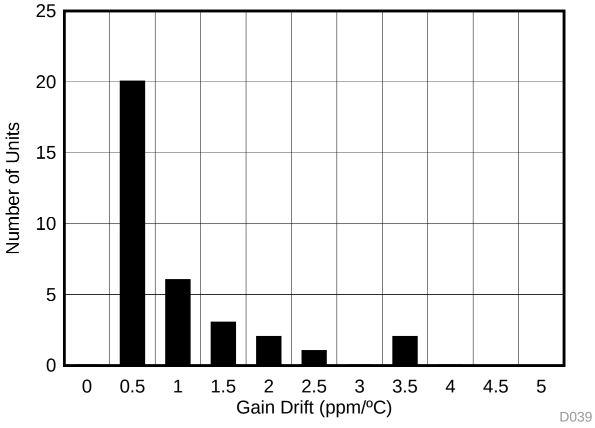


Figure 31. Typical Histogram for Gain Error Drift

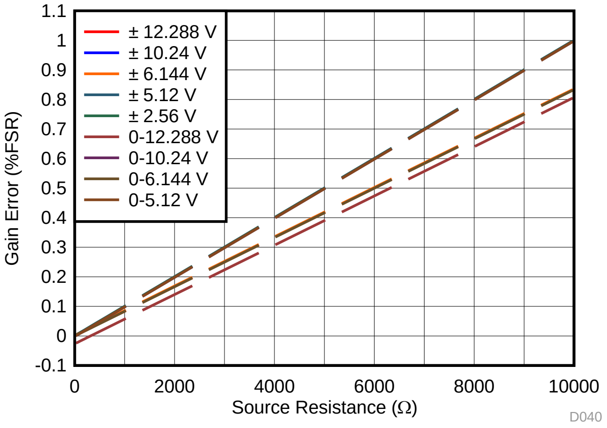
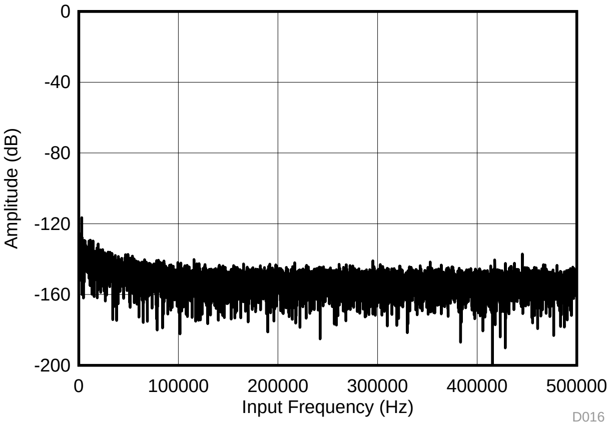


Figure 32. Gain Error vs External Resistance (R_{EXT})

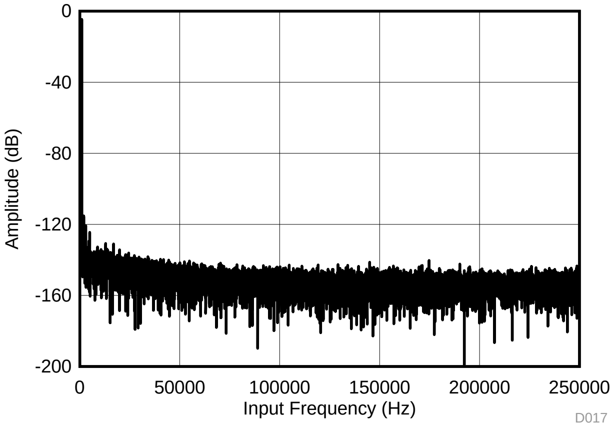
Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, V_{REF} = 4.096 V (internal), and maximum throughput (unless otherwise noted)



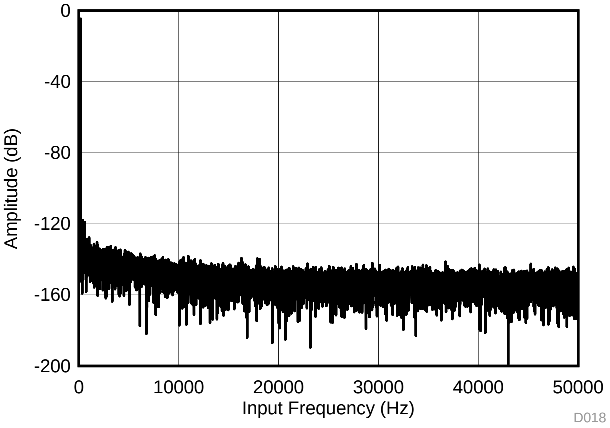
Number of points = 64k, f_{IN} = 1 kHz

Figure 33. Typical FFT Plot (All Ranges) for the ADS8691



Number of points = 64k, f_{IN} = 1 kHz

Figure 34. Typical FFT Plot (All Ranges) for the ADS8695



Number of points = 64k, f_{IN} = 1 kHz

Figure 35. Typical FFT Plot (All Ranges) for the ADS8699

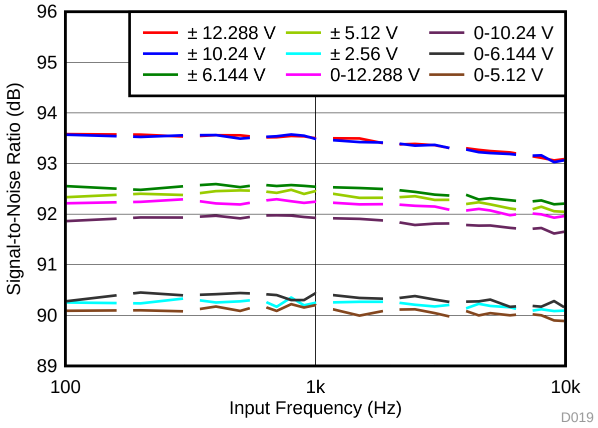
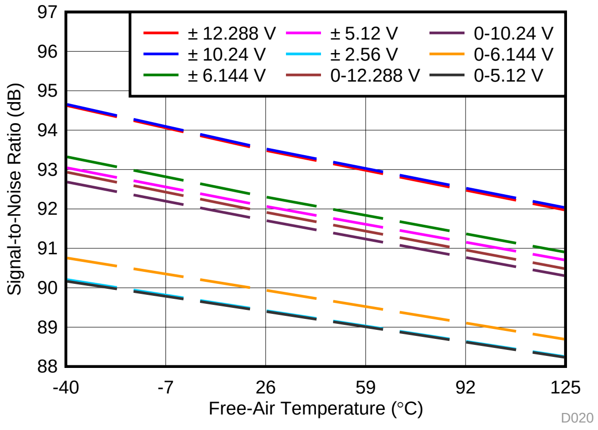


Figure 36. SNR vs Input Frequency



f_{IN} = 1 kHz

Figure 37. SNR vs Temperature

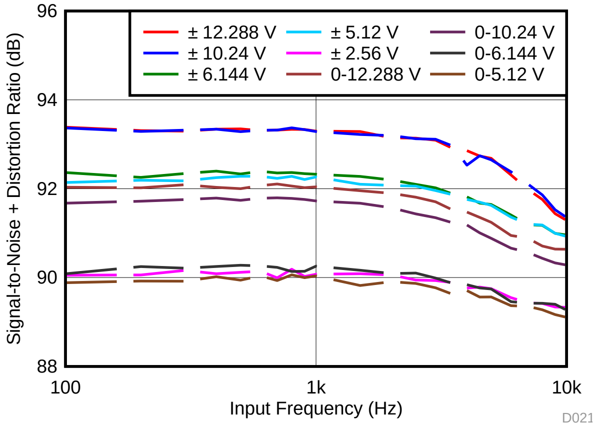


Figure 38. SINAD vs Input Frequency

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, V_{REF} = 4.096 V (internal), and maximum throughput (unless otherwise noted)

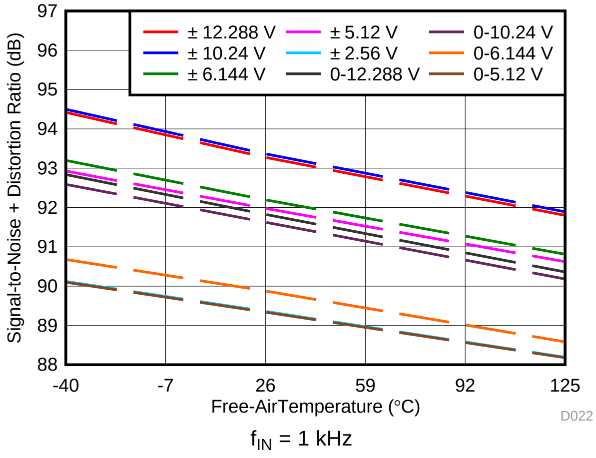


Figure 39. SINAD vs Temperature

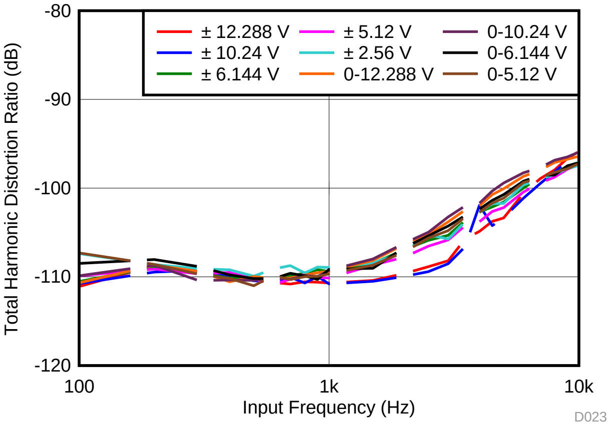


Figure 40. THD vs Input Frequency

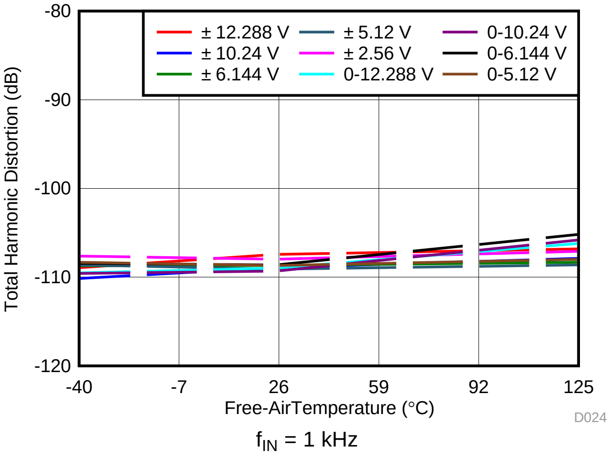


Figure 41. THD vs Temperature

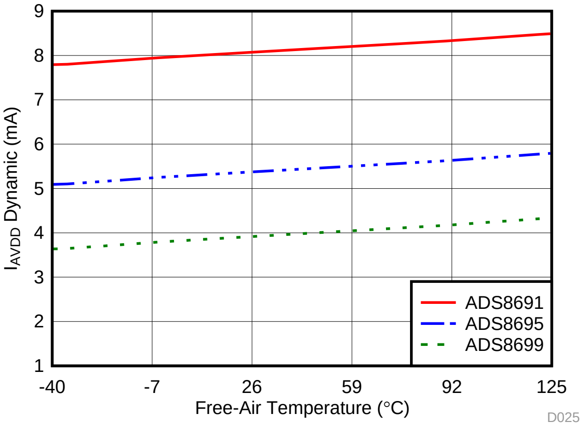


Figure 42. AVDD Current vs Temperature

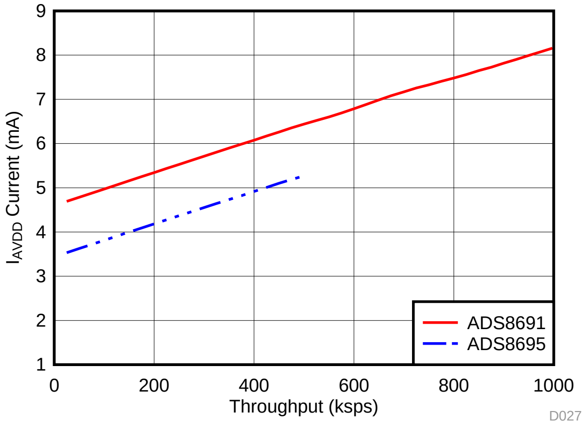


Figure 43. AVDD Current vs Throughput

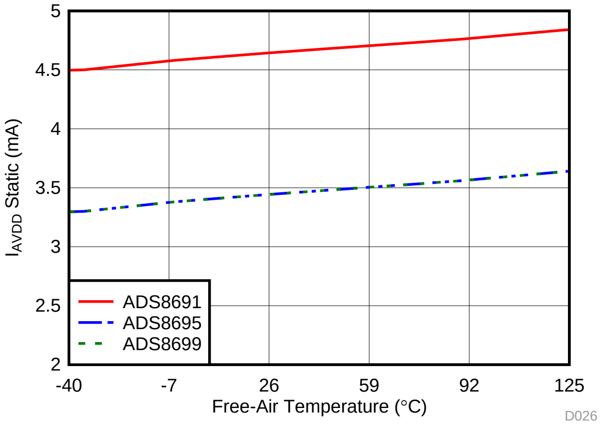


Figure 44. AVDD Current vs Temperature (During Sampling)

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, V_{REF} = 4.096 V (internal), and maximum throughput (unless otherwise noted)

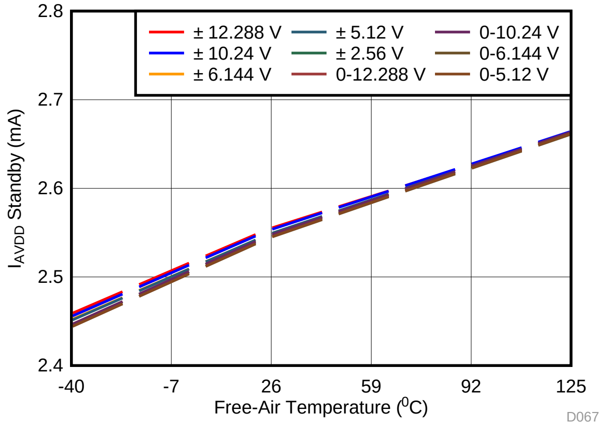


Figure 45. AVDD Current vs Temperature (Standby Mode)

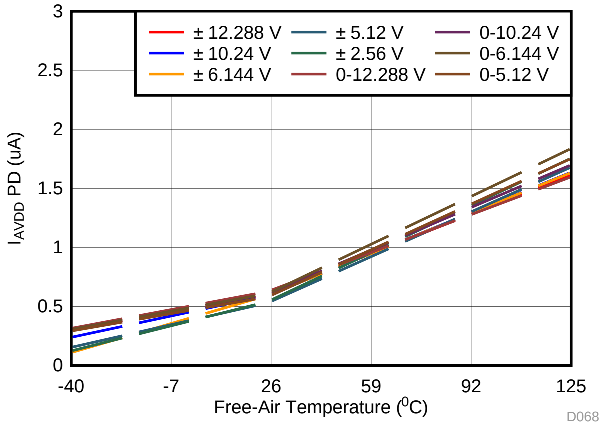


Figure 46. AVDD Current vs Temperature (Power-Down Mode)

7 Detailed Description

7.1 Overview

The ADS869x devices belong to a family of high-speed, high-performance, easy-to-use integrated data acquisition system. This single-channel device supports true bipolar input voltage swings up to ±12.288 V, operating on a single 5-V analog supply. The device features an enhanced SPI interface (multiSPI) that allows the sampling rate to be maximized even with lower speed host controllers.

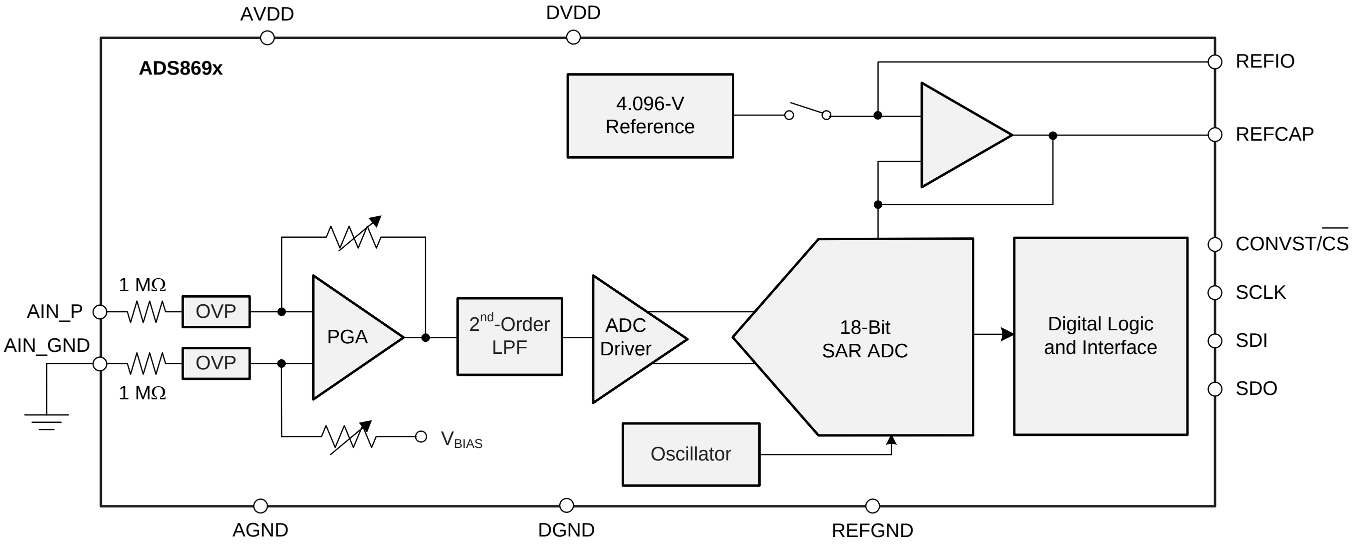
The device consists of a high-precision successive approximation register (SAR) analog-to-digital converter (ADC) and a power-optimized analog front-end (AFE) circuit for signal conditioning that includes:

- A high-resistive input impedance (≥ 1 MΩ) that is independent of the sampling rate
- A programmable gain amplifier (PGA) with a pseudo-differential input configuration supporting nine software-programmable unipolar and bipolar input ranges
- A second-order, low-pass antialiasing filter
- An ADC driver amplifier that ensures quick settling of the SAR ADC input for high accuracy
- An input overvoltage protection circuit up to ±20 V

The device also features a low temperature drift, 4.096-V internal reference with a fast-settling buffer and a multiSPI serial interface with daisy-chain (DAISY) and ALARM features.

The integration of the multichannel precision AFE circuit with high input impedance and a precision ADC operating from a single 5-V supply offers a simplified end solution without requiring external high-voltage bipolar supplies and complicated driver circuits.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Analog Input Structure

The device features a pseudo-differential input structure, meaning that the single-ended analog input signal is applied at the positive input AIN_P and the negative input AIN_GND is tied to GND. Figure 47 shows the simplified circuit schematic for the AFE circuit, including the input overvoltage protection circuit, PGA, low-pass filter (LPF), and high-speed ADC driver.

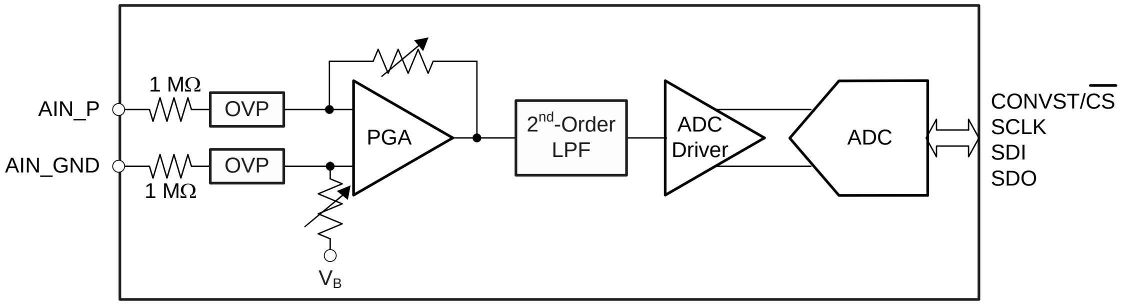


Figure 47. Simplified Analog Front-End Circuit Schematic

The device can support multiple unipolar or bipolar, single-ended input voltage ranges based on the configuration of the program registers. As explained in the RANGE_SEL_REG register, the input voltage range for each analog channel can be configured to bipolar ±3 × V_{REF}, ±2.5 × V_{REF}, ±1.5 × V_{REF}, ±1.25 × V_{REF}, and ±0.625 × V_{REF} or unipolar 0 to 3 × V_{REF}, 0 to 2.5 × V_{REF}, 0 to 1.5 × V_{REF} and 0 to 1.25 × V_{REF}. With the internal or external reference voltage set to 4.096 V, the input ranges of the device can be configured to bipolar ranges of ±12.288 V, ±10.24 V, ±6.144 V, ±5.12 V, and ±2.56 V or unipolar ranges of 0 V to 12.288 V, 0 V to 10.24 V, 0 V to 6.144 V, and 0 V to 5.12 V.

The device samples the voltage difference (AIN_P – AIN_GND) between the analog input and the AIN_GND pin. The device allows a ±0.1-V range on the AIN_GND pin. This feature is useful in modular systems where the sensor or signal-conditioning block is further away from the ADC on the board and when a difference in the ground potential of the sensor or signal conditioner from the ADC ground is possible. In such cases, running separate wires from the AIN_GND pin of the device to the sensor or signal-conditioning ground is recommended. In order to obtain optimum performance, the input currents and impedances along each input path are recommended to be matched. The two single-ended signals to AIN_P and AIN_GND must be routed as symmetrically as possible from the signal source to the ADC input pins.

If the analog input pin (AIN_P) to the device is left floating, the output of the ADC corresponds to an internal biasing voltage. The output from the ADC must be considered as invalid if the device is operated with floating input pins. This condition does not cause any damage to the device, which becomes fully functional when a valid input voltage is applied to the pins.

7.3.2 Analog Input Impedance

The device presents a resistive input impedance ≥ 1 MΩ on each of the analog inputs. The input impedance is independent of the ADC sampling frequency or the input signal frequency. The primary advantage of such high-impedance inputs is the ease of driving the ADC inputs without requiring driving amplifiers with low output impedance. Bipolar, high-voltage power supplies are not required in the system because this ADC does not require any high-voltage, front-end drivers. In most applications, the signal sources or sensor outputs can be directly connected to the ADC input, thus significantly simplifying the design of the signal chain.

In order to maintain the dc accuracy of the system, matching the external source impedance on the AIN_P input pin with an equivalent resistance on the AIN_GND pin is recommended. This matching helps cancel any additional offset error contributed by the external resistance.

Feature Description (continued)

7.3.3 Input Protection Circuit

The device features an internal overvoltage protection (OVP) circuit on each of the analog inputs. Use the internal protection circuit only as a secondary protection scheme. The external protection devices in the end application are highly recommended to be used to protect against surges, electrostatic discharge (ESD), and electrical fast transient (EFT) conditions. A conceptual block diagram of the internal OVP circuit is shown in Figure 48.

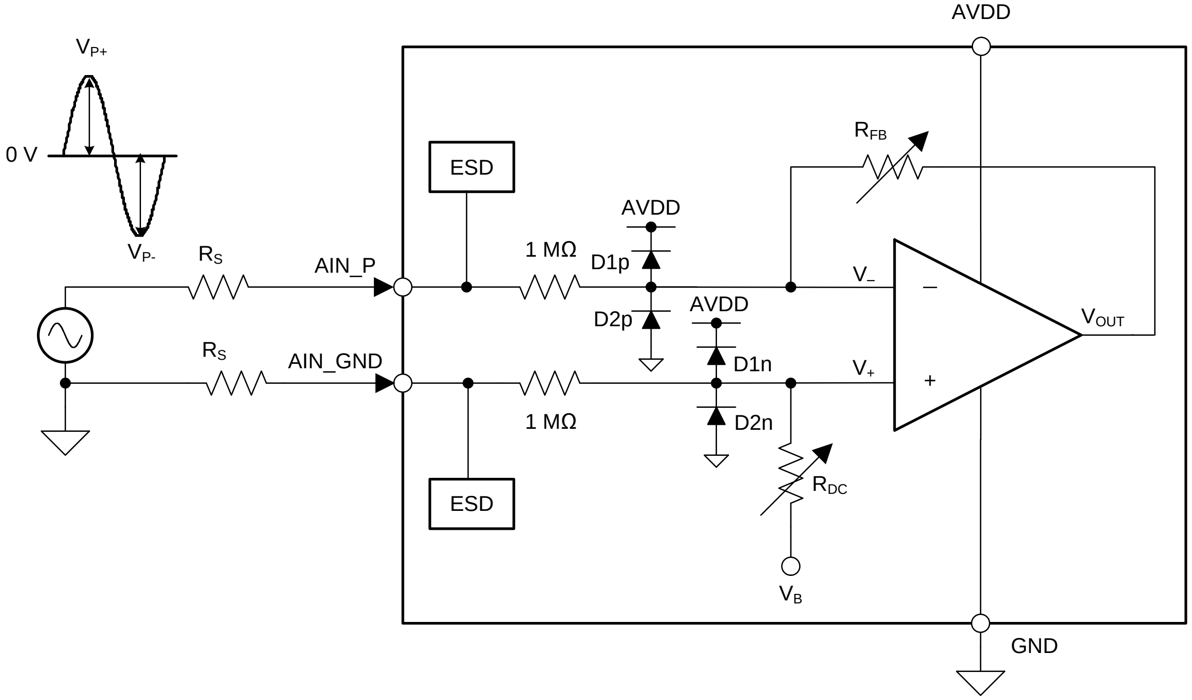


Figure 48. Input Overvoltage Protection Circuit Schematic

As shown in Figure 48, the combination of the 1-MΩ (or, 1.2 MΩ for appropriate input ranges) input resistors along with the PGA gain-setting resistors R_{FB} and R_{DC} limit the current flowing into the input pin. A combination of anti-parallel diodes, D1 and D2 are added to protect the internal circuitry and set the overvoltage protection limits.

Table 1 explains the various operating conditions for the device when powered on. This table indicates that when the device is properly powered up (AVDD = 5 V) or offers a low impedance of < 30 kΩ, the internal overvoltage protection circuit can withstand up to ±20 V on the analog input pins.

Table 1. Input Overvoltage Protection Limits When AVDD = 5 V or Offers a Low Impedance of < 30 kΩ(1)

INPUT CONDITION (V_{OVP} = ±20 V)		TEST CONDITION	ADC OUTPUT	COMMENTS
CONDITION	RANGE			
$\lvert V_{IN} \rvert < \lvert V_{RANGE} \rvert$	Within operating range	All input ranges	Valid	Device functions as per data sheet specifications.
$\lvert V_{RANGE} \rvert < \lvert V_{IN} \rvert < \lvert V_{OVP} \rvert$	Beyond operating range but within overvoltage range	All input ranges	Saturated	ADC output is saturated, but device is internally protected (not recommended for extended time).
$\lvert V_{IN} \rvert > \lvert V_{OVP} \rvert$	Beyond overvoltage range	All input ranges	Saturated	This usage condition can cause irreversible damage to the device.

(1) GND = 0 V, AIN_GND = 0 V, $\lvert V_{RANGE} \rvert$ is the maximum input voltage for any selected input range, and $\lvert V_{OVP} \rvert$ is the break-down voltage for the internal OVP circuit. Assume that R_S is approximately 0 Ω.

The results indicated in Table 1 are based on an assumption that the analog input pin is driven by a very low impedance source (R_S is approximately 0 Ω). However, if the source driving the input has higher impedance, the current flowing through the protection diodes reduces further, thereby increasing the OVP voltage range. Note that higher source impedances result in gain errors and contribute to overall system noise performance.

Figure 49 shows the voltage versus current response of the internal overvoltage protection circuit when the device is powered on. According to this current-to-voltage (I-V) response, the current flowing into the device input pin is limited by the 1-MΩ (or 1.2 MΩ for appropriate input ranges) input impedance. However, for voltages beyond ±20 V, the internal node voltages surpass the break-down voltage for internal transistors, thus setting the limit for overvoltage protection on the input pin.

The same overvoltage protection circuit also provides protection to the device when the device is not powered on and AVDD is floating with an impedance > 30 kΩ. This condition can arise when the input signals are applied before the ADC is fully powered on. The overvoltage protection limits for this condition are shown in Table 2.

Table 2. Input Overvoltage Protection Limits When AVDD = Floating with Impedance > 30 kΩ(1)

INPUT CONDITION (V_{OVP} = ±11 V)		TEST CONDITION	ADC OUTPUT	COMMENTS
CONDITION	RANGE			
$\lvert V_{IN}\rvert < \lvert V_{OVP}\rvert$	Within overvoltage range	All input ranges	Invalid	Device is not functional but is protected internally by the OVP circuit.
$\lvert V_{IN}\rvert > \lvert V_{OVP}\rvert$	Beyond overvoltage range	All input ranges	Invalid	This usage condition can cause irreversible damage to the device.

(1) AVDD = floating, GND = 0 V, AIN_GND = 0 V, $\lvert V_{RANGE}\rvert$ is the maximum input voltage for any selected input range, and $\lvert V_{OVP}\rvert$ is the break-down voltage for the internal OVP circuit. Assume that R_S is approximately 0 Ω.

Figure 50 shows the I-V response of the internal overvoltage protection circuit when the device is not powered on. According to this I-V response, the current flowing into the device input pin is limited by the 1-MΩ input impedance. However, for voltages beyond ±11 V, the internal node voltage surpasses the break-down voltage for internal transistors, thus setting the limit for overvoltage protection on the input pin.

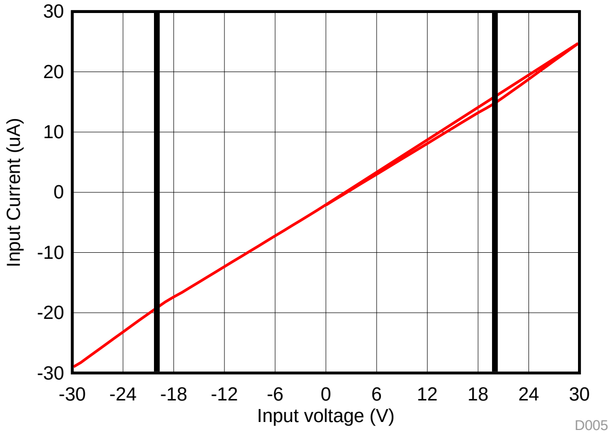


Figure 49. I-V Curve for the Input OVP Circuit (AVDD = 5 V)

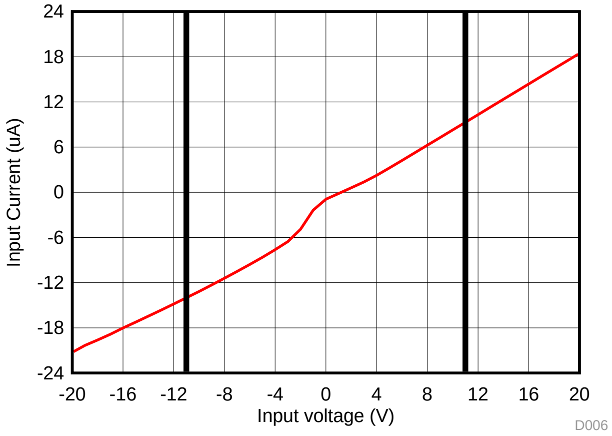


Figure 50. I-V Curve for the Input OVP Circuit (AVDD = Floating)

7.3.4 Programmable Gain Amplifier (PGA)

The device features a programmable gain amplifier (PGA) as part of the analog signal-conditioning circuit that converts the original single-ended input signal into a fully-differential signal to drive the internal SAR ADC. The PGA also adjusts the common-mode level of the input signal before feeding it into the SAR ADC to ensure maximum usage of the ADC input dynamic range. Depending on the range of the input signal, the PGA gain can be adjusted by setting the RANGE_SEL[3:0] bits in the configuration register (see the RANGE_SEL_REG register). The default or power-on state for the RANGE_SEL[3:0] bits is 0000, corresponding to an input signal range of ±3 × V_{REF}. Table 3 lists the various configurations of the RANGE_SEL[3:0] bits for the different analog input voltage ranges.

The PGA uses a precisely-matched network of resistors for multiple gain configurations. Matching between these resistors is accurately trimmed to keep the overall gain error low across all input ranges.

Table 3. Input Range Selection Bits Configuration

ANALOG INPUT RANGE	RANGE_SEL[3:0]			
	BIT 3	BIT 2	BIT 1	BIT 0
±3 × V_{REF}	0	0	0	0
±2.5 × V_{REF}	0	0	0	1
±1.5 × V_{REF}	0	0	1	0
±1.25 × V_{REF}	0	0	1	1
±0.625 × V_{REF}	0	1	0	0
0–3 × V_{REF}	1	0	0	0
0–2.5 × V_{REF}	1	0	0	1
0–1.5 × V_{REF}	1	0	1	0
0–1.25 × V_{REF}	1	0	1	1

7.3.5 Second-Order, Low-Pass Filter (LPF)

In order to mitigate the noise of the front-end amplifier and gain resistors of the PGA, the AFE circuit of the device features a second-order, antialiasing LPF at the output of the PGA. The magnitude and phase response of the analog antialiasing filter are shown in Figure 51 and Figure 52, respectively. For maximum performance, the –3-dB cutoff frequency for the antialiasing filter is typically set to 15 kHz. The performance of the filter is consistent across all input ranges supported by the ADC.

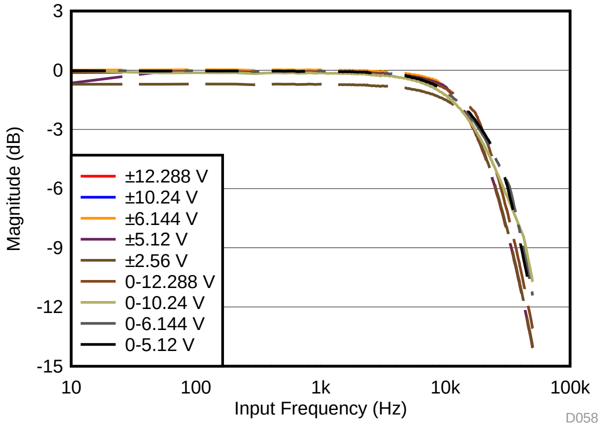


Figure 51. Second-Order LPF Magnitude Response

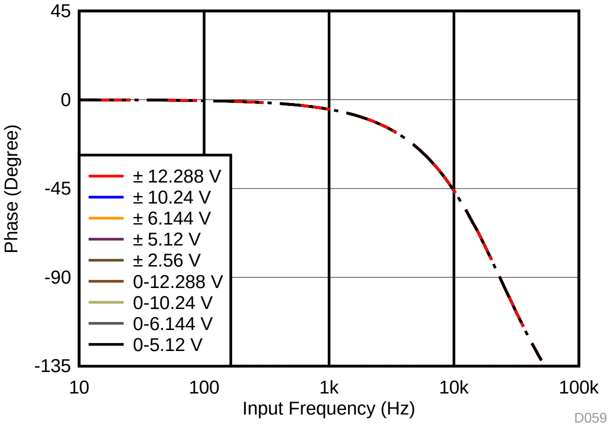


Figure 52. Second-Order LPF Phase Response

7.3.6 ADC Driver

In order to meet the performance of the device at the maximum sampling rate, the sample-and-hold capacitors at the input of the ADC must be successfully charged and discharged during the acquisition time window. This drive requirement at the input of the ADC necessitates the use of a high-bandwidth, low-noise, and stable amplifier buffer. Such an input driver is integrated in the front-end signal path of the analog input channel of the device.

7.3.7 Reference

The device can operate with either an internal voltage reference or an external voltage reference using the internal buffer. The internal or external reference selection is determined by programming the INTREF_DIS bit of the RANGE_SEL_REG register. The internal reference source is enabled (INTREF_DIS = 0) by default after reset or when the device powers up. The INTREF_DIS bit must be programmed to logic 1 to disable the internal reference source whenever an external reference source is used.

7.3.7.1 Internal Reference

The device features an internal reference source with a nominal output value of 4.096 V. In order to select the internal reference, the INTREF_DIS bit of the RANGE_SEL_REG register must be programmed to logic 0. When the internal reference is used, the REFIO pin becomes an output with the internal reference value. A 4.7-µF (minimum) decoupling capacitor is recommended to be placed between the REFIO pin and REFGND, as shown in Figure 53. The capacitor must be placed as close to the REFIO pin as possible. The output impedance of the internal band-gap circuit creates a low-pass filter with this capacitor to band-limit the noise of the reference. The use of a smaller capacitor value allows higher reference noise in the system that can potentially degrade SNR and SINAD performance. The REFIO pin must not be used to drive external ac or dc loads because of limited current output capability. The REFIO pin can be used as a source if followed by a suitable op amp buffer (such as the OPA320).

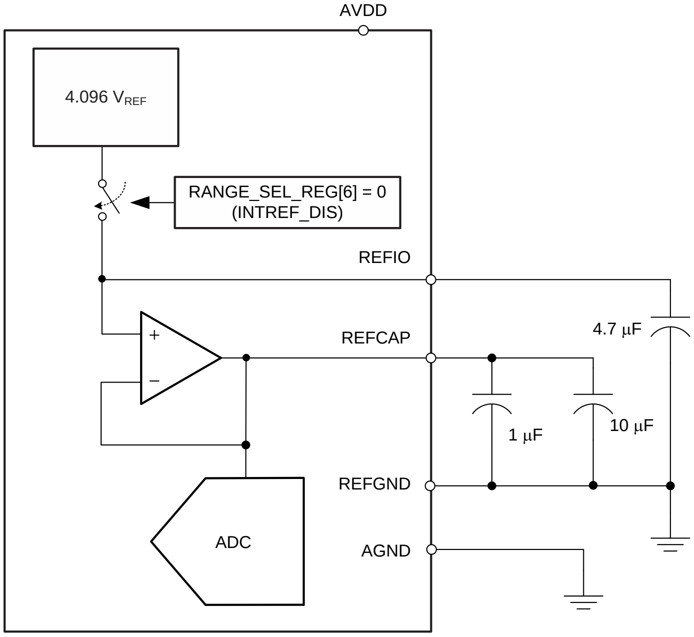


Figure 53. Device Connections for Using an Internal 4.096-V Reference

The device internal reference is factory-trimmed to ensure the initial accuracy specification. The histogram in Figure 54 shows the distribution of the internal voltage reference output taken from more than 3420 production devices.

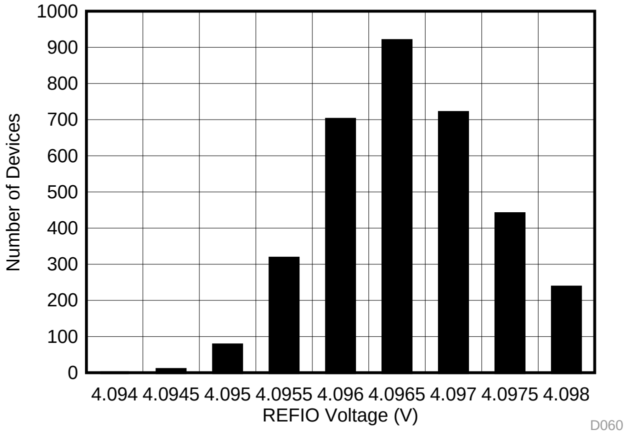


Figure 54. Internal Reference Accuracy Histogram at Room Temperature

The initial accuracy specification for the internal reference can be degraded if the die is exposed to any mechanical or thermal stress. Heating the device when being soldered to a printed circuit board (PCB) and any subsequent solder reflow is a primary cause for shifts in the V_{REF} value. The main cause of thermal hysteresis is a change in die stress and is therefore a function of the package, die-attach material, and molding compound, as well as the layout of the device itself.

In order to illustrate this effect, 30 devices were soldered using lead-free solder paste with the manufacturer suggested reflow profile, as explained in application report *AN-2029 Handling & Process Recommendations* (SNOA550). The internal voltage reference output is measured before and after the reflow process and the typical shift in value is shown in Figure 55. Although all tested units exhibit a positive shift in their output voltages, negative shifts are also possible. Note that the histogram in Figure 55 shows the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, which is common on PCBs with surface-mount components on both sides, causes additional shifts in the output voltage. If the PCB is to be exposed to multiple reflows, solder the ADS869x in the second pass to minimize device exposure to thermal stress.

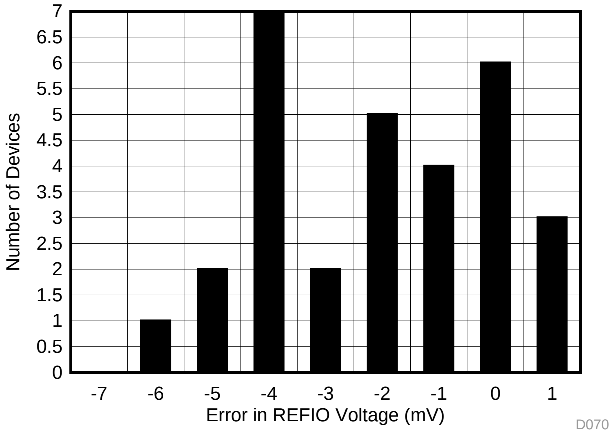


Figure 55. Solder Heat Shift Distribution Histogram

The internal reference is also temperature compensated to provide excellent temperature drift over an extended industrial temperature range of –40°C to +125°C. Figure 56 and Figure 57 show the variation of the internal reference voltage across temperature for different values of the AVDD supply voltage. Note that the temperature drift of the internal reference is also a function of the package type. Figure 58 and Figure 59 show histogram distribution of the reference voltage drift for the TSSOP (PW) and WQFN (RUM) packages, respectively.

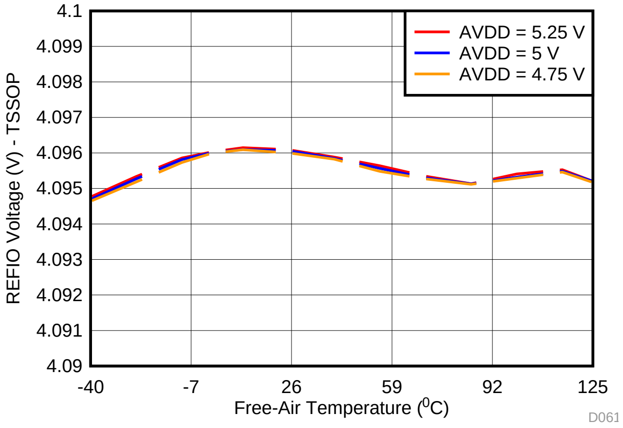


Figure 56. REFIO Voltage Variation Across AVDD and Temperature (PW Package)

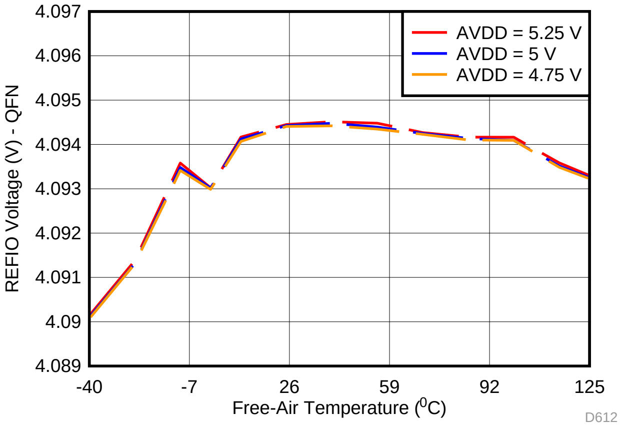
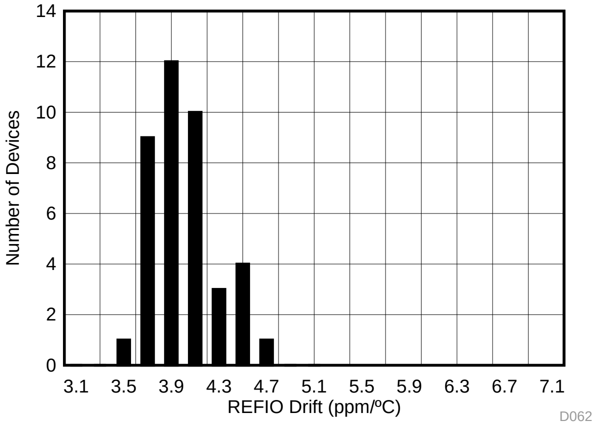
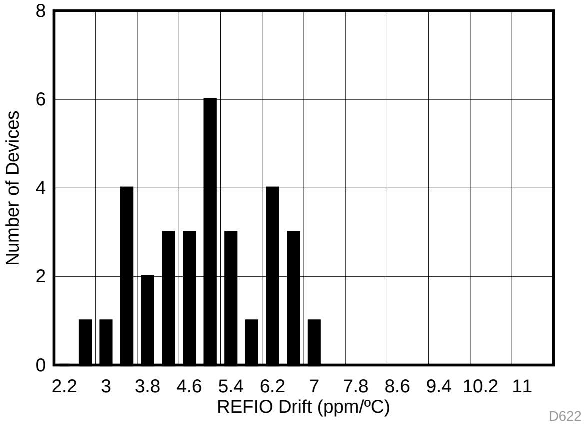


Figure 57. REFIO Voltage Variation Across AVDD and Temperature (RUM Package)



AVDD = 5 V, number of devices = 30, ΔT = –40°C to +125°C

Figure 58. Internal Reference Temperature Drift Histogram (PW Package)



AVDD = 5 V, number of devices = 30, ΔT = –40°C to +125°C

Figure 59. Internal Reference Temperature Drift Histogram (RUM Package)

7.3.7.2 External Reference

For applications that require a better reference voltage or a common reference voltage for multiple devices, the device provides a provision to use an external reference source along with an internal buffer to drive the ADC reference pin. In order to select the external reference mode, the INTREF_DIS bit of the RANGE_SEL_REG register must be programmed to logic 1. In this mode, an external 4.096-V reference must be applied at the REFIO pin, which functions as an input. Any low-power, low-drift, or small-size external reference can be used in this mode because the internal buffer is optimally designed to handle the dynamic loading on the REFCAP pin that is internally connected to the ADC reference input. The output of the external reference must be appropriately filtered to minimize the resulting effect of the reference noise on system performance. A typical connection diagram for this mode is shown in Figure 60.

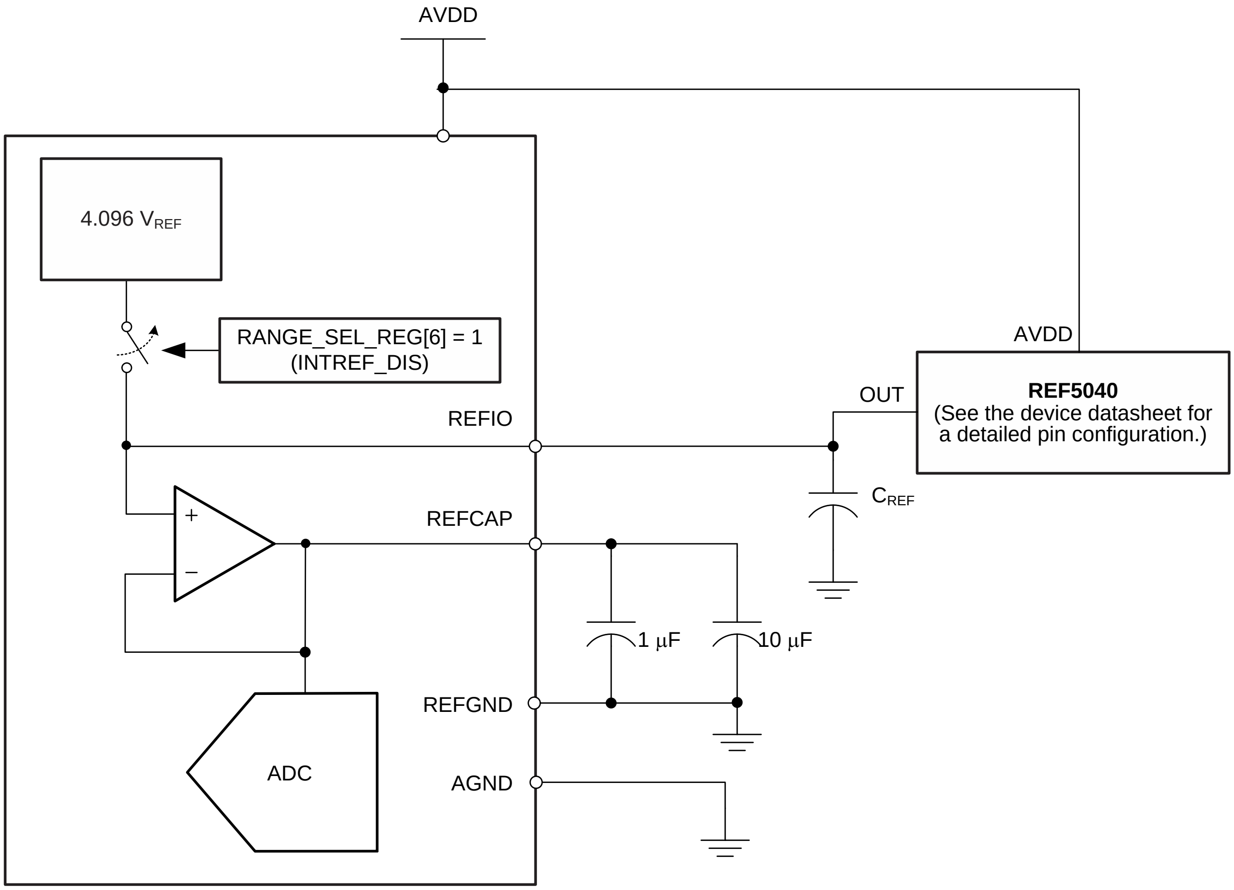


Figure 60. Device Connections for Using an External 4.096-V Reference

The output of the internal reference buffer appears at the REFCAP pin. A minimum capacitance of 10 µF must be placed between the REFCAP and REFGND pins. Place another capacitor of 1 µF as close to the REFCAP pin as possible for decoupling high-frequency signals. Do not use the internal buffer to drive external ac or dc loads because of the limited current output capability of this buffer.

The performance of the internal buffer output is very stable across the entire operating temperature range of –40°C to +125°C. Figure 61 (for the PW package) and Figure 63 (for the RUM package) show the variation in the REFCAP output across temperature for different values of the AVDD supply voltage. The typical specified value of the reference buffer drift over temperature is 0.5 ppm/°C, as shown in Figure 62 (for the PW package) and Figure 64 (for the RUM package), and the maximum specified temperature drift is equal to 2 ppm/°C.

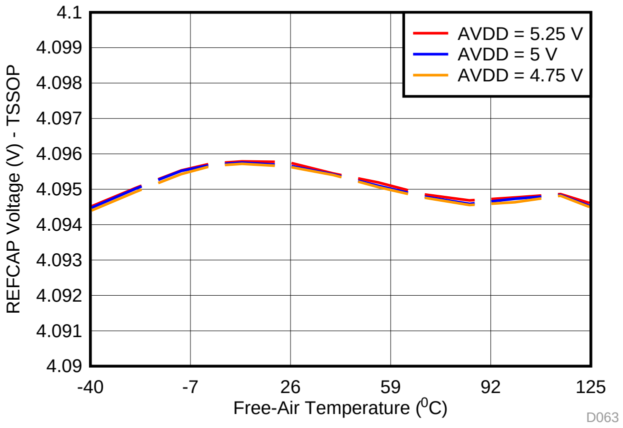
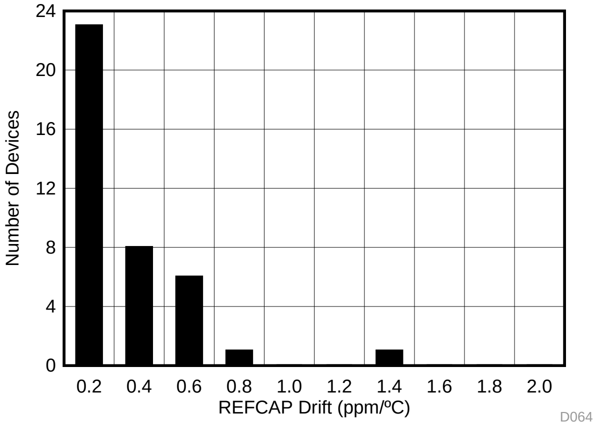


Figure 61. Reference Buffer Output (REFCAP) Variation vs Supply and Temperature (PW Package)



AVDD = 5 V, number of devices = 30, ΔT = –40°C to +125°C

Figure 62. Reference Buffer Temperature Drift Histogram (PW Package)

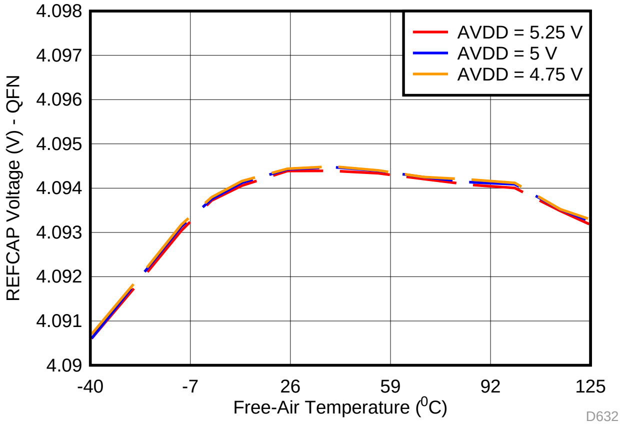
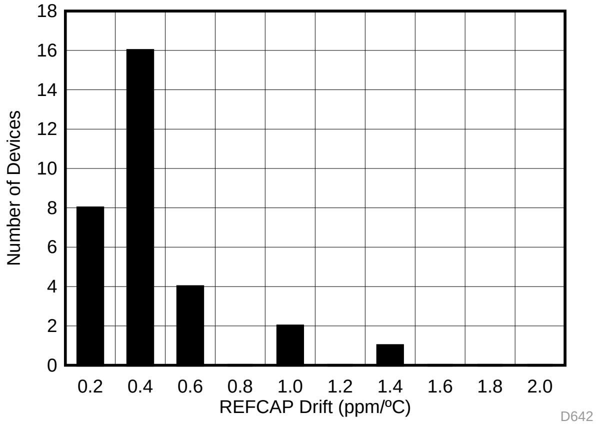


Figure 63. Reference Buffer Output (REFCAP) Variation vs Supply and Temperature (RUM Package)



WQFN (RUM) package, AVDD = 5 V, number of devices = 30, ΔT = –40°C to +125°C

Figure 64. Reference Buffer Temperature Drift Histogram (RUM Package)

7.3.8 ADC Transfer Function

The device supports a pseudo-differential input supporting both bipolar and unipolar input ranges. The output of the device is in straight-binary format for both bipolar and unipolar input ranges.

The ideal transfer characteristic for all input ranges is shown in Figure 65. The full-scale range (FSR) for each input signal is equal to the difference between the positive full-scale (PFS) input voltage and the negative full-scale (NFS) input voltage. The LSB size is equal to FSR / 2^{18}. For a reference voltage of V_{REF} = 4.096 V, the LSB values corresponding to the different input ranges are listed in Table 4.

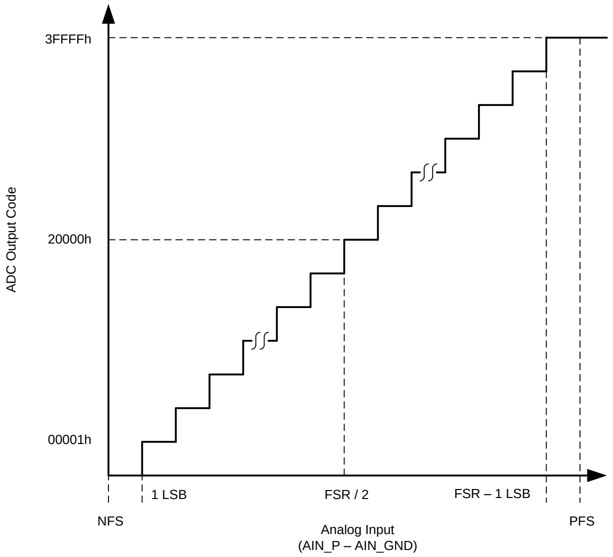


Figure 65. Device Transfer Function (Straight-Binary Format)

Table 4. ADC LSB Values for Different Input Ranges (V_{REF} = 4.096 V)

INPUT RANGE	POSITIVE FULL-SCALE (V)	NEGATIVE FULL-SCALE (V)	FULL-SCALE RANGE (V)	LSB
±3 × V_{REF}	12.288	–12.288	24.576	93.75 µV
±2.5 × V_{REF}	10.24	–10.24	20.48	78.125 µV
±1.5 × V_{REF}	6.144	–6.144	12.288	46.875 µV
±1.25 × V_{REF}	5.12	–5.12	10.24	39.06 µV
±0.625 × V_{REF}	2.56	–2.56	5.12	19.53 µV
0 to 3 × V_{REF}	12.288	0	12.288	46.875 µV
0 to 2.5 × V_{REF}	10.24	0	10.24	39.06 µV
0 to 1.5 × V_{REF}	6.144	0	6.144	23.43 µV
0 to 1.25 × V_{REF}	5.12	0	5.12	19.53 µV

7.3.9 Alarm Features

The device features an active-high alarm output on the ALARM/SDO-1/GPO pin, provided that the pin is configured for alarm functionality. To enable the ALARM output on the multi-function pin, se the SDO1_CONFIG[1:0] bits of the SDO_CTL_REG register to 01b (see the SDO_CTL_REG register).

The device features two types of alarm functions: an input alarm and an AVDD alarm.

- For the input alarm, the voltage at the input of the ADC is monitored and compared against user-programmable high and low threshold values. The device sets an active high alarm output when the corresponding digital value of the input signal goes beyond the high or low threshold set by the user; see the *Input Alarm* section for a detailed explanation of the input alarm feature functionality.
- For the AVDD alarm, the analog supply voltage (AVDD) of the ADC is monitored and compared against the specified typical low threshold (4.7 V) and high threshold (5.3 V) values of the AVDD supply. The device sets an active high alarm output if the value of AVDD crosses the specified low (4.7 V) and high threshold (5.3 V) values in either direction.

When the alarm functionality is turned on, both the input and AVDD alarm functions are enabled by default. These alarm functions can be selectively disabled by programming the IN_AL_DIS and VDD_AL_DIS bits (respectively) of the RST_PWRCTL_REG register.

Each alarm (input alarm or AVDD alarm) has two types of alarm flags associated with it: the *active* alarm flag and the *tripped* alarm flag. All the alarm flags can be read in the ALARM_REG register. Both flags are set when the associated alarm is triggered. However while the active alarm is cleared at the end of the current ADC conversion (and set again if the alarm condition persists), the tripped flag is cleared only after ALARM_REG is read.

The ALARM output flags are updated internally at the end of every conversion. These output flags can be read during any data frame that the user initiates by bringing the CONVST/$\overline{\text{CS}}$ signal to a low level.

The ALARM output flags can be read in three different ways: either via the ALARM output pin, by reading the internal ALARM registers, or by appending the ALARM flags to the data output.

- A high level on the ALARM pin indicates an over- or undervoltage condition on AVDD or on the analog input channel of the device. This pin can be wired to interrupt the host input.
- The internal ALARM flag bits in the ALARM_REG register are updated at the end of conversion. After receiving an ALARM interrupt on the output pin, the internal alarm flag registers can be read to obtain more details on the conditions that generated the alarm.
- The alarm output flags can be selectively appended to the data output bit stream (see the DATAOUT_CTL_REG register for configuration details).

Figure 66 shows a functional block diagram for the device alarm functionality.

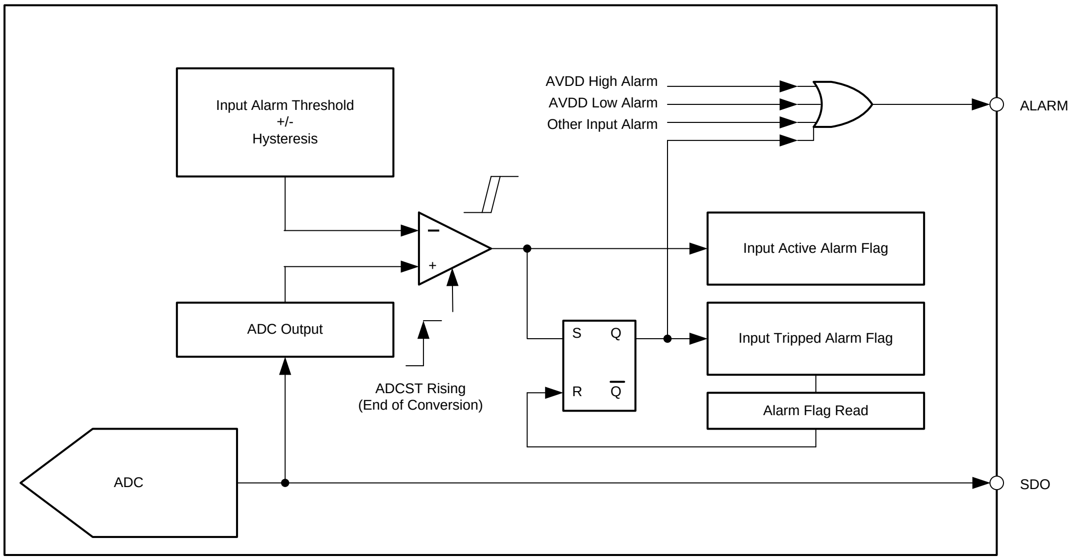


Figure 66. Alarm Functionality Schematic

7.3.9.1 Input Alarm

The device features a high and a low alarm on the analog input. The alarms corresponding to the input signal have independently-programmable thresholds and a common hysteresis setting that can be controlled through the ALARM_H_TH_REG and ALARM_L_TH_REG registers.

The device sets the input high alarm when the digital output exceeds the high alarm upper limit [high alarm threshold (T)]. The alarm resets when the digital output is less than or equal to the high alarm lower limit [high alarm (T) – H – 1). This function is shown in Figure 67.

Similarly, the input low alarm is triggered when the digital output falls below the low alarm lower limit [low alarm threshold (T)]. The alarm resets when the digital output is greater than or equal to the low alarm higher limit [low alarm (T) + H + 1]. This function is shown in Figure 68.

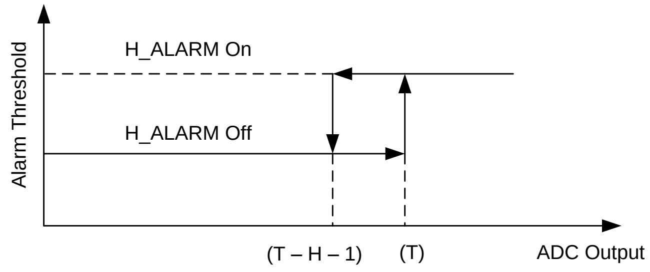


Figure 67. High ALARM Hysteresis

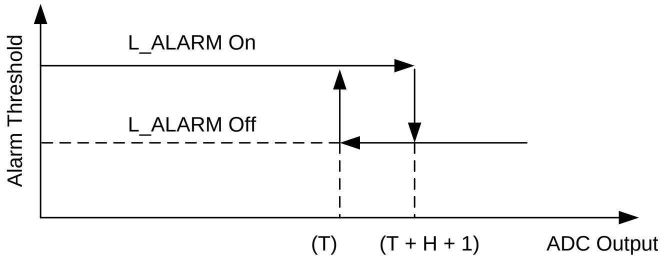


Figure 68. Low ALARM Hysteresis

7.3.9.2 AVDD Alarm

The device features a high and a low alarm on the analog voltage supply, AVDD. Unlike the input signal alarm, the AVDD alarm has fixed trip points that are set by design. The device features an internal analog comparator that constantly monitors the analog supply against the high and low threshold voltages. The high alarm is set if AVDD exceeds a typical value of 5.3 V and the low alarm is asserted if AVDD drops below 4.7 V. This feature is specially useful for debugging unusual device behavior caused by a glitch or brown-out condition on the analog AVDD supply.

7.4 Device Functional Modes

The device features the multiSPI digital interface for communication and data transfer between the device and the host controller. The multiSPI interface supports many data transfer protocols that the host uses to exchange data and commands with the device. The host can transfer data into the device using one of the standard SPI modes. However, the device can be configured to output data in a number of ways to suit the application demands of throughput and latency. The data output in these modes can be controlled either by the host or the device, and the timing can either be system synchronous or source synchronous. For detailed explanation of the supported data transfer protocols, see the *Data Transfer Protocols* section.

This section describes the main components of the digital interface module as well as supported configurations and protocols. As shown in Figure 69, the interface module is comprised of shift registers (both input and output), configuration registers, and a protocol unit. During any particular data frame, data are transferred both into and out of the device. As a result, the host always perceives the device as a 32-bit input-output shift register, as shown in Figure 69.

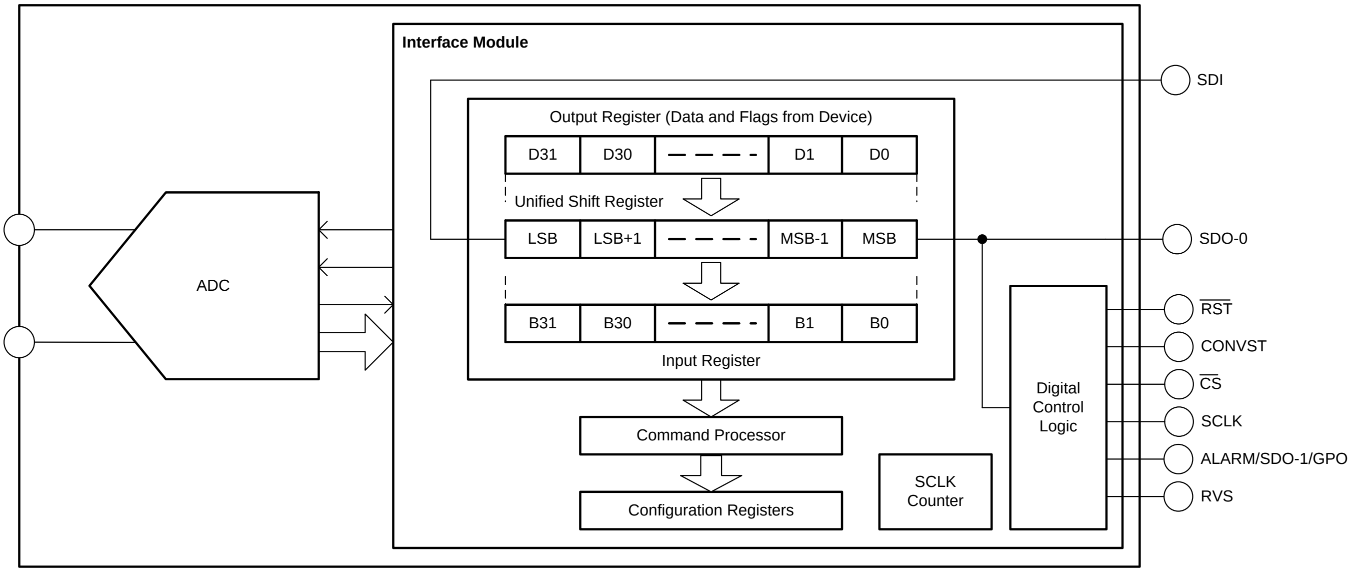


Figure 69. Device Interface Module

The *Pin Configuration and Functions* section provides descriptions of the interface pins; the *Data Transfer Frame* section details the functions of shift registers, the SCLK counter, and the command processor; the *Data Transfer Protocols* section details supported protocols; and the *Register Maps* section explains the configuration registers and bit settings.

Device Functional Modes (continued)

7.4.1 Host-to-Device Connection Topologies

The multiSPI interface and device configuration registers offer great flexibility in the ways a host controller can exchange data or commands with the device. This section describes how to select the hardware connection topology to meet different system requirements.

7.4.1.1 Single Device: All multiSPI Options

Figure 70 shows the pin connection between a host controller and a stand-alone device to exercise all options provided by the multiSPI interface.

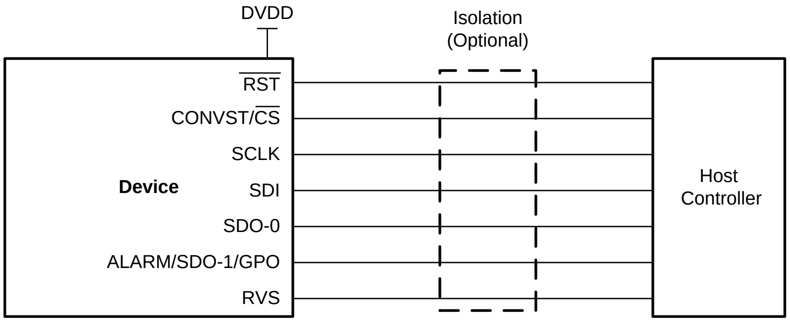


Figure 70. All multiSPI Protocols Pin Configuration

7.4.1.2 Single Device: Standard SPI Interface

Figure 71 shows the minimum pin interface for applications using a standard SPI protocol.

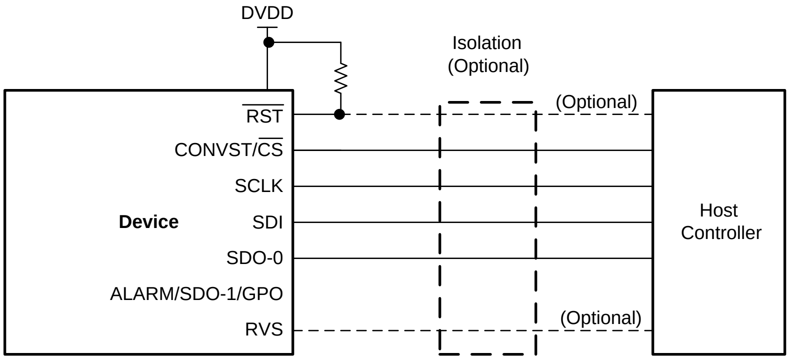


Figure 71. Standard SPI Protocol Pin Configuration

The CONVST/$\overline{\text{CS}}$, SCLK, SDI, and SDO-0 pins constitute a standard SPI port of the host controller. The $\overline{\text{RST}}$ pin can be tied to DVDD. The RVS pin can be monitored for timing benefits. The ALARM/SDO-1/GPO pin may not have any external connection.

Device Functional Modes (continued)

7.4.1.3 Multiple Devices: Daisy-Chain Topology

A typical connection diagram showing multiple devices in a daisy-chain topology is shown in Figure 72.

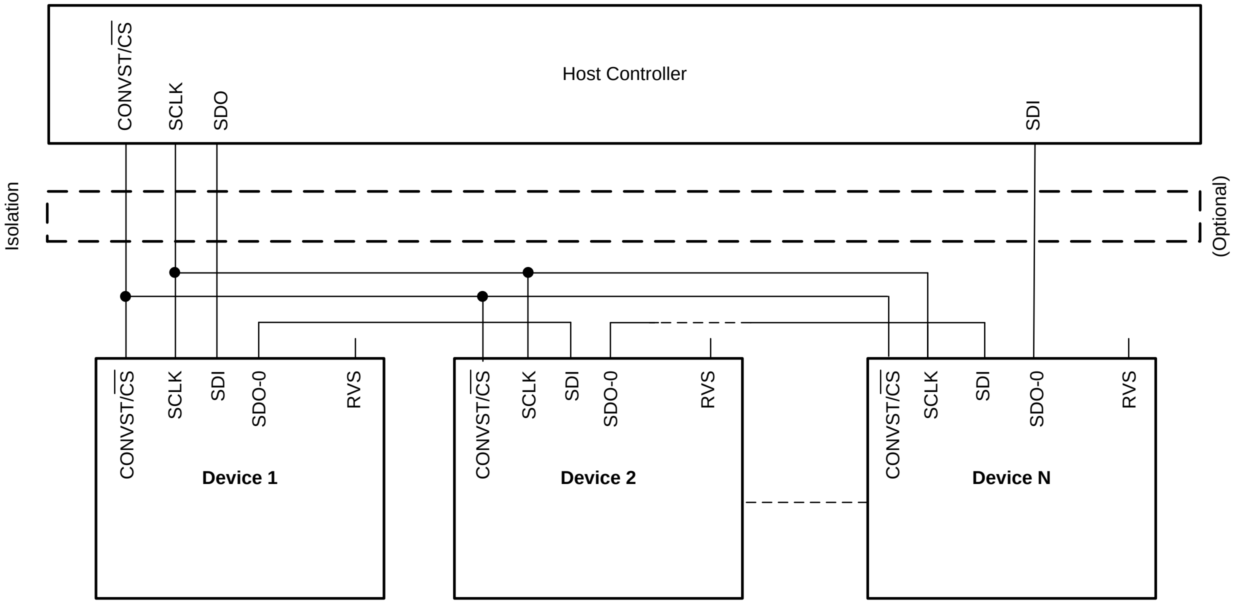


Figure 72. Daisy-Chain Connection Schematic

The CONVST/$\overline{CS}$ and SCLK inputs of all devices are connected together and controlled by a single CONVST/$\overline{CS}$ and SCLK pin of the host controller, respectively. The SDI input pin of the first device in the chain (device 1) is connected to the SDO-x pin of the host controller, the SDO-0 output pin of device 1 is connected to the SDI input pin of device 2, and so forth. The SDO-0 output pin of the last device in the chain (device N) is connected to the SDI pin of the host controller.

To operate multiple devices in a daisy-chain topology, the host controller must program the configuration registers in each device with identical values. The devices must operate with a single SDO-0 output, using the external clock with any of the legacy, SPI-compatible protocols for data read and data write operations. In the SDO_CTL_REG register, bits 7-0 must be programmed to 00h.

All devices in the daisy-chain topology sample their analog input signals on the rising edge of the CONVST/$\overline{CS}$ signal and the data transfer frame starts with a falling edge of the same signal. At the launch edge of the SCLK signal, every device in the chain shifts out the MSB to the SDO-0 pin. On every SCLK capture edge, each device in the chain shifts in data received on its SDI pin as the LSB bit of the unified shift register; see Figure 69. Therefore, in a daisy-chain configuration, the host controller receives the data of device N, followed by the data of device N-1, and so forth (in MSB-first fashion). On the rising edge of the CONVST/$\overline{CS}$ signal, each device decodes the contents in its unified and takes appropriate action.

For N devices connected in a daisy-chain topology, an optimal data transfer frame must contain 32 × N SCLK capture edges (see Figure 73). A shorter data transfer frame can result in an erroneous device configuration and must be avoided. For a data transfer frame with > 32 × N SCLK capture edges, the host controller must appropriately align the configuration data for each device before bringing CONVST/$\overline{CS}$ high.

Note that the overall throughput of the system is proportionally reduced with the number of devices connected in a daisy-chain topology.

Device Functional Modes (continued)

A typical timing diagram for three devices connected in a daisy-chain topology and using the SPI-00-S protocol is shown in Figure 73.

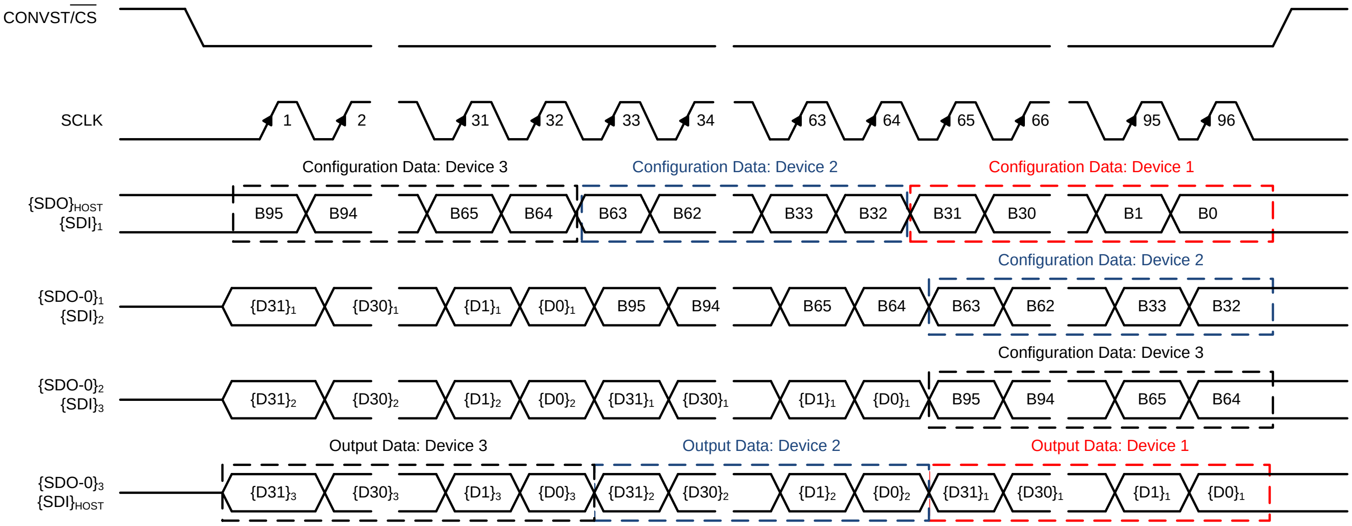


Figure 73. Three Devices in Daisy-Chain Mode Timing Diagram

7.4.2 Device Operational Modes

As shown in Figure 74, the device supports three functional states: RESET, ACQ, and CONV. The device state is determined by the status of the CONVST/$\overline{\text{CS}}$ and $\overline{\text{RST}}$ control signals provided by the host controller.

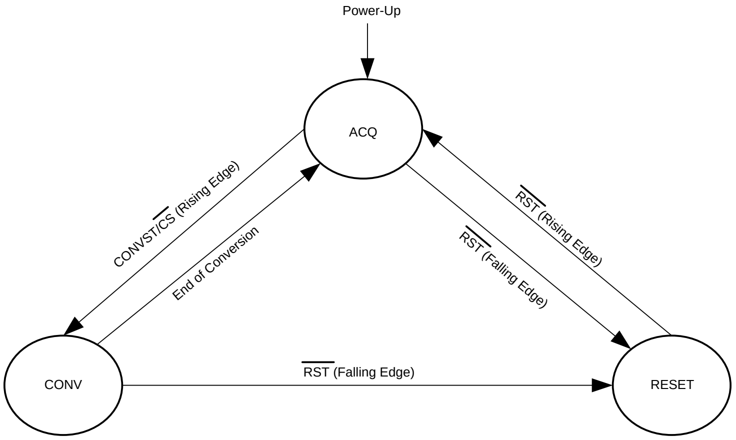


Figure 74. Device Functional States

Device Functional Modes (continued)

7.4.2.1 RESET State

The device features an active-low $\overline{\text{RST}}$ pin that is an asynchronous digital input. In order to enter a RESET state, the $\overline{\text{RST}}$ pin must be pulled low and kept low for the t_{wl_RST} duration (as specified in the *Timing Requirements: Asynchronous Reset* table).

The device features two different types of reset functions: an application reset or a power-on reset (POR). The functionality of the $\overline{\text{RST}}$ pin is determined by the state of the RSTn_APP bit in the RST_PWRCTL_REG register.

- In order to configure the $\overline{\text{RST}}$ pin to issue an application reset, the RSTn_APP bit in the RST_PWRCTL_REG register must be configured to 1b. In this RESET state, all configuration registers (see the *Register Maps* section) are reset to their default values, the RVS pins remain low, and the SDO-x pins are tri-stated.
- The default configuration for the $\overline{\text{RST}}$ pin is to issue a power-on reset when pulled to a low level. The RSTn_APP bit is set to 0b in this state. When a POR is issued, all internal circuitry of the device (including the PGA, ADC driver, and voltage reference) are reset. When the device comes out of the POR state, the $t_{D\_RST\_POR}$ time duration must be allowed for (see the *Timing Requirements: Asynchronous Reset* table) in order for the internal circuitry to accurately settle.

In order to exit any of the RESET states, the $\overline{\text{RST}}$ pin must be pulled high with CONVST/$\overline{\text{CS}}$ and SCLK held low. After a delay of $t_{D\_RST\_POR}$ or $t_{D\_RST\_APP}$ (see the *Timing Requirements: Asynchronous Reset* table), the device enters ACQ state and the RVS pin goes high.

To operate the device in any of the other two states (ACQ or CONV), the $\overline{\text{RST}}$ pin must be held high. With the $\overline{\text{RST}}$ pin held high, transitions on the CONVST/$\overline{\text{CS}}$ pin determine the functional state of the device. A typical conversion cycle is illustrated in Figure 1.

7.4.2.2 ACQ State

In ACQ state, the device acquires the analog input signal. The device enters ACQ state on power-up, after any asynchronous reset, or after the end of every conversion.

The falling edge of the $\overline{\text{RST}}$ falling edge takes the device from an ACQ state to a RESET state. A rising edge of the CONVST/$\overline{\text{CS}}$ signal takes the device from ACQ state to a CONV state.

The device offers a low-power NAP mode to reduce power consumption in the ACQ state; see the *NAP Mode* section for more details on NAP mode.

7.4.2.3 CONV State

The device moves from ACQ state to CONV state on the rising edge of the CONVST/$\overline{\text{CS}}$ signal. The conversion process uses an internal clock and the device ignores any further transitions on the CONVST/$\overline{\text{CS}}$ signal until the ongoing conversion is complete (that is, during the time interval of t_{conv}).

At the end of conversion, the device enters ACQ state. The cycle time for the device is given by Equation 1:

$$t_{cycle\text{-}min} = t_{conv} + t_{acq\text{-}min} \tag{1}$$

NOTE

The conversion time, t_{conv}, can vary within the specified limits of t_{conv_min} and t_{conv_max} (as specified in the *Timing Requirements: Conversion Cycle* table). After initiating a conversion, the host controller must monitor for a low-to-high transition on the RVS pin or wait for the t_{conv_max} duration to elapse before initiating a new operation (data transfer or conversion). If RVS is not monitored, substitute t_{conv} in Equation 1 with t_{conv_max}.

7.5 Programming

The device features nine configuration registers (as described in the *Register Maps* section) and supports two types of data transfer operations: data write (the host configures the device), and data read (the host reads data from the device).

7.5.1 Data Transfer Frame

A data transfer frame between the device and the host controller begins at the falling edge of the CONVST/$\overline{\text{CS}}$ pin and ends when the device starts conversion at the subsequent rising edge. The host controller can initiate a data transfer frame by bringing the CONVST/$\overline{\text{CS}}$ signal low (as shown in Figure 75) after the end of the CONV phase, as described in the *CONV State* section.

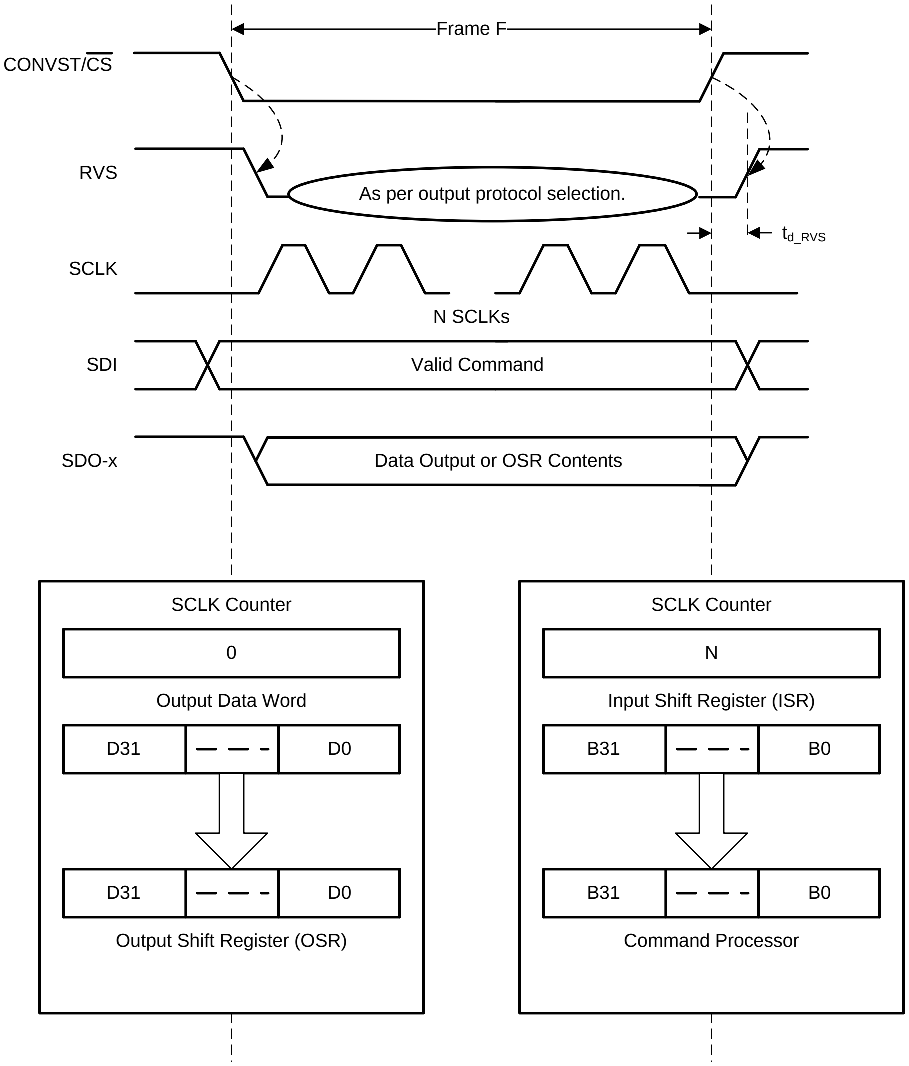


Figure 75. Data Transfer Frame

Programming (continued)

For a typical data transfer frame F:

1. The host controller pulls CONVST/$\overline{\text{CS}}$ low to initiate a data transfer frame. On the falling edge of the CONVST/$\overline{\text{CS}}$ signal:
   - RVS goes low, indicating the beginning of the data transfer frame.
   - The internal SCLK counter is reset to 0.
   - The device takes control of the data bus. As illustrated in Figure 75, the contents of the output data word are loaded into the 32-bit output shift register (OSR).
   - The internal configuration register is reset to 0000h, corresponding to a NOP command.
2. During the frame, the host controller provides clocks on the SCLK pin:
   - On each SCLK capture edge, the SCLK counter is incremented and the data bit received on the SDI pin is shifted into the LSB of the input shift register.
   - On each launch edge of the output clock (SCLK in this case), the MSB of the output shift register data is shifted out on the selected SDO-x pins.
   - The status of the RVS pin depends on the output protocol selection (see the *Protocols for Reading From the Device* section).
3. The host controller pulls the CONVST/$\overline{\text{CS}}$ pin high to end the data transfer frame. On the rising edge of CONVST/$\overline{\text{CS}}$:
   - The SDO-x pins go to tri-state.
   - As illustrated in Figure 75, the contents of the input shift register are transferred to the command processor for decoding and further action.
   - RVS output goes low, indicating the beginning of conversion.

After pulling CONVST/$\overline{\text{CS}}$ high, the host controller must monitor for a low-to-high transition on the RVS pin or wait for the t_{conv_max} time (see the *Timing Requirements: Conversion Cycle* table) to elapse before initiating a new data transfer frame.

At the end of the data transfer frame F:

- If the SCLK counter = 32, then the device treats the frame F as an *optimal* data transfer frame for any read or write operation. At the end of an optimal data transfer frame, the command processor treats the 32-bit contents of the input shift register as a valid command word.
- If the SCLK counter is < 32, then the device treats the frame F as a *short* data transfer frame.
  - The data write operation to the device in invalid and the device treats this frame as an NOP command.
  - The output data bits transferred during a short frame on the SDO-x pins are still valid data. The host controller can use the short data transfer frame to read only the required number of MSB bits from the 32-bit output shift register.
- If the SCLK counter is > 32, then the device treats the frame F as a *long* data transfer frame. At the end of a long data transfer frame, the command processor treats the 32-bit contents of the input shift register as a valid command word. There is no restriction on the maximum number of clocks that can be provided within any data transfer frame F. However, when the host controller provides a long data transfer frame, the last 32 bits shifted into the device prior to the CONVST/$\overline{\text{CS}}$ rising edge must constitute the desired command.

Programming (continued)

7.5.2 Input Command Word and Register Write Operation

Any data write operation to the device is always synchronous to the external clock provided on the SCLK pin.

The device allows either one byte or two bytes (equivalent to half a word) to be read or written during any device programming operation. Table 5 lists the input commands supported by the device. The input commands associated with reading or writing two bytes in a single operation are suffixed as *HWORD*.

For any HWORD command, the LSB of the 9-bit address is always ignored and considered as 0b. For example, regardless whether address 04h or 05h is entered for any particular HWORD command, the device always exercises the command on address 04h.

Table 5. List of Input Commands

OPCODE B[31:0]	COMMAND ACRONYM	COMMAND DESCRIPTION
00000000_000000000_00000000_00000000	NOP	No operation
11000_xx_<9-bit address>_<16-bit data>	CLEAR_HWORD	• Command used to clear any (or a group of) bits of a register. • Any bit marked 1 in the data field results in that particular bit of the specified register being reset to 0, leaving the other bits unchanged. • Half-word command (that is, the command functions on 16 bits at a time). • LSB of the 9-bit address is always ignored and considered as 0b.
11001_xx_<9-bit address>_00000000_00000000	READ_HWORD	• Command used to perform a 16-bit read operation. • Half-word command (that is, the device outputs 16 bits of register data at a time). • LSB of the 9-bit address is always ignored and considered as 0b. • Upon receiving this command, the device sends out 16 bits of the register in the next frame.
01001_xx_<9-bit address>_00000000_00000000	READ	• Same as the READ_HWORD except that only eight bits of the register (byte read) are returned in the next frame.
11010_00_<9-bit address>_<16-bit data>	WRITE	• Half-word write command (two bytes of input data are written into the specified address). • LSB of the 9-bit address is always ignored and considered as 0b.
11010_01_<9-bit address>_<16-bit data>		• Half-word write command. • LSB of the 9-bit address is always ignored and considered as 0b. • With this command, only the MS byte of the 16-bit data word is written at the specified register address. The LS byte is ignored.
11010_10_<9-bit address>_<16-bit data>		• Half-word write command. • LSB of the 9-bit address is always ignored and considered as 0b. • With this command, only the LS byte of the 16-bit data word is written at the specified register address. The MS byte is ignored.
11011_xx_<9-bit address>_<16-bit data>	SET_HWORD	• Command used to set any (or a group of) bits of a register. • Any bit marked 1 in the data field results in that particular bit of the specified register being set to 1, leaving the other bits unchanged. • Half-word command (that is, the command functions on 16 bits at a time). • LSB of the 9-bit address is always ignored and considered as 0b.
All other input command combinations	NOP	No operation

All input commands (including the CLEAR_HWORD, WRITE, and SET_HWORD commands listed in Table 5) used to configure the internal registers must be 32 bits long. If any of these commands are provided in a particular data frame F, that command gets executed at the rising edge of the CONVST/$\overline{\text{CS}}$ signal.

7.5.3 Output Data Word

The data read from the device can be synchronized to the external clock on the SCLK pin or to an internal clock of the device by programming the configuration registers (see the *Data Transfer Protocols* section for details).

In any data transfer frame, the contents of the internal output shift register are shifted out on the SDO-x pins. The output data for any frame (F+1) is determined by the command issued in frame F and the status of DATA_VAL[2:0] bits:

- If DATA_VAL[2:0] bits in DATAOUT_CTL_REG register are set to 1xxb, then the output data word for frame (F+1) contains fixed data pattern as described in the DATAOUT_CTL_REG register.
- If a valid READ command is issued in frame F, the output data word for frame (F+1) contains 8-bit register data, followed by 0's.
- If a valid READ_HWORD command is issued in frame F, the output data word for frame (F+1) contains 16-bit register data, followed by 0's.
- For all other combinations, the output data word for frame (F+1) contains the latest 18-bit conversion result. Program the DATAOUT_CTL_REG register to append various data flags to the conversion result. The data flags are appended as per following sequence:
  1. DEVICE_ADDR[3:0] bits are appended if the DEVICE_ADDR_INCL bit is set to 1
  2. AVDD ALARM FLAGS are appended if the VDD_ACTIVE_ALARM_INCL bit is set to 1
  3. INPUT ALARM FLAGS are appended if the IN_ACTIVE_ALARM_INCL bit is set to 1
  4. ADC INPUT RANGE FLAGS are appended if the RANGE_INCL bit is set to 1
  5. PARITY bits are appended if the PAR_EN bit is set to 1
  6. All the remaining bits in the 32-bit output data word are set to 0.

Table 6 shows the output data word with all data flags enabled.

Table 6. Output Data Word With All Data Flags Enabled

DEVICE_ADDR_INCL = 1b, VDD_ACTIVE_ALARM_INCL = 1b, IN_ACTIVE_ALARM_INCL = 1b, RANGE_INCL = 1b, and PAR_EN = 1b						
D[31:14]	**D[13:10]**	**D[9:8]**	**D[7:6]**	**D[5:2]**	**D[1:0]**	**No trailing 0's**
Conversion result	Device address	AVDD alarm flags	Input alarm flags	ADC input range	Parity bits	No trailing 0's

Table 7 shows output data word with only some of the data flags enabled.

Table 7. Output Data Word With Only Some Data Flags Enabled

DEVICE_ADDR_INCL = 0b, VDD_ACTIVE_ALARM_INCL = 1b, IN_ACTIVE_ALARM_INCL = 0b, RANGE_INCL = 1b, and PAR_EN = 1b				
D[31:14]	**D[13:12]**	**D[11:8]**	**D[7:6]**	**D[5:0]**
Conversion result	AVDD alarm flags	ADC input range	Parity bits	000000b

7.5.4 Data Transfer Protocols

The device features a multiSPI interface that allows the host controller to operate at slower SCLK speeds and still achieve the required cycle time with a faster response time.

- For any data write operation, the host controller can use any of the four legacy, SPI-compatible protocols to configure the device, as described in the *Protocols for Configuring the Device* section.
- For any data read operation from the device, the multiSPI interface module offers the following options:
  - Legacy, SPI-compatible protocol with a single SDO-x (see the *Legacy, SPI-Compatible (SYS-xy-S) Protocols with a Single SDO-x* section)
  - Legacy, SPI-compatible protocol with dual SDO-x (see the *Legacy, SPI-Compatible (SYS-xy-S) Protocols with Dual SDO-x* section)
  - ADC master clock or source-synchronous (SRC) protocol for data transfer (see the *Source-Synchronous (SRC) Protocols* section)

7.5.4.1 Protocols for Configuring the Device

As described in Table 8, the host controller can use any of the four legacy, SPI-compatible protocols (SPI-00-S, SPI-01-S, SPI-10-S, or SPI-11-S) to write data into the device.

Table 8. SPI Protocols for Configuring the Device

PROTOCOL	SCLK POLARITY (At CS Falling Edge)	SCLK PHASE (Capture Edge)	SDI_CTL_REG	SDO_CTL_REG	DIAGRAM
SPI-00-S	Low	Rising	00h	00h	Figure 76
SPI-01-S	Low	Falling	01h	00h	Figure 76
SPI-10-S	High	Falling	02h	00h	Figure 77
SPI-11-S	High	Rising	03h	00h	Figure 77

On power-up or after coming out of any asynchronous reset, the device supports the SPI-00-S protocol for data read and data write operations. To select a different SPI-compatible protocol, program the SDI_MODE[1:0] bits in the SDI_CNTL_REG register. This first write operation must adhere to the SPI-00-S protocol. Any subsequent data transfer frames must adhere to the newly-selected protocol. Note that the SPI protocol selected by the configuration of the SDI_MODE[1:0] is applicable to both read and write operations.

Figure 76 and Figure 77 detail the four protocols using an optimal data frame; see the *Timing Requirements: SPI-Compatible Serial Interface* table for associated timing parameters.

NOTE

As explained in the *Data Transfer Frame* section, a valid write operation to the device requires a minimum of 32 SCLKs to be provided within a data transfer frame.

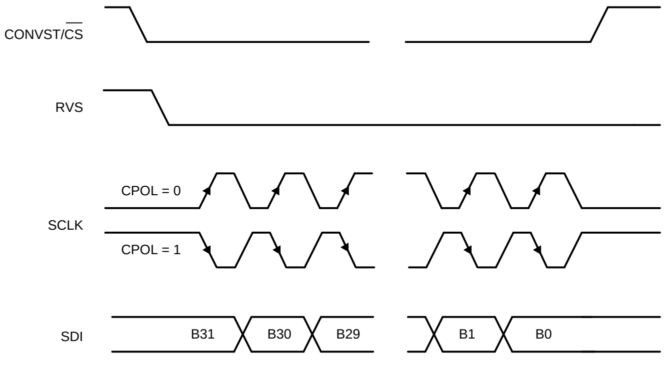


Figure 76. Standard SPI Timing Protocol (CPHA = 0, 32 SCLK Cycles)

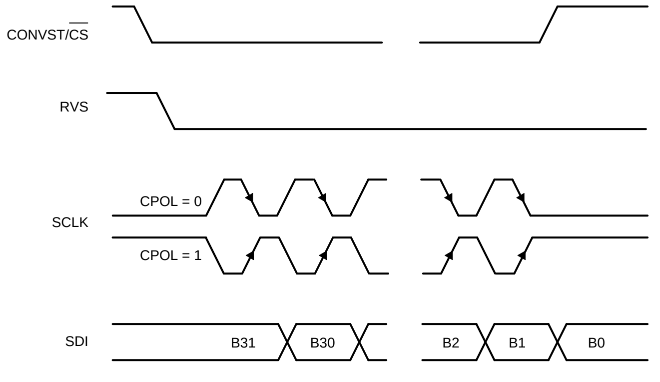


Figure 77. Standard SPI Timing Protocol (CPHA = 1, 32 SCLK Cycles)

7.5.4.2 Protocols for Reading From the Device

The protocols for the data read operation can be broadly classified into three categories:

1. Legacy, SPI-compatible protocols with a single SDO-x
2. Legacy, SPI-compatible protocols with dual SDO-x
3. ADC master clock or source-synchronous (SRC) protocol for data transfer

7.5.4.2.1 Legacy, SPI-Compatible (SYS-xy-S) Protocols with a Single SDO-x

As shown in Table 9, the host controller can use any of the four legacy, SPI-compatible protocols (SPI-00-S, SPI-01-S, SPI-10-S, or SPI-11-S) to read data from the device.

Table 9. SPI Protocols for Reading From the Device

PROTOCOL	SCLK POLARITY (At $\overline{CS}$ Falling Edge)	SCLK PHASE (Capture Edge)	MSB BIT LAUNCH EDGE	SDI_CTL_REG	SDO_CTL_REG	DIAGRAM
SPI-00-S	Low	Rising	$\overline{CS}$ falling	00h	00h	Figure 78
SPI-01-S	Low	Falling	1st SCLK rising	01h	00h	Figure 78
SPI-10-S	High	Falling	$\overline{CS}$ falling	02h	00h	Figure 79
SPI-11-S	High	Rising	1st SCLK falling	03h	00h	Figure 79

On power-up or after coming out of any asynchronous reset, the device supports the SPI-00-S protocol for data read and data write operations. To select a different SPI-compatible protocol for both the data transfer operations:

1. Program the SDI_MODE[1:0] bits in the SDI_CTL_REG register. This first write operation must adhere to the SPI-00-S protocol. Any subsequent data transfer frames must adhere to the newly-selected protocol.
2. Set the SDO_MODE[1:0] bits = 00b in the SDO_CTL_REG register.

NOTE

The SPI transfer protocol selected by configuring the SDI_MODE[1:0] bits in the SDI_CTL_REG register determines the data transfer protocol for both write and read operations. Either data can be read from the device using the selected SPI protocol by configuring the SDO_MODE[1:0] bits = 00b in the SDO_CTL_REG register, or one of the SRC protocols can be selected for data read, as explained in the *Source-Synchronous (SRC) Protocols* section.

When using any of the SPI-compatible protocols, the RVS output remains low throughout the data transfer frame; see the *Timing Requirements: SPI-Compatible Serial Interface* table for associated timing parameters.

Figure 78 and Figure 79 explain the details of the four protocols. As explained in the *Data Transfer Frame* section, the host controller can use a short data transfer frame to read only the required number of MSB bits from the 32-bit output data word.

If the host controller uses a long data transfer frame with SDO_CNTL_REG[7:0] = 00h, then the device exhibits daisy-chain operation (see the *Multiple Devices: Daisy-Chain Topology* section).

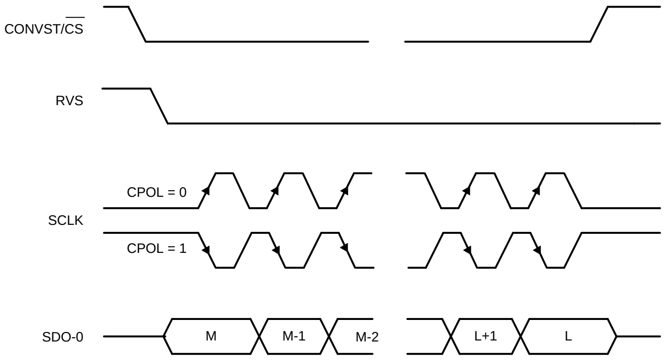


Figure 78. Standard SPI Timing Protocol (CPHA = 0, Single SDO-x)

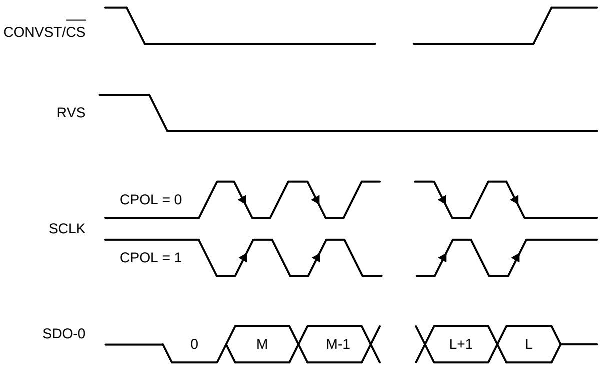


Figure 79. Standard SPI Timing Protocol (CPHA = 1, Single SDO-x)

7.5.4.2.2 Legacy, SPI-Compatible (SYS-xy-S) Protocols with Dual SDO-x

The device provides an option to increase the SDO-x bus width from one bit (default, single SDO-x) to two bits (dual SDO-x) when operating with any of the data transfer protocols. In order to operate the device in dual SDO mode, the SDO1_CONFIG[1:0] bits in the SDO_CTL_REG register must be set to 11b. In this mode, the ALARM/SDO-1/GPO pin functions as SDO-1.

In dual SDO mode, two bits of data are launched on the two SDO-x pins (SDO-0 and SDO-1) on every SCLK launch edge, as shown in Figure 80 and Figure 81.

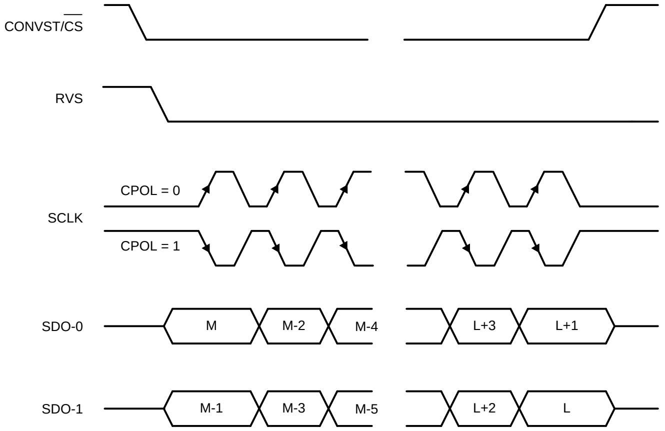


Figure 80. Standard SPI Timing Protocol (CPHA = 0, Dual SDO-x)

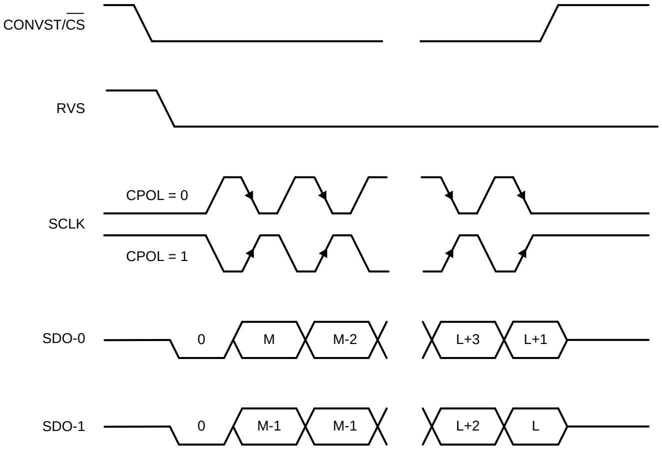


Figure 81. Standard SPI Timing Protocol (CPHA = 1, Dual SDO-x)

NOTE

For any particular SPI protocol, the device follows the same timing specifications for single and dual SDO modes. The only difference is that the device requires half as many SCLK cycles to output the same number of bits when in single SDO mode, thus reducing the minimum required SCLK frequency for a certain sampling rate of the ADC.

7.5.4.2.3 Source-Synchronous (SRC) Protocols

The multiSPI interface supports an ADC master clock or source-synchronous mode of data transfer between the device and host controller. In this mode, the device provides an output clock that is synchronous with the output data. Furthermore, the host controller can also select the output clock source and data bus width options in this mode of operation. In all SRC modes of operation, the RVS pin provides the output clock, synchronous to the device data output.

The SRC protocol allows the clock source (internal or external) and the width of the output bus to be configured, similar to the SPI protocols.

7.5.4.2.3.1 Output Clock Source Options

The device allows the output clock on the RVS pin to be synchronous to either the external clock provided on the SCLK pin or to the internal clock of the device. This selection is done by configuring the SSYNC_CLK bit, as explained in the SDO_CTL_REG register. The timing diagram and specifications for operating the device with an SRC protocol in external CLK mode are provided in Figure 7 and the *Timing Requirements: Source-Synchronous Serial Interface (External Clock)* table. The timing diagram and specifications for operating the device with an SRC protocol in internal CLK mode are provided in Figure 8 and the *Timing Requirements: Source-Synchronous Serial Interface (Internal Clock)* table.

7.5.4.2.3.2 Output Bus Width Options

The device provides an option to increase the SDO-x bus width from one bit (default, single SDO-x) to two bits (dual SDO-x) when operating with any of the SRC protocols. In order to operate the device in dual SDO mode, the SDO1_CONFIG[1:0] bits in the SDO_CTL_REG register must be set to 11b. In this mode, the ALARM/SDO-1/GPO pin functions as SDO-1.

NOTE

For any particular SRC protocol, the device follows the same timing specifications for single and dual SDO modes. The only difference is that the device requires half as many clock cycles to output the same number of bits when in single SDO mode, thus reducing the minimum required clock frequency for a certain sampling rate of the ADC.

7.6 Register Maps

7.6.1 Device Configuration and Register Maps

The device features nine configuration registers, mapped as described in Table 10. Each configuration registers is comprised of four registers, each containing a data byte.

Table 10. Configuration Registers Mapping

ADDRESS	REGISTER NAME	REGISTER FUNCTION
00h	DEVICE_ID_REG	Device ID register
04h	RST_PWRCTL_REG	Reset and power control register
08h	SDI_CTL_REG	SDI data input control register
0Ch	SDO_CTL_REG	SDO-x data input control register
10h	DATAOUT_CTL_REG	Output data control register
14h	RANGE_SEL_REG	Input range selection control register
20h	ALARM_REG	ALARM output register
24h	ALARM_H_TH_REG	ALARM high threshold and hysteresis register
28h	ALARM_L_TH_REG	ALARM low threshold register

7.6.1.1 *DEVICE_ID_REG Register (address = 00h)*

This register contains the unique identification numbers associated to a device that is used in a daisy-chain configuration involving multiple devices.

Figure 82. DEVICE_ID_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">Reserved</td><td colspan="4">Reserved</td><td colspan="4">DEVICE_ADDR[3:0]</td></tr>
<tr><td colspan="8">R-00h</td><td colspan="4">R-0000b</td><td colspan="4">R/W-0000b</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">Reserved</td></tr>
<tr><td colspan="16">R-0000h</td></tr>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset; -0, -1 = Condition after application reset;
-<0>, -<1> = Condition after power-on reset
Address for bits 7-0 = 00h
Address for bits 15-8 = 01h
Address for bits 23-16 = 02h
Address for bits 31-24 = 03h

Table 11. DEVICE_ID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Reserved	R	00h	Reserved. Reads return 00h.
23-20	Reserved	R	0000b	Reserved. Reads return 0000b.
19-16	DEVICE_ADDR[3:0] (1)	R	0000b	These bits can be used to identify up to 16 different devices in a system.
15-0	Reserved	R	0000h	Reserved. Reads return 0000h.

(1) These bits are useful in daisy-chain mode.

7.6.1.2 RST_PWRCTL_REG Register (address = 04h)

This register controls the reset and power-down features offered by the converter.

Any write operation to the RST_PWRCTL_REG register must be preceded by a write operation with the register address set to 05h and the register data set to 69h.

Figure 83. RST_PWRCTL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0000h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKEY[7:0]								Reserved		VDD_AL_DIS	IN_AL_DIS	Reserved	RSTn_APP	NAP_EN	PWRDN
R/W-00h								R-00b		R/W-0b	R/W-0b	R-0b	R/W-<0>b	R/W-<0>b	R/W-0b

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset; -0, -1 = Condition after application reset;
-<0>, -<1> = Condition after power-on reset

Address for bits 7-0 = 04h Address for bits 15-8 = 05h Address for bits 23-16 = 06h Address for bits 31-24 = 07h

Table 12. RST_PWRCTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0000h	Reserved. Reads return 0000h.
15-8	WKEY[7:0]	R/W	00h	This value functions as a protection key to enable writes to bits 5-0. Bits are written only if WKEY is set to 69h first.
7-6	Reserved	R	00b	Reserved. Reads return 00b
5	VDD_AL_DIS	R/W	0b	0b = VDD alarm is enabled 1b = VDD alarm is disabled
4	IN_AL_DIS	R/W	0b	0b = Input alarm is enabled 1b = Input alarm is disabled
3	Reserved	R	0b	Reserved. Reads return 0h.
2	RSTn_APP(1)	R/W	0b	0b = $\overline{\text{RST}}$ pin functions as a POR class reset (causes full device initialization) 1b = $\overline{\text{RST}}$ pin functions as an application reset (only user-programmed modes are cleared)
1	NAP_EN(2)	R/W	0b	0b = Disables the NAP mode of the converter 1b = Enables the converter to enter NAP mode if CONVST/$\overline{\text{CS}}$ is held high after the current conversion completes
0	PWRDN(2)	R/W	0b	0b = Puts the converter into active mode 1b = Puts the converter into power-down mode

(1) Setting this bit forces the $\overline{\text{RST}}$ pin to function as an application reset until the next power cycle.
(2) See the *Electrical Characteristics* table for details on the latency encountered when entering and exiting the associated low-power mode.

7.6.1.3 SDI_CTL_REG Register (address = 08h)

This register configures the protocol used for writing data to the device.

Figure 84. SDI_CTL_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">Reserved</td></tr>
<tr><td colspan="16">R-0000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">Reserved</td><td colspan="6">Reserved</td><td colspan="2">SDI_MODE [1:0]</td></tr>
<tr><td colspan="8">R-00h</td><td colspan="6">R-000000b</td><td colspan="2">R/W-<00>b</td></tr>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset; -0, -1 = Condition after application reset;
-<0>, -<1> = Condition after power-on reset

Address for bits 7-0 = 08h Address for bits 15-8 = 09h Address for bits 23-16 = 0Ah Address for bits 31-24 = 0Bh

Table 13. SDI_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0000h	Reserved. Reads return 0000h.
15-8	Reserved	R	00h	Reserved. Reads return 00h.
7-2	Reserved	R	000000b	Reserved. Reads return 000000b.
1-0	SDI_MODE[1:0]	R/W	00b	These bits select the protocol for reading from or writing to the device. 00b = Standard SPI with CPOL = 0 and CPHASE = 0 01b = Standard SPI with CPOL = 0 and CPHASE = 1 10b = Standard SPI with CPOL = 1 and CPHASE = 0 11b = Standard SPI with CPOL = 1 and CPHASE = 1

7.6.1.4 SDO_CTL_REG Register (address = 0Ch)

This register controls the data protocol used to transmit data out from the SDO-x pins of the device.

Figure 85. SDO_CTL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0000h															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			GPO_VAL	Reserved		SDO1_ CONFIG [1:0]		Reserved	SSYNC_CLK	Reserved				SDO_ MODE[1:0]	
R-000b			R/W-0b	R-00b		R/W-00b		R-0b	R/W-<0>b	R-0h				R/W-<0>b	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset; -0, -1 = Condition after application reset;
-<0>, -<1> = Condition after power-on reset

Address for bits 7-0 = 0Ch Address for bits 15-8 = 0Dh Address for bits 23-16 = 0Eh Address for bits 31-24 = 0Fh

Table 14. SDO_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0000h	Reserved. Reads return 0h.
15-13	Reserved	R	000b	Reserved. Reads return 000b.
12	GPO_VAL	R/W	0b	1-bit value for the output on the GPO pin.
11-10	Reserved	R	00b	Reserved. Reads return 00b.
9-8	SDO1_CONFIG[1:0]	R/W	00b	Two bits are used to configure ALARM/SDO-1/GPO: 00b = SDO-1 is always tri-stated; 1-bit SDO mode 01b = SDO-1 functions as ALARM; 1-bit SDO mode 10b = SDO-1 functions as GPO; 1-bit SDO mode 11b = SDO-1 combined with SDO-0 offers a 2-bit SDO mode
7	Reserved	R	0b	Reserved. Reads return 0b.
6	SSYNC_CLK (1)	R/W	0b	This bit controls the source of the clock selected for source-synchronous transmission. 0b = External SCLK (no division) 1b = Internal clock (no division)
5-2	Reserved	R	0000b	Reserved. Reads return 0000b.
1-0	SDO_MODE[1:0]	R/W	00b	These bits control the data output modes of the device. 0xb = SDO mode follows the same SPI protocol as that used for SDI; see the SDI_CTL_REG register 10b = Invalid configuration 11b = SDO mode follows the ADC master clock or source-synchronous protocol

(1) This bit takes effect **only** in the ADC master clock or source-synchronous mode of operation.

7.6.1.5 DATAOUT_CTL_REG Register (address = 10h)

This register controls the data output by the device.

Figure 86. DATAOUT_CTL_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">Reserved</td></tr>
<tr><td colspan="16">R-0000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Reserved</td><td>DEVICE_ADDR_INCL</td><td colspan="2">VDD_ACTIVE_ALARM_INCL[1:0]</td><td colspan="2">IN_ACTIVE_ALARM_INCL[1:0]</td><td>Reserved</td><td>RANGE_INCL</td><td colspan="4">Reserved</td><td>PAR_EN</td><td colspan="3">DATA_VAL [2:0]</td></tr>
<tr><td>R-0b</td><td>R/W-0b</td><td colspan="2">R/W-0b</td><td colspan="2">R/W-0b</td><td>R-0b</td><td>R/W-0b</td><td colspan="4">R-0000b</td><td>R/W-<0>b</td><td colspan="3">R/W-000b</td></tr>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset; -0, -1 = Condition after application reset;
-<0>, -<1> = Condition after power-on reset

Address for bits 7-0 = 10h Address for bits 15-8 = 11h Address for bits 23-16 = 12h Address for bits 31-24 = 13h

Table 15. DATAOUT_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0000h	Reserved. Reads return 0000h.
15	Reserved	R	0b	Reserved. Reads return 0b.
14	DEVICE_ADDR_INCL	R/W	0b	Control to include the 4-bit DEVICE_ADDR register value in the SDO-x output bit stream. 0b = Do not include the register value 1b = Include the register value
13-12	VDD_ACTIVE_ALARM_INCL[1:0]	R/W	00b	Control to include the active VDD ALARM flags in the SDO-x output bit stream. 00b = Do not include 01b = Include ACTIVE_VDD_H_FLAG 10b = Include ACTIVE_VDD_L_FLAG 11b = Include both flags
11-10	IN_ACTIVE_ALARM_INCL[1:0]	R/W	00b	Control to include the active input ALARM flags in the SDO-x output bit stream. 00b = Do not include 01b = Include ACTIVE_IN_H_FLAG 10b = Include ACTIVE_IN_L_FLAG 11b = Include both flags
9	Reserved	R	0b	Reserved. Reads return 0h.
8	RANGE_INCL	R/W	0b	Control to include the 4-bit input range setting in the SDO-x output bit stream. 0b = Do not include the range configuration register value 1b = Include the range configuration register value
7-4	Reserved	R	0000b	Reserved. Reads return 0000b.
3	PAR_EN (1)	R/W	0b	0b = Output data does not contain parity information 1b = Two parity bits (ADC output and output data frame) are appended to the LSBs of the output data The ADC output parity bit reflects an even parity for the ADC output bits only. The output data frame parity bit reflects an even parity signature for the entire output data frame, including the ADC output bits and any internal flags or register settings.
2-0	DATA_VAL[2:0]	R/W	000b	These bits control the data value output by the converter. 0xxb = Value output is the conversion data 100b = Value output is all 0's 101b = Value output is all 1's 110b = Value output is alternating 0's and 1's 111b = Value output is alternating 00's and 11's

(1) Setting this bit increases the length of the output data by two bits.

7.6.1.6 RANGE_SEL_REG Register (address = 14h)

This register controls the configuration of the internal reference and input voltage ranges for the converter.

Figure 87. RANGE_SEL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0000h															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved								Reserved	INTREF_ DIS	Reserved		RANGE_SEL[3:0]			
R-00h								R-0b	R/W-0b	R-00b		R/W-<0000>b			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset; -0, -1 = Condition after application reset;
-<0>, -<1> = Condition after power-on reset

Address for bits 7-0 = 14h Address for bits 15-8 = 15h Address for bits 23-16 = 16h Address for bits 31-24 = 17h

Table 16. RANGE_SEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0000h	Reserved. Reads return 0000h.
15-8	Reserved	R	00h	Reserved. Reads return 00h.
7	Reserved	R	0b	Reserved. Reads return 0b.
6	INTREF_DIS	R/W	0b	Control to disable the ADC internal reference. 0b = Internal reference is enabled 1b = Internal reference is disabled
5-4	Reserved	R	00b	Reserved. Reads return 00b.
3-0	RANGE_SEL[3:0]	R/W	0000b	These bits comprise the 4-bit register that selects the nine input ranges of the ADC. 0000b = ±3 × V_{REF} 0001b = ±2.5 × V_{REF} 0010b = ±1.5 × V_{REF} 0011b = ±1.25 × V_{REF} 0100b = ±0.625 × V_{REF} 1000b = 3 × V_{REF} 1001b = 2.5 × V_{REF} 1010b = 1.5 × V_{REF} 1011b = 1.25 × V_{REF}

7.6.1.7 ALARM_REG Register (address = 20h)

This register contains the output alarm flags (active and tripped) for the input and AVDD alarm.

Figure 88. ALARM_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0000h															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACTIVE_VDD_L_FLAG	ACTIVE_VDD_H_FLAG	Reserved		ACTIVE_IN_L_FLAG	ACTIVE_IN_H_FLAG	Reserved		TRP_VDD_L_FLAG	TRP_VDD_H_FLAG	TRP_IN_L_FLAG	TRP_IN_H_FLAG	Reserved			OVW_ALARM
R-0b	R-0b	R-00b		R-0b	R-0b	R-00b		R-0b	R-0b	R-0b	R-0b	R-000b			R-0b

LEGEND: R = Read only; -n = value after reset; -0, -1 = Condition after application reset; -<0>, -<1> = Condition after power-on reset

Address for bits 7-0 = 20h Address for bits 15-8 = 21h Address for bits 23-16 = 22h Address for bits 31-24 = 23h

Table 17. ALARM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Reserved	R	0000h	Reserved. Reads return 0000h.
15	ACTIVE_VDD_L_FLAG	R	0b	Active ALARM output flag for low AVDD voltage. 0b = No ALARM condition 1b = ALARM condition exists
14	ACTIVE_VDD_H_FLAG	R	0b	Active ALARM output flag for high AVDD voltage. 0b = No ALARM condition 1b = ALARM condition exists
13-12	Reserved	R	00b	Reserved. Reads return 00b.
11	ACTIVE_IN_L_FLAG	R	0b	Active ALARM output flag for high input voltage. 0b = No ALARM condition 1b = ALARM condition exists
10	ACTIVE_IN_H_FLAG	R	0b	Active ALARM output flag for low input voltage. 0b = No ALARM condition 1b = ALARM condition exists
9-8	Reserved	R	00b	Reserved. Reads return 00b.
7	TRP_VDD_L_FLAG	R	0b	Tripped ALARM output flag for low AVDD voltage. 0b = No ALARM condition 1b = ALARM condition exists
6	TRP_VDD_H_FLAG	R	0b	Tripped ALARM output flag for high AVDD voltage. 0b = No ALARM condition 1b = ALARM condition exists
5	TRP_IN_L_FLAG	R	0b	Tripped ALARM output flag for high input voltage. 0b = No ALARM condition 1b = ALARM condition exists
4	TRP_IN_H_FLAG	R	0b	Tripped ALARM output flag for low input voltage. 0b = No ALARM condition 1b = ALARM condition exists
3-1	Reserved	R	000b	Reserved. Reads return 000b.
0	OVW_ALARM	R	0b	Logical OR outputs all tripped ALARM flags. 0b = No ALARM condition 1b = ALARM condition exists

7.6.1.8 ALARM_H_TH_REG Register (address = 24h)

This register controls the hysteresis and high threshold for the input alarm.

Figure 89. ALARM_H_TH_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="8">INP_ALRM_HYST[7:0]</td><td colspan="8">Reserved</td></tr>
<tr><td colspan="8">R/W-00h</td><td colspan="8">R-00h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">INP_ALRM_HIGH_TH[15:0]</td></tr>
<tr><td colspan="16">R/W-FFFFh</td></tr>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset; -0, -1 = Condition after application reset;
-<0>, -<1> = Condition after power-on reset

Address for bits 7-0 = 24h Address for bits 15-8 = 25h Address for bits 23-16 = 26h Address for bits 31-24 = 27h

Table 18. ALARM_H_TH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	INP_ALRM_HYST[7:0]	R/W	00h	INP_ALRM_HYST[7:2]: 6-bit hysteresis value for the input ALARM. INP_ALRM_HYST[1:0] must be set to 00b.
23-16	Reserved	R	00h	Reserved. Reads return 00h.
15-0	INP_ALRM_HIGH_TH[15:0]	R/W	FFFFh	Threshold for comparison is INP_ALRM_HIGH_TH[15:0] appended with 00b.

7.6.1.9 ALARM_L_TH_REG Register (address = 28h)

This register controls the low threshold for the input alarm.

Figure 90. ALARM_L_TH_REG Register

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="16">Reserved</td></tr>
<tr><td colspan="16">R-0000h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">INP_ALRM_LOW_TH[15:0]</td></tr>
<tr><td colspan="16">R/W-0000h</td></tr>
</table>

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset; -0, -1 = Condition after application reset;
-<0>, -<1> = Condition after power-on reset

Address for bits 7-0 = 28h Address for bits 15-8 = 29h Address for bits 23-16 = 2Ah Address for bits 31-24 = 2Bh

Table 19. ALARM_L_TH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
32:16	Reserved	R	0000h	Reserved. Reads return 0000h.
15-0	INP_ALRM_LOW_TH[15:0]	R/W	0000h	Threshold for comparison is INP_ALRM_LOW_TH[15:0] appended with 00b.

8 Application and Implementation

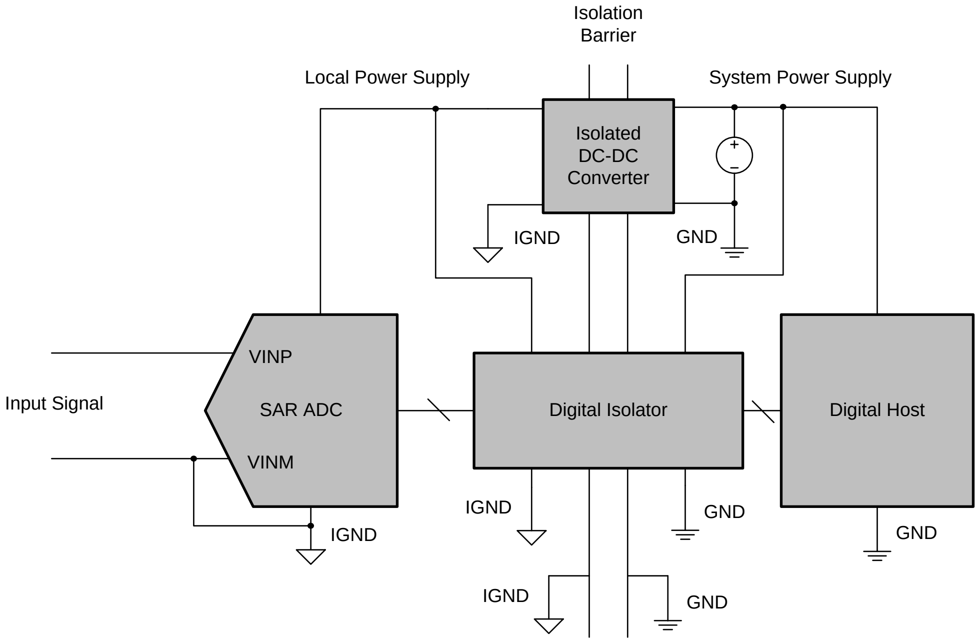
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ADS869x is a fully-integrated data acquisition (DAQ) system based on a 18-bit successive approximation (SAR) analog-to-digital converter (ADC). The device includes an integrated analog front-end (AFE) circuit to drive the inputs of the ADC and an integrated precision reference with a buffer. As such, this device does not require any additional external circuits for driving the reference or analog input pins of the ADC.

8.2 Typical Application



NOTE: The potential difference between IGND and GND can be as high as the barrier breakdown voltage (often thousands of volts).

Figure 91. 18-Bit Isolated DAQ System for High Common-Mode Rejection

8.2.1 Design Requirements

Design a 18-bit DAQ system for processing input signals up to ±12 V superimposed on large dc or ac common-mode offsets relative to the ground potential of the system main power supply. The specific performance requirements are as follows:

- Input signal: ±12-V amplitude signal of a 1-kHz frequency superimposed on a ±75-V common-mode with frequency between dc and 15 kHz
- CMRR > 100 dB over stipulated common-mode frequency range
- SNR > 91 dB
- THD < –106 dB

Typical Application (continued)

8.2.2 Detailed Design Procedure

The design uses galvanic isolation between the DAQ system inputs and main power supply to achieve extremely high CMRR, as indicated by Figure 91. The system not only tolerates large common-mode voltages beyond its absolute maximum ratings but also delivers excellent performance largely independent of common-mode amplitude and frequency (within the specified operating limits). The relevant performance characteristics are illustrated in Figure 99, Figure 93, and Figure 94.

The system performance requirements by itself can be easily satisfied by using the ADS869x. This device simplifies system design because the ADS869x eliminates the need for designing a discrete high-performance signal chain needed with most other SAR ADCs. In addition, the use of galvanic isolation has the following system design implications:

- A local floating supply is needed to power the ADS869x because the device cannot load the system main power supply
- A digital isolator is required to facilitate data transfer between the isolated ADS869x serial interface and the digital host controller

The floating power supply can be realized as an isolated transformer-based, push-pull converter followed by a rectifier and low-dropout (LDO) regulator to largely eliminate the ADC power-supply ripple by taking advantage of the high PSRR provided by most LDOs. A schematic of this design is shown in Figure 92.

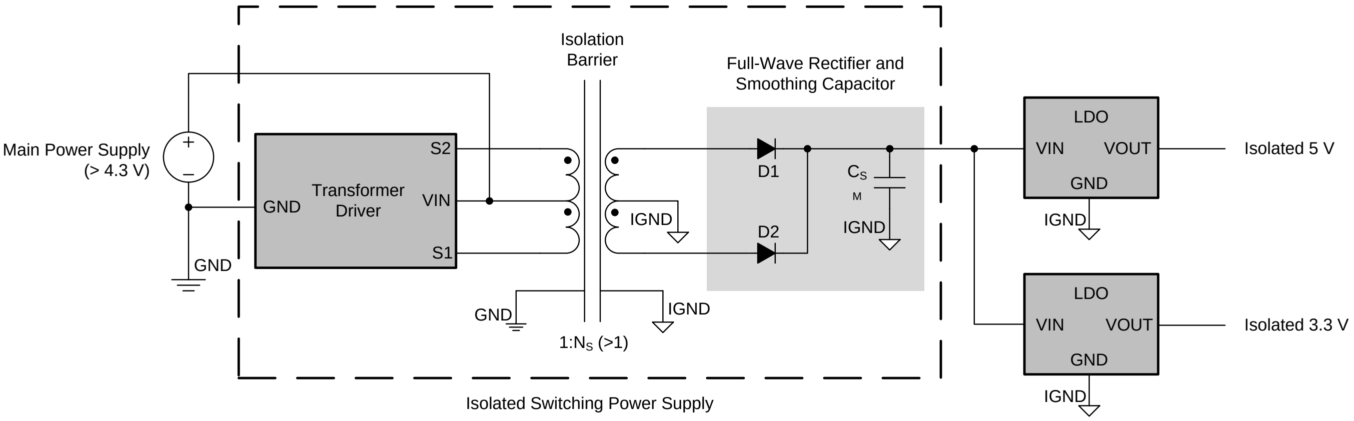


Figure 92. Isolated Power-Supply Design

Recommended components for the circuit shown in Figure 92 are given below:

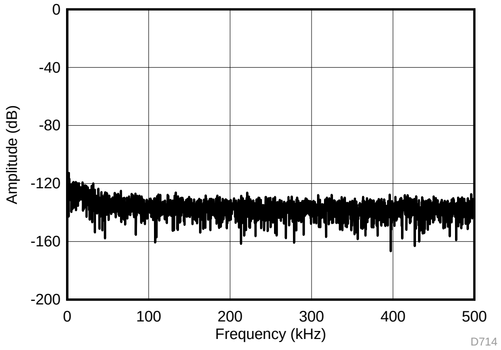
- The SN6501 transformer driver is selected for its low input voltage requirement, small form-factor, and the flexibility offered for easily adjusting the system isolation voltage rating by substituting the transformer
- A miniature printed circuit board (PCB)-mount, center-tapped transformer with a gain > 1 maintains line regulation at the LDO outputs
- Schottky rectifiers for minimal forward voltage drop
- Smoothing capacitor for sufficiently low ripple at the LDO input
- The TPS7A4901 LDOs for an ultra-low noise contribution relative to the ADS869x and high PSRR over a wide frequency range to attenuate output ripple to levels below the LDO output noise level

With regard to the digital isolator, the ISO7640FM is recommended for the following reasons:

- Supports > a 50-MHz SCLK and the required logic levels for operating the ADS869x at the full throughput
- Quad-channel device that facilitates excellent delay-matching between critical interface signals for reliable operation at high speed

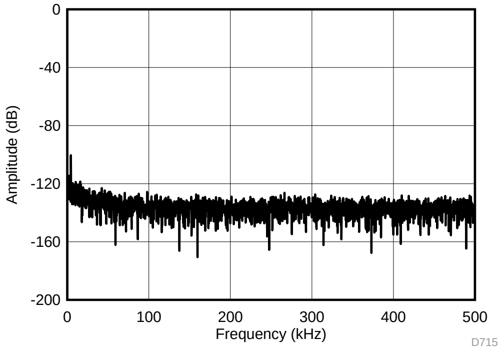
Typical Application (continued)

8.2.3 Application Curves



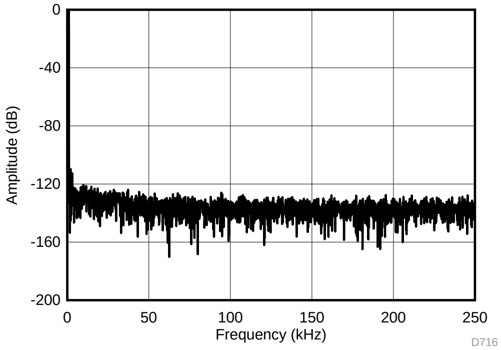
f_{SAMPLE} = 1 MSPS, V_{IN} = ±12 V, f_{IN} = 1 kHz, V_{CM} = 50 V_{DC},
SINAD = 92.2 dB, THD = –109 dB

Figure 93. FFT Plot With a DC Common-Mode at 1 MSPS



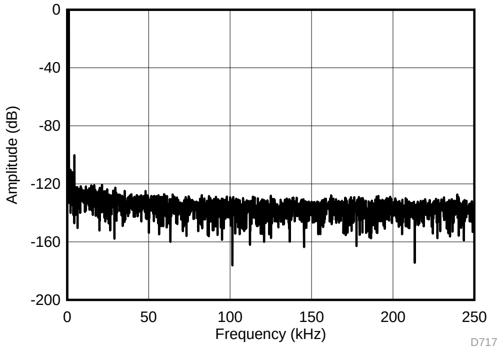
f_{SAMPLE} = 1 Msps, V_{IN} = ±12 V, f_{IN} = 1 kHz,
V_{CM} = 155 V_{PP}, SINAD = 91.5 dB, THD = –109 dB

Figure 94. FFT Plot With an AC Common-Mode at 1 MSPS



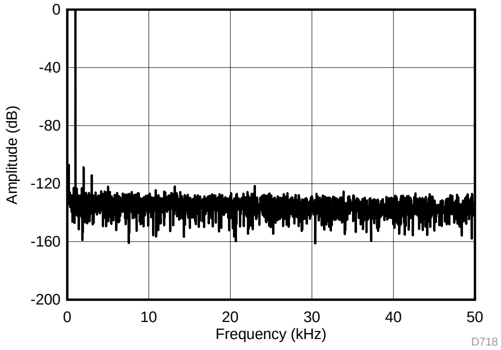
f_{SAMPLE} = 500 kSPS, V_{IN} = ±12 V, f_{IN} = 1 kHz, V_{CM} = 50 V_{DC},
SINAD = 92.3 dB, THD = –109 dB

Figure 95. FFT Plot With a DC Common-Mode at 500 kSPS



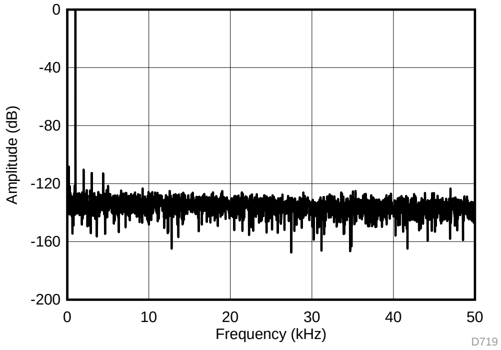
f_{SAMPLE} = 500 kSPS, V_{IN} = ±12 V, f_{IN} = 1 kHz,
V_{CM} = 155 V_{PP}, SINAD = 91.9 dB, THD = –109 dB

Figure 96. FFT Plot With an AC Common-Mode at 500 kSPS



f_{SAMPLE} = 100 kSPS, V_{IN} = ±12 V, f_{IN} = 1 kHz, V_{CM} = 50 V_{DC},
SINAD = 91.9 dB, THD = –109 dB

Figure 97. FFT Plot With a DC Common-Mode at 100 kSPS



f_{SAMPLE} = 100 kSPS, V_{IN} = ±12 V, f_{IN} = 1 kHz,
V_{CM} = 155 V_{PP}, SINAD = 91.4 dB, THD = –109 dB

Figure 98. FFT Plot With an AC Common-Mode at 100 kSPS

Typical Application (continued)

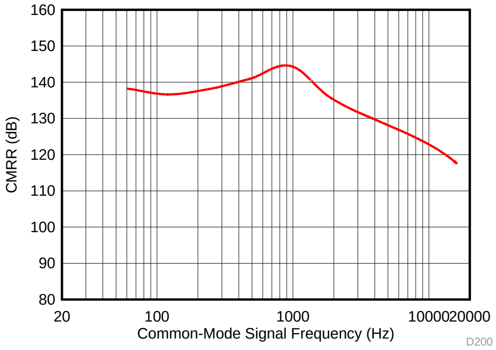


Figure 99. Common-Mode Rejection Ratio vs Frequency

9 Power Supply Recommendations

The device uses two separate power supplies: AVDD and DVDD. The internal circuits of the device operate on AVDD and DVDD is used for the digital interface. AVDD and DVDD can be independently set to any value within the permissible range.

9.1 Power Supply Decoupling

The AVDD supply pins must be decoupled with AGND by using a minimum 10-µF and 1-µF capacitor on each supply. Place the 1-µF capacitor as close to the supply pins as possible. Place a minimum 10-µF decoupling capacitor very close to the DVDD supply to provide the high-frequency digital switching current. The effect of using the decoupling capacitor is illustrated in the difference between the power-supply rejection ratio (PSRR) performance of the device. Figure 100 shows the PSRR of the device without using a decoupling capacitor. The PSRR improves when the decoupling capacitors are used, as shown in Figure 101.

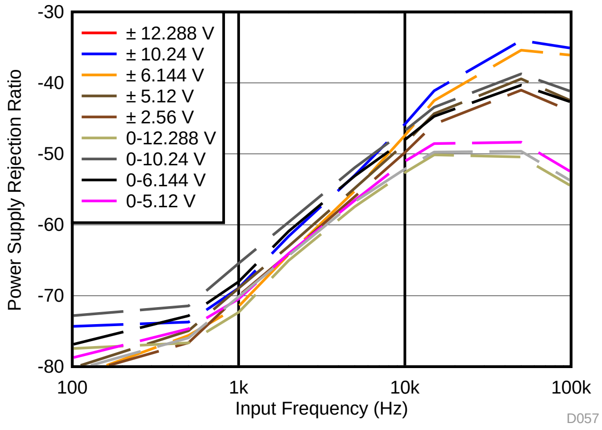


Figure 100. PSRR Without a Decoupling Capacitor

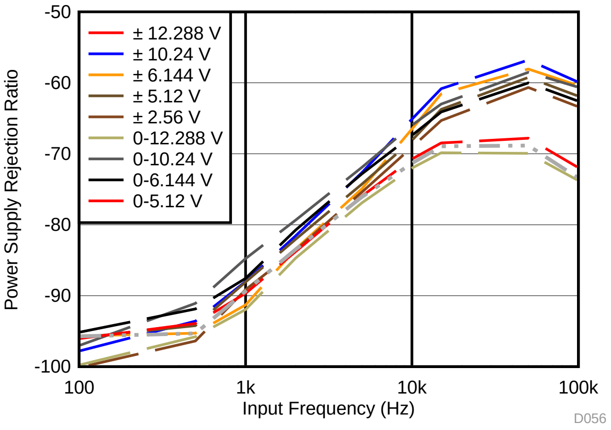


Figure 101. PSRR With a Decoupling Capacitor

9.2 Power Saving

In normal mode of operation, the device does not power down between conversions, and therefore achieves high throughput.However, the device offers two programmable low-power modes: NAP and power-down (PD) to reduce power consumption when the device is operated at lower throughput rates.

9.2.1 NAP Mode

In NAP mode, the internal blocks of the device are placed into a low-power mode to reduce the overall power consumption of the device in the ACQ state.

To enable NAP mode:

- Write 69h to register address 05h to unlock the RST_PWRCTL_REG register.
- The NAP_EN bit in the RST_PWRCTL_REG register must be set to 1b. The CONVST/$\overline{\text{CS}}$ pin must be kept high at the end of the conversion process. The device then enters NAP mode at the end of conversion and remains in NAP mode as long as the CONVST/$\overline{\text{CS}}$ pin is held high.

A falling edge on the CONVST/$\overline{\text{CS}}$ brings the device out of NAP mode; however, the host controller can initiate a new conversion (CONVST/$\overline{\text{CS}}$ rising edge) only after the t_{NAP_WKUP} time has elapsed (see the *Timing Requirements: Asynchronous Reset* table).

Power Saving (continued)

9.2.2 Power-Down (PD) Mode

The device also features a deep power-down mode (PD) to reduce the power consumption at very low throughput rates.

The following steps must be taken to enter PD mode:

1. Write 69h to register address 05h to unlock the RST_PWRCTL_REG register.
2. Set the PWRDN bit in the RST_PWRCTL_REG register to 1b. The device enters PD mode on the rising edge of the CONVST/$\overline{\text{CS}}$ signal.

In PD mode, all analog blocks within the device are powered down; however, the interface remains active and the register contents are also retained. The RVS pin is high, indicating that the device is ready to receive the next command.

In order to exit PD mode:

1. Clear the PWRDN bit in the RST_PWRCTL_REG register to 0b.
2. The RVS pin goes high, indicating that the device has started coming out of PD mode. However, the host controller must wait for the t_{PWRUP} time (see the *Timing Requirements: Asynchronous Reset* table) to elapse before initiating a new conversion.

10 Layout

10.1 Layout Guidelines

Figure 102 illustrates a PCB layout example for the ADS869x.

- Partition the PCB into analog and digital sections. Care must be taken to ensure that the analog signals are kept away from the digital lines. This layout helps keep the analog input and reference input signals away from the digital noise. In this layout example, the analog input and reference signals are routed on the lower side of the board and the digital connections are routed on the top side of the board.
- Using a single dedicated ground plane is strongly encouraged.
- Power sources to the ADS869x must be clean and well-bypassed. Using a 1-µF, X7R-grade, 0603-size ceramic capacitor with at least a 10-V rating in close proximity to the analog (AVDD) supply pins is recommended. For decoupling the digital supply pin (DVDD), a 1-µF, X7R-grade, 0603-size ceramic capacitor with at least a 10-V rating is recommended. Placing vias between the AVDD, DVDD pins and the bypass capacitors must be avoided. All ground pins must be connected to the ground plane using short, low-impedance paths.
- There are two decoupling capacitors used for the REFCAP pin. The first is a small, 1-µF, 0603-size ceramic capacitor placed close to the device pins for decoupling the high-frequency signals and the second is a 10-µF, 0805-size ceramic capacitor to provide the charge required by the reference circuit of the device. A capacitor with an ESR less than 0.2 Ω is recommended for the 10-µF capacitor. Both of these capacitors must be directly connected to the device pins without any vias between the pins and capacitors.
- The REFIO pin also must be decoupled with a minimum of 4.7-µF ceramic capacitor if the internal reference of the device is used. The capacitor must be placed close to the device pins.

10.2 Layout Example

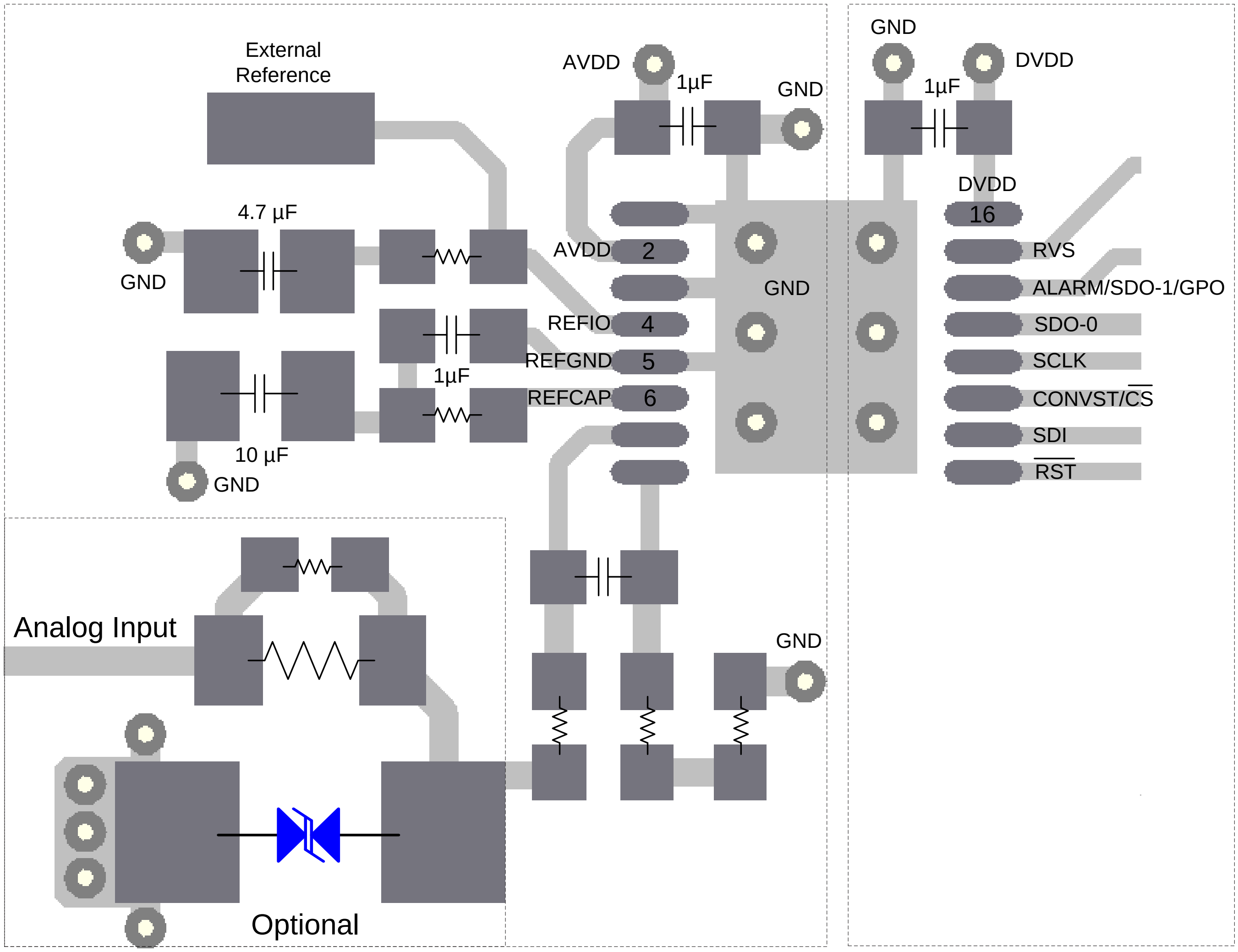


Figure 102. Board Layout for the ADS869x

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档如下：

- 《OPA320 具有关断功能的高精度、20MHz、0.9pA、低噪声、RRIO、CMOS 运算放大器》（文献编号：SBOS513）
- 《SN6501 适用于隔离式电源的变压器驱动器》（文献编号：SLLSEA0）
- 《TPS7A49 36V、150mA 超低噪声正线性稳压器》（文献编号：SBVS121）
- 《ISO764xFM 低功耗四通道数字隔离器》（文献编号：SLLSE89）
- 《AN-2029 操作和处理建议》应用报告（文献编号：SNOA550）

11.2 相关链接

以下表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **20.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
ADS8691	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ADS8695	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ADS8699	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.3 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8691IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8691	Samples
ADS8691IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8691	Samples
ADS8691IRUMR	PREVIEW	WQFN	RUM	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8691	
ADS8691IRUMT	PREVIEW	WQFN	RUM	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8691	
ADS8695IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8695	Samples
ADS8695IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8695	Samples
ADS8695IRUMR	PREVIEW	WQFN	RUM	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8695	
ADS8695IRUMT	PREVIEW	WQFN	RUM	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8695	
ADS8699IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8699	Samples
ADS8699IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8699	Samples
ADS8699IRUMR	PREVIEW	WQFN	RUM	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8699	
ADS8699IRUMT	PREVIEW	WQFN	RUM	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8699	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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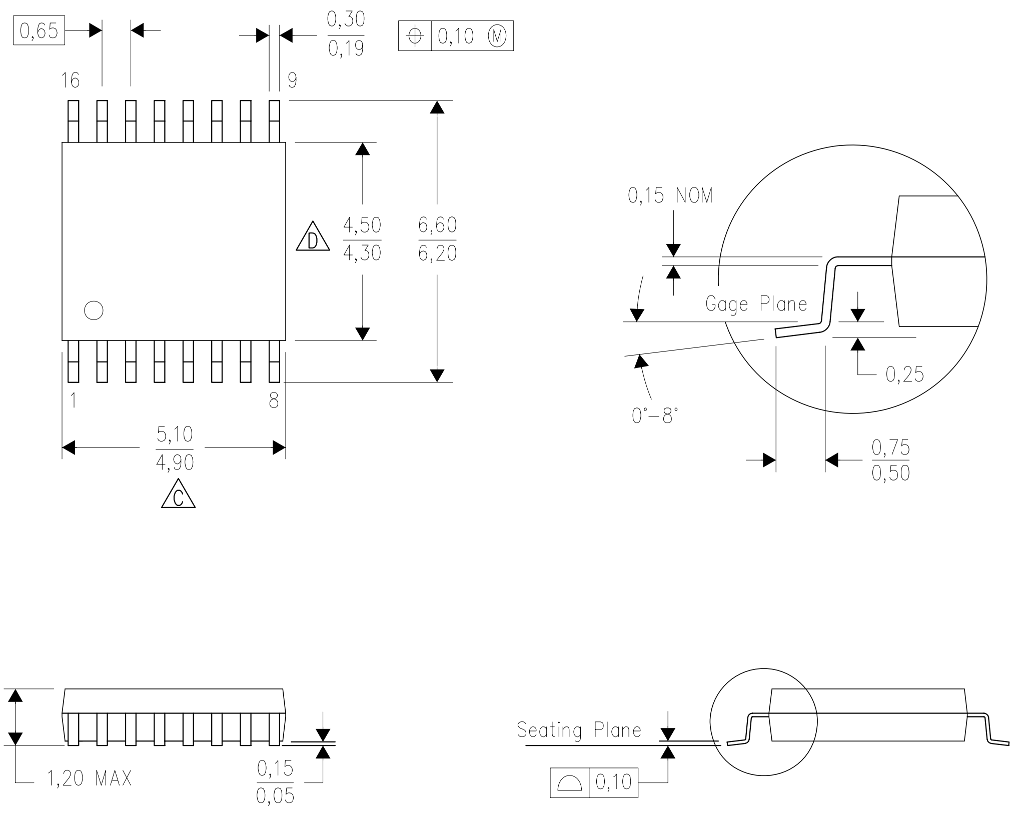
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.

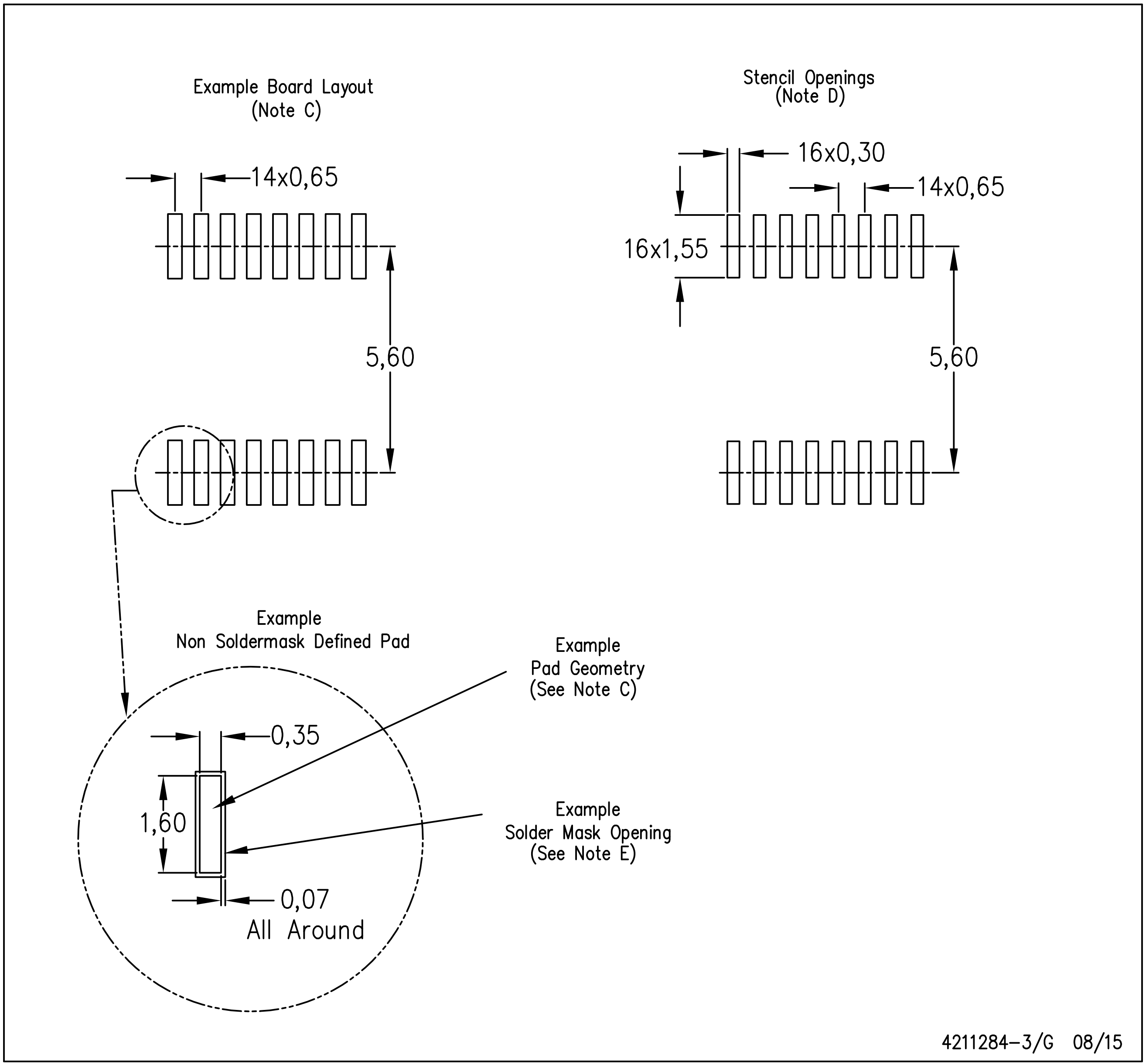
B. This drawing is subject to change without notice.

△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

△D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

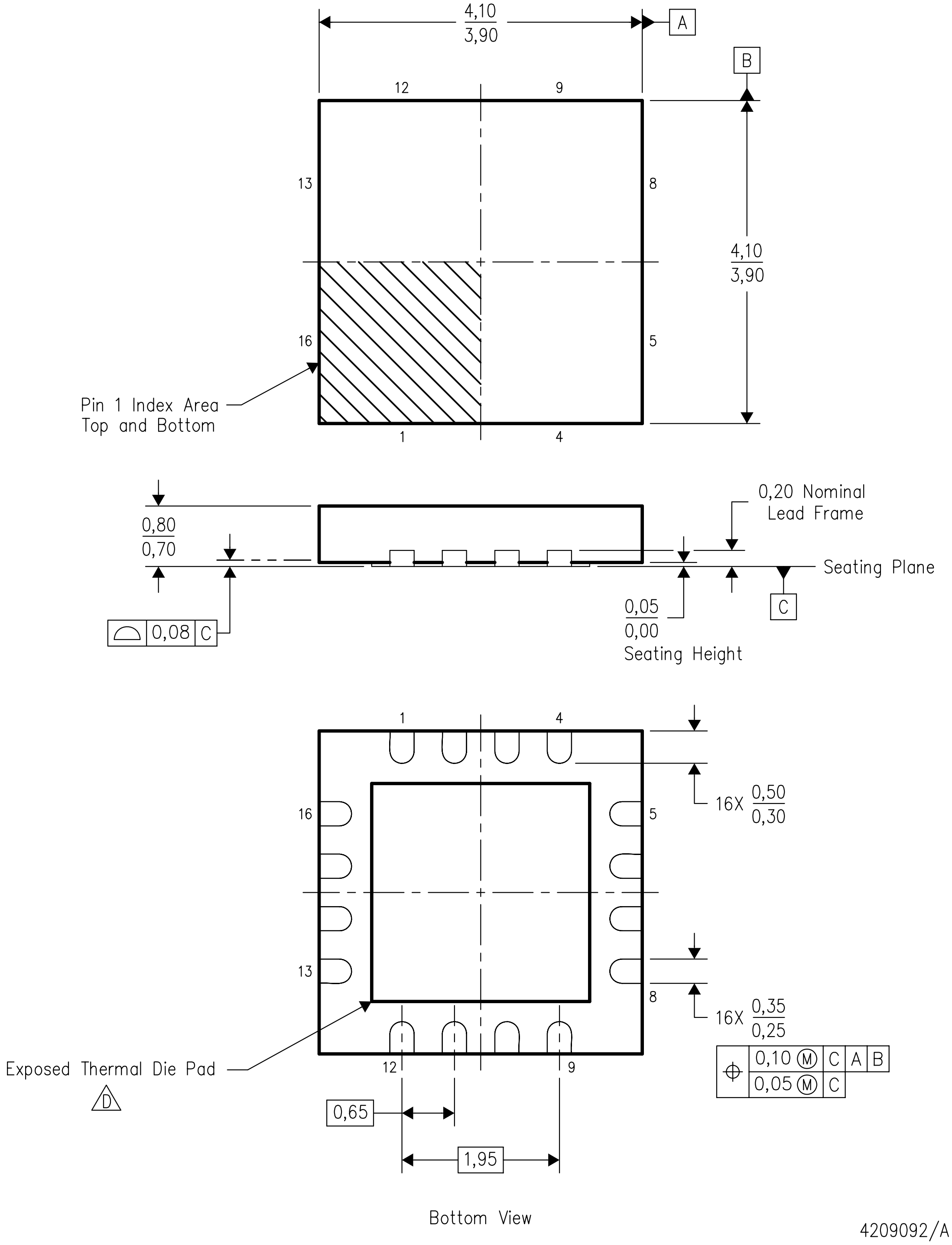
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RUM (S-PQFP-N16) PLASTIC QUAD FLATPACK



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NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Package complies to JEDEC MO–220 variation WGGC–3.

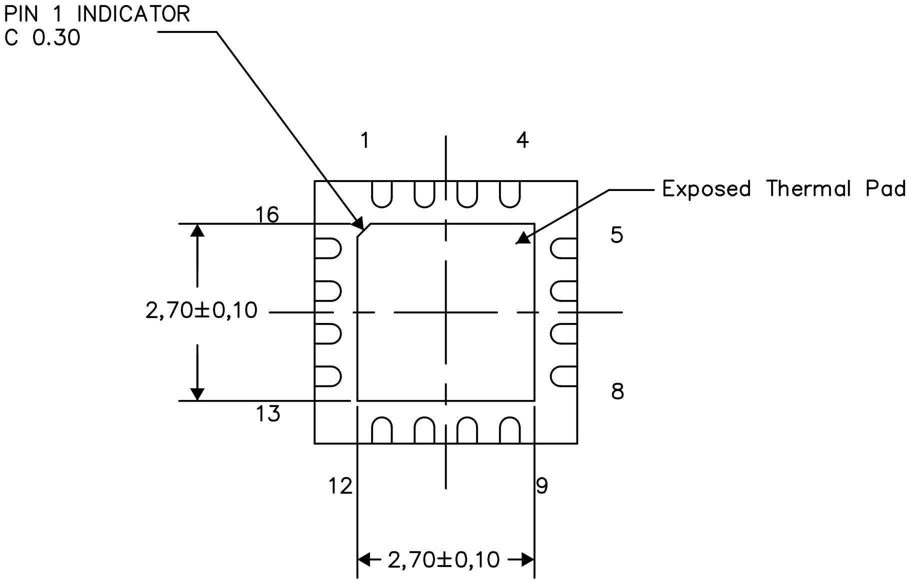
RUM (S-PWQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



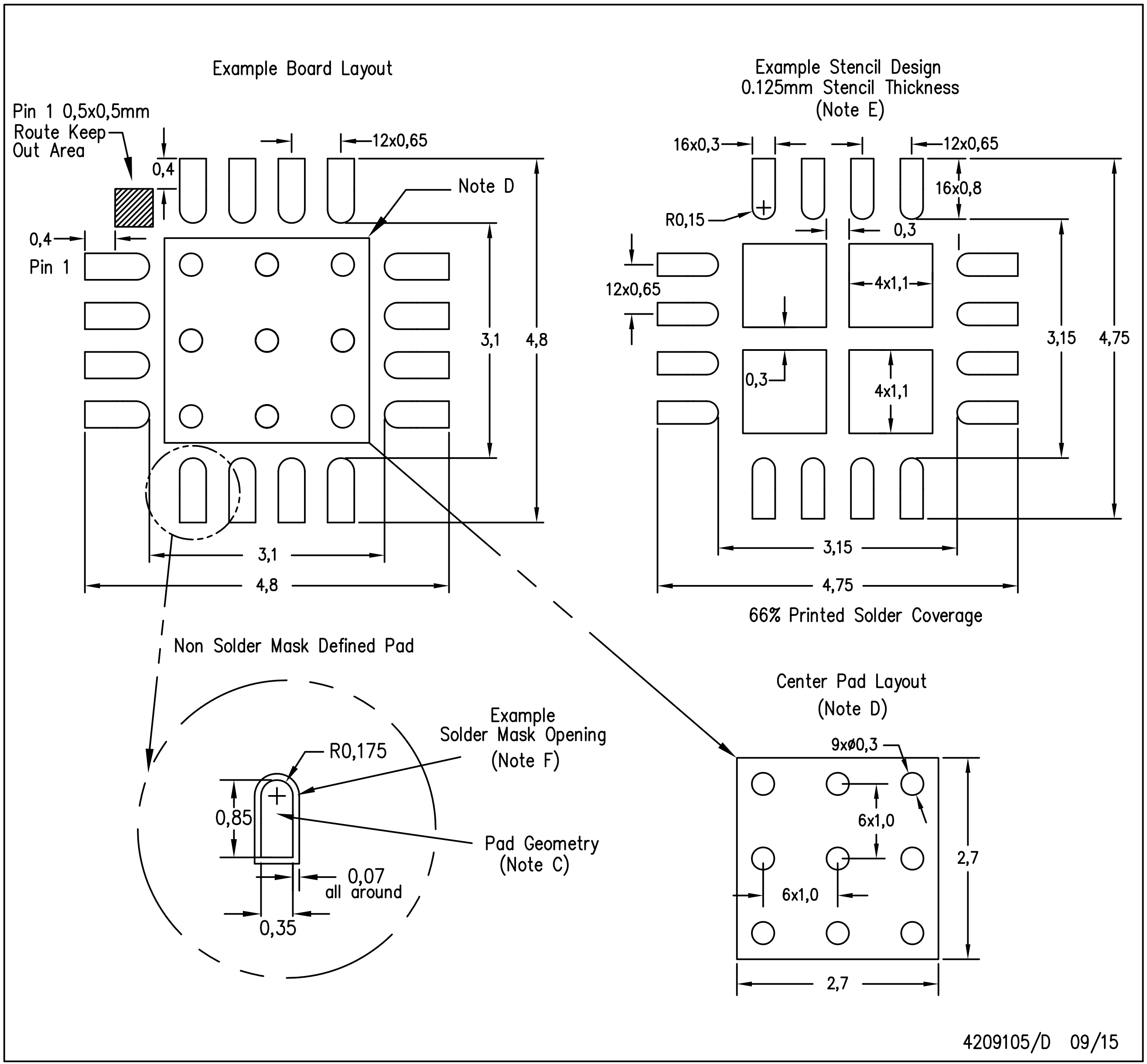
Bottom View

Exposed Thermal Pad Dimensions

4209093-2/F 09/15

NOTES: All linear dimensions are in millimeters

RUM (S-PWQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

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