

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

[illegible]

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance current output/serial input, 16 bit, digital to analog converter (DAC) microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/12662</u>	-	<u>01</u>	<u>X</u>	<u>B</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01 <u>1</u> /	AD5543	Current output/serial input, 16 bit, digital to analog converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	8	MO-187-AA	Small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1/ The device contains 1040 transistors. The die size measures 55 mil x 73 mil or 4,015 square mil.

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1.3 Absolute maximum ratings. 2/

Positive supply power input (V_{DD}) to analog and digital ground (GND)	-0.3 V to +8 V
DAC reference input (V_{REF}) to GND	-18 V to +18 V
Logic inputs to GND	-0.3 V to +8 V
Voltage at DAC current output ($V(I_{OUTX})$) to GND	-0.3 V, $V_{DD} + 0.3$ V
Input current to any pin except supplies	± 50 mA
Power dissipation (P_D)	$(T_{Jmax} - T_A) / \theta_{JA}$ and see table I.
Maximum junction temperature range (T_J)	150°C
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature:	
Vapor phase, 60 seconds	215°C
Infrared, 15 seconds	220°C

1.4 Recommended operating conditions. 3/

Supply voltage range (V_{DD})	5 V
Operating free-air temperature range (T_A)	-55°C to +125°C

1.5 Thermal characteristics.

Thermal resistance, junction to ambient (θ_{JA})	150°C/W
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- 2/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at <http://www.jedec.org>)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Timing waveforms. The timing waveforms shall be as shown in figure 3.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Static performance <u>3/</u>							
Resolution	N	1 LSB = V _{REF} / 2 ¹⁶ = 153 μV when V _{REF} = 10 V	-55°C to +125°C	01		16	Bits
Relative accuracy	INL		-55°C to +125°C	01		±3	LSB
Differential nonlinearity	DNL	Monotonic	-55°C to +125°C	01		-1/+2	LSB
Output leakage current	I _{OUT}	Data = 0x0000	+25°C	01		10	nA
			+125°C			20	
Full scale gain error	G _{FSE}	Data = 0xFFFF	+25°C	01	±1/±4 typical maximum		mV
Full scale temperature coefficient	TCV _{FS}	<u>4/</u>	+25°C	01	1 typical		ppm/ °C
Reference input							
VREF range	V _{REF}		-55°C to +125°C	01	-15	+15	V
Input resistance	R _{REF}		+25°C	01	5 typical		kΩ <u>5/</u>
Input capacitance <u>4/</u>	C _{REF}		+25°C	01	5 typical		pF
Analog output							
Output current	I _{OUT}	Data = 0xFFFF	+25°C	01	2 typical		mA
Output capacitance <u>4/</u>	C _{OUT}	Code dependent	+25°C	01	200 typical		pF
Logic inputs and output							
Logic input low voltage	V _{IL}		-55°C to +125°C	01		0.8	V
Logic input high voltage	V _{IH}		-55°C to +125°C	01	2.4		V
Input leakage current	I _{IL}		-55°C to +125°C	01		10	μA
Input capacitance <u>4/</u>	C _{IL}		-55°C to +125°C	01		10	pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Interface timing <u>4/ 6/</u>							
Clock input frequency	f _{CLK}		-55°C to +125°C	01		50	MHz
Clock width high	t _{CH}		-55°C to +125°C	01	10		ns
Clock width low	t _{CL}		-55°C to +125°C	01	10		ns
$\overline{\text{CS}}$ to clock setup	t _{CSS}		-55°C to +125°C	01	0		ns
Clock to $\overline{\text{CS}}$ hold	t _{CSH}		-55°C to +125°C	01	10		ns
Data setup	t _{DS}		-55°C to +125°C	01	5		ns
Data hold	t _{DH}		-55°C to +125°C	01	10		ns
Supply characteristics							
Power supply range	V _{DD} RANGE		-55°C to +125°C	01	4.5	5.5	V
Positive supply current	I _{DD}	Logic inputs = 0 V	-55°C to +125°C	01		10	μA
Power dissipation	PD	Logic inputs = 0 V	-55°C to +125°C	01		0.055	mW
Power supply sensitivity	PSS	ΔV _{DD} = ±5%	-55°C to +125°C	01		0.006	%/%
AC characteristics <u>6/</u>							
Output voltage settling time	t _S	To ±0.1% of full scale, data = 0x0000 to 0xFFFF to 0x0000	+25°C	01	0.5 typical		μs
Reference multiplying bandwidth	BW	V _{REF} = 100 mV rms, data = 0xFFFF	+25°C	01	6.6 typical		MHz
DAC glitch impulse	Q	V _{REF} = 0 V, data = 0x7FFF to 0x8000	-55°C to +125°C	01		7	nV- sec
Feedthrough error	V _{OUT} / V _{REF}	Data = 0x0000, V _{REF} = 10 mV rms, same channel	-55°C to +125°C	01		-83	dB

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
AC characteristics <u>6/</u>							
Digital feedthrough	Q	C _S = 1 and f _{CLK} = 1 MHz	-55°C to +125°C	01		7	nV-sec
Total harmonic distortion	THD	V _{REF} = 5 Vpp, data = 0xFFFF, f = 1 kHz	+25°C	01	-103 typical		dB
Output spot noise voltage	e _N	f = 1 kHz, BW = 1 Hz	-55°C to +125°C	01	12		nV / $\sqrt{\text{Hz}}$

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Unless otherwise specified, $V_{DD} = 5$ V $\pm 10\%$, $V_{SS} = 0$ V, $I_{OUT} =$ virtual GND, GND = 0 V, $V_{REF} = 10$ V, and $T_A =$ full temperature range.
- 3/ All static performance tests (except I_{OUT}) are performed in a closed loop system using an external precision OP177 current to voltage amplifier. The R_{FB} terminal is tied to the amplifier output. The +INPUT operational amplifier is grounded, and the DAC I_{OUT} is tied to the –INPUT operational amplifier. Typical values represent average readings measured at 25°C.
- 4/ These parameters are guaranteed by design and are not subject to production testing.
- 5/ All ac characteristic tests are performed in a closed loop system using an AD8038 current to voltage (I to V) converter amplifier except for total harmonic distortion (THD) where an AD8065 was used.
- 6/ All input control signals are specified with $t_R = t_F = 2.5$ ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

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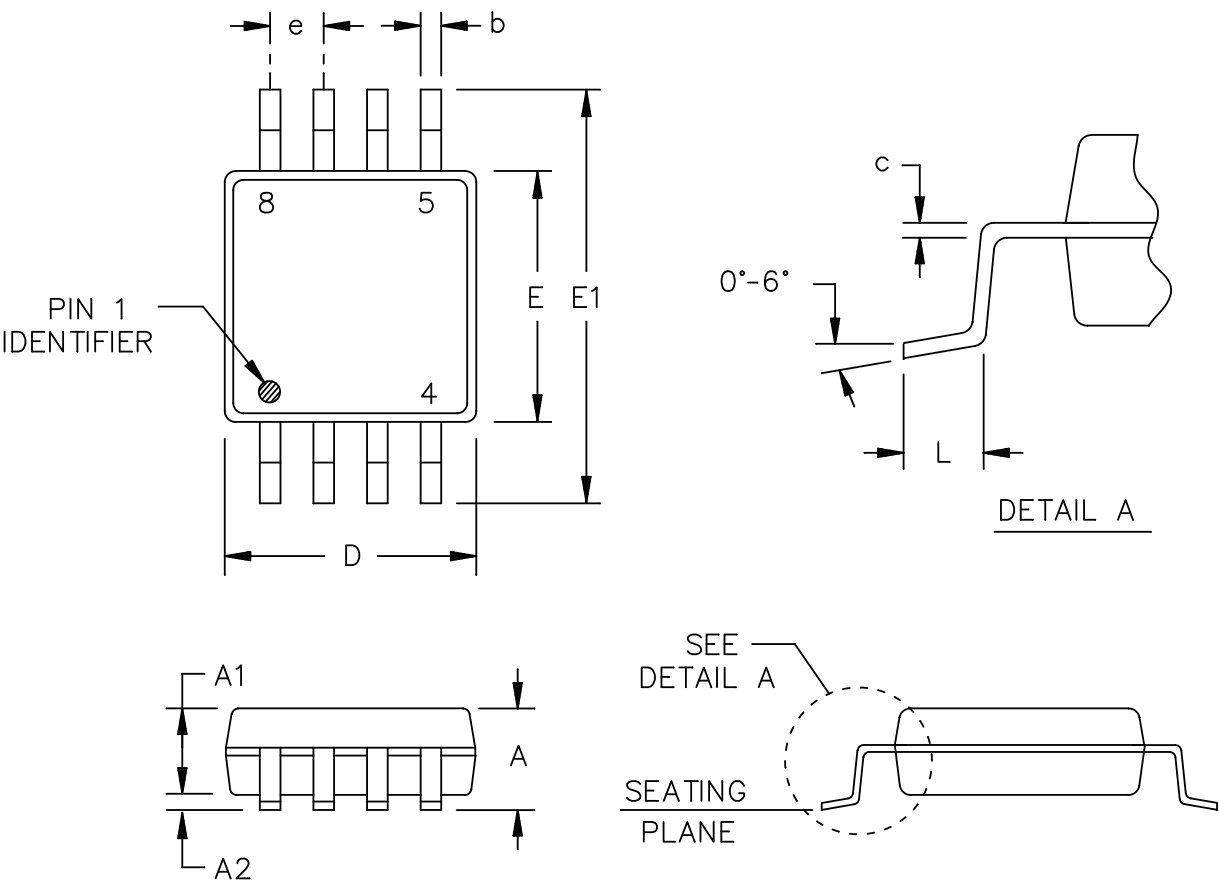


FIGURE 1. Case outline.

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Case X

Symbol	Dimensions					
	Inches			Millimeters		
	Min	Med	Max	Min	Med	Max
A	---	---	.043	---	--	1.10
A1	.029	.033	.037	0.75	0.85	0.95
A2	.001	0.10 coplanarity	.005	0.05	0.10 coplanarity	0.15
b	.009	---	.015	0.25	---	0.40
c	.003	---	.009	0.09	---	0.23
D	.110	.118	.125	2.80	3.00	3.20
E	.110	.118	.125	2.80	3.00	3.20
E1	.183	.192	.202	4.65	4.90	5.15
e	.025 BSC			0.65 BSC		
L	.015	.021	.031	0.40	0.55	0.80

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MO-187-AA.

FIGURE 1. Case outline - Continued.

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Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	CLK	Clock input. Positive edge triggered, clocks data into shift register.
2	SDI	Serial register input. Data loads directly into the shift register MSB first. Extra leading bits are ignored.
3	RFB	Internal matching feedback resistor. This pin connects to an external operational amplifier for voltage output.
4	VREF	DAC reference input pin. Establishes DAC full scale voltage. Constant input resistance versus code.
5	IOUT	DAC current output. This pin connects to the inverting terminal of the external precision current to voltage operational amplifier for voltage output.
6	GND	Analog and digital ground.
7	VDD	Positive power supply input. Specified range of operation at $5\text{ V} \pm 10\%$.
8	$\overline{\text{CS}}$	Chip select. Active low digital input. Transfers shift register data to DAC register on rising edge.

FIGURE 2. Terminal connections.

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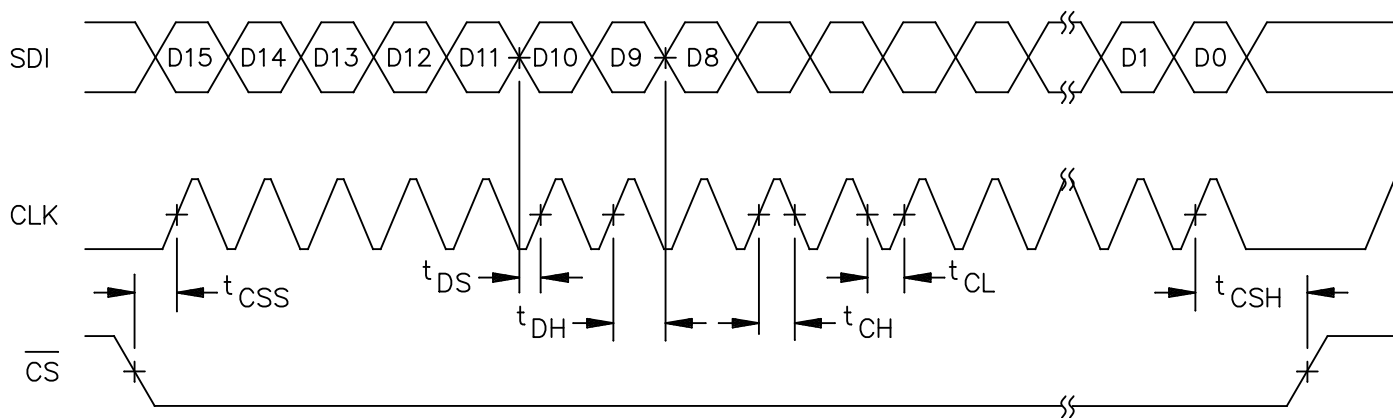


FIGURE 3. Timing waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1</u> /	Device manufacturer CAGE code	Vendor part number <u>2</u> /
V62/12662-01XB	24355	AD5543SRMZ-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ Z = RoHS complaint part.

CAGE code

24355

Source of supply

Analog Devices
Route 1 Industrial Park
P.O. Box 9106
Norwood, MA 02062
Point of contact: Raheen Business Park
Limerick, Ireland

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