Enhancement Mode GaN FETs and ICs Visual Characterization Guide

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A detailed description of the EPC enhancement mode transistors and integrated circuits physical characteristics is given including the visual criteria all devices must meet before they are released for shipment to customers. This article, used in conjunction with the two companion articles, "Assembling eGaN FETs"[1], and "EPC GaN Transistor Parametric Characterization Guide"[2], gives the user a set of tools to develop circuits and systems that take advantage of the enhancement mode GaN FET's and IC's advanced form factor and consequent unprecedented performance potential.

OVERVIEW OF GALLIUM NITRIDE (GaN) TECHNOLOGY

In June 2009 Efficient Power Conversion Corporation (EPC) introduced the first enhancement mode gallium nitride on silicon power transistors designed specifically as power MOSFET replacements. These products were developed to be produced in high volume at low cost using standard silicon manufacturing technology and facilities. For more information about EPC's GaN technology, go to www.epc-co.com.

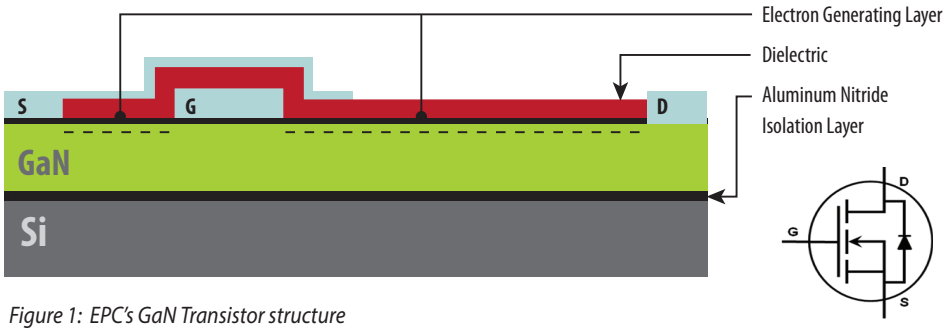


Figure 1: EPC's GaN Transistor structure

STRUCTURE

A device's cost effectiveness starts with leveraging existing production infrastructure. EPC's process begins with silicon wafers. A thin layer of Aluminum Nitride (AlN) is grown on the Silicon to isolate the device structure from the substrate. The isolation between the substrate and the active device, for product with voltage ratings 200 V and below, is over 300 V. On top of this AlN, a thick layer of highly resistive GaN is grown. This layer provides a foundation on which to build the active transistor. An electron generating material comprised of Aluminum, Gallium, and Nitrogen (AlGaN) is applied on top of the GaN. This layer creates an abundance of free electrons just below it. Further processing forms a depletion region under the gate. To enhance the transistor, a positive voltage is applied to the gate in a similar manner to turning on an n-channel, enhancement mode power MOSFET. A cross section of this structure, repeated many times to form a complete power device, is depicted in figure 1. The end result is a fundamentally simple, cost effective solution for power switching[3]. EPC's GaN transistors are lateral devices with all three terminals: gate, drain, and source, on the top side of the chip. The active device is isolated from the substrate and fully encapsulated by passivation layers. Generally, EPC devices have three layers of metal used to connect the active device to the outside world (fig 2). The top metal layer is then used as a foundation for solder bumps as shown in Figure 3. This configuration allows EPC's GaN transistors to eliminate unnecessary elements of traditional power MOSFET packaging that contribute to higher inductance, thermal and electrical resistance, higher costs, and compromised reliability.

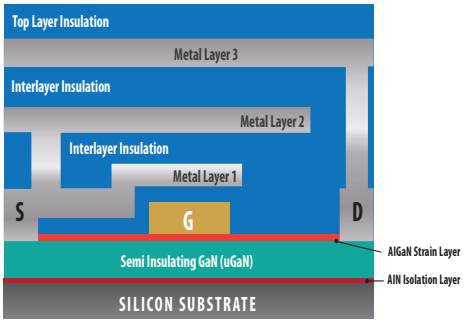


Figure 2: Device construction

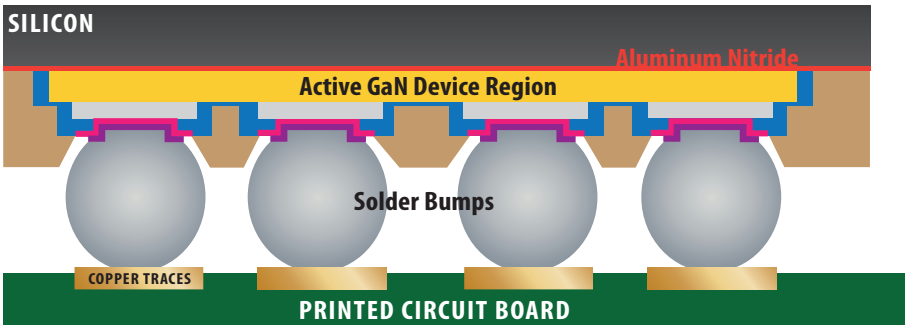


Figure 3: Flip Chip

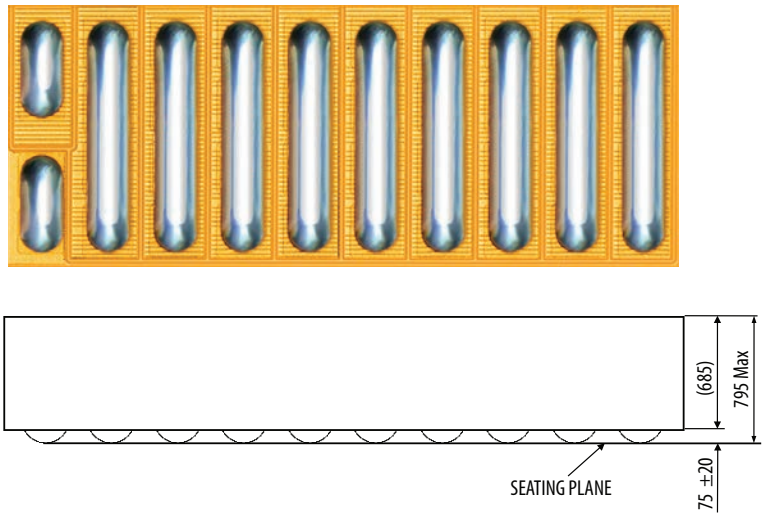
A VISUAL TOUR

Table 2 shows the top and side view of example EPC GaN transistor and integrated circuit part numbers. Solder bars or solder balls are used to make reliable connections directly to a printed circuit board. A polyimide coating on top of multiple silicon dioxide and silicon nitride layers are used to seal the active device from the outside environment.

TABLE 1 Picture of Die Front Side and Side View Representation in µm Units (Front side pictures and drawings are to scale with respect to each other)

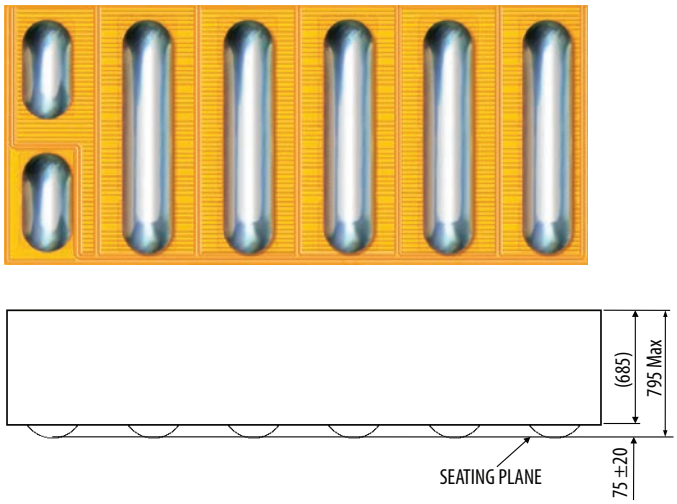
EPC Die Part Number:
EPC2001C, EPC2015C

Max Die Size (µm):
4135 x 1662



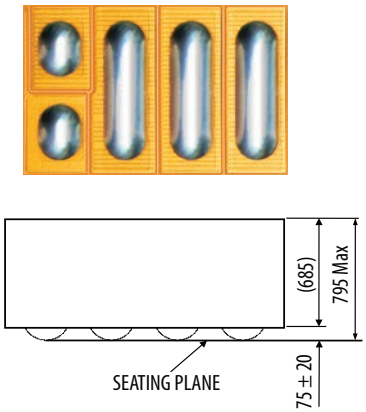
EPC Die Part Number:
EPC2010C

Max Die Size (µm):
3584 x 1662



EPC Die Part Number:
EPC2007C, EPC2014C

Max Die Size (µm):
1732 x 1117



EPC Die Part Number:
EPC2012C

Max Die Size (µm):
1741 x 949

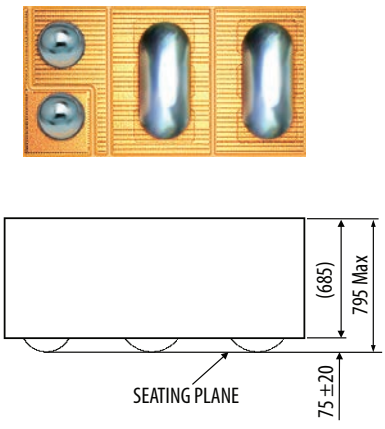
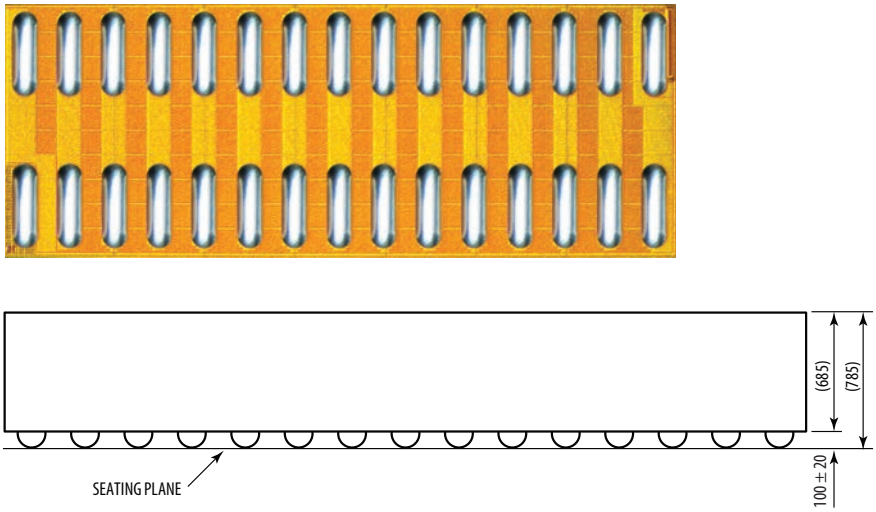


TABLE 1, continued: Picture of Die Front Side and Side View Representation in µm Units (Front side pictures and drawings are to scale with respect to each other)

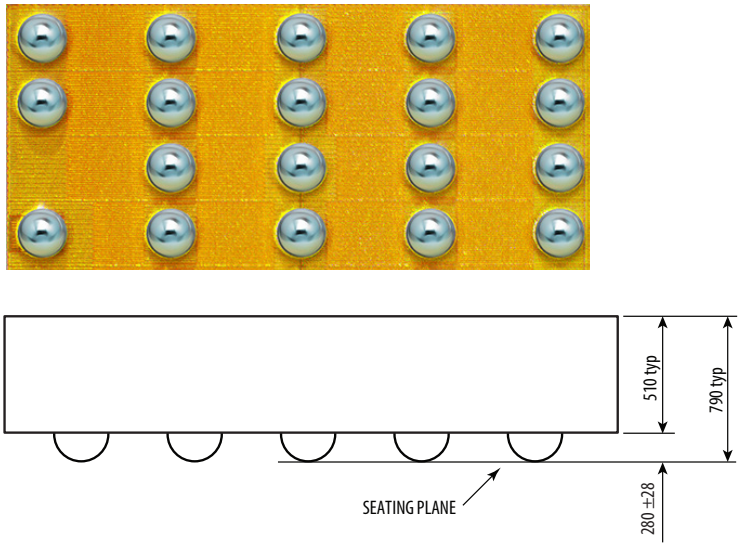
EPC Die Part Number:
EPC2020, EPC2021, EPC2022, EPC2023, EPC2024

Max Die Size (µm):
6080 x 2330



EPC Die Part Number:
EPC2029, EPC2030, EPC2031, EPC2032, EPC2033, EPC2034

Max Die Size (µm):
4630 x 2630



EPC Die Part Number:
EPC2100, EPC2101, EPV2105

Max Die Size (µm):
6080 x 2330

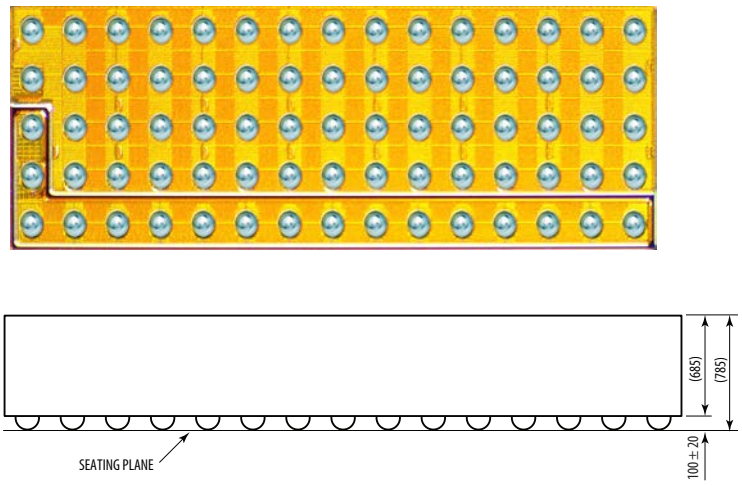
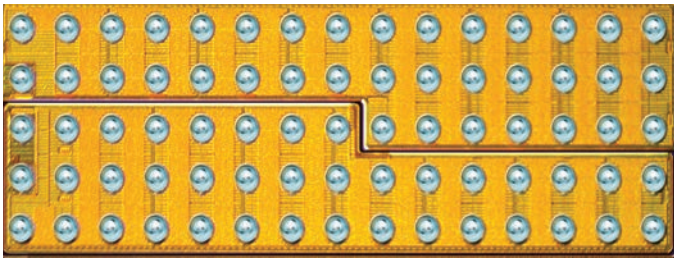
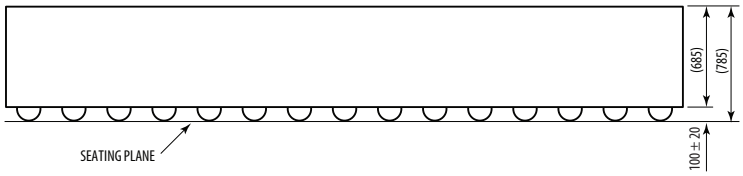


TABLE 1, continued: Picture of Die Front Side and Side View Representation in µm Units (Front side pictures and drawings are to scale with respect to each other)

EPC Die Part Number:
EPC2102, EPC2103, EPC2104

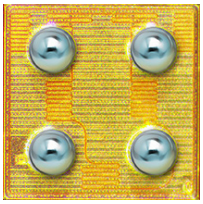
Max Die Size (µm):
6080 x 2330

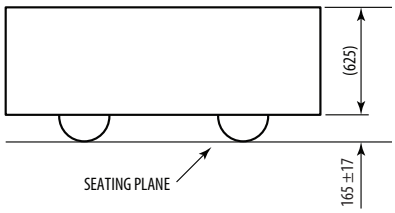




EPC Die Part Number:
EPC2035, EPC2036,
EPC2037, EPC2038

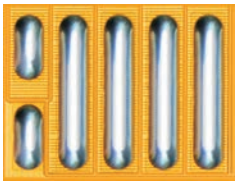
Max Die Size (µm):
930 x 930

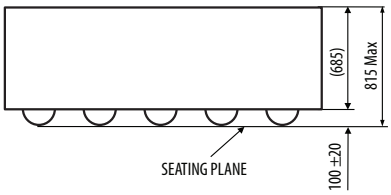




EPC Die Part Number:
EPC2016

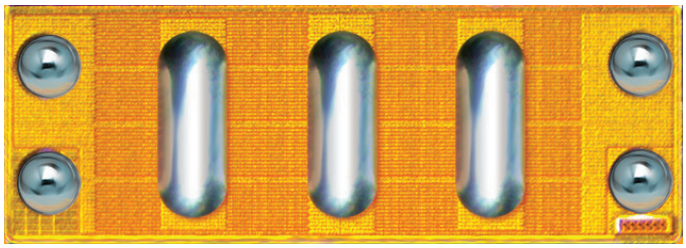
Max Die Size (µm):
2136 x 1662





EPC Die Part Number:
EPC2019

Max Die Size (µm):
2796 x 980



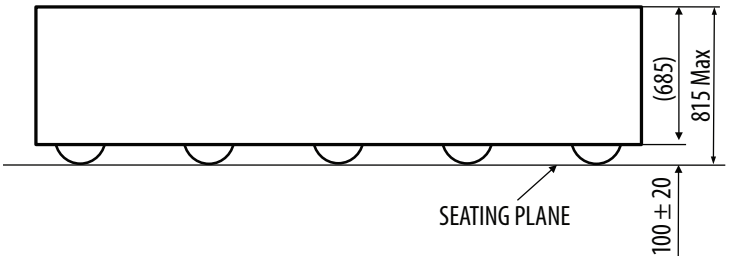
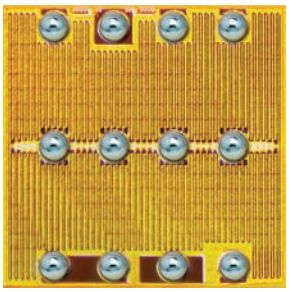
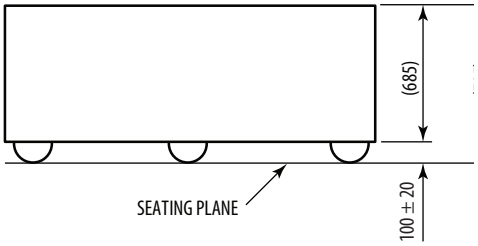


TABLE 1, continued: Picture of Die Front Side and Side View Representation in µm Units (Front side pictures and drawings are to scale with respect to each other)

EPC Die Part Number:
EPC2025

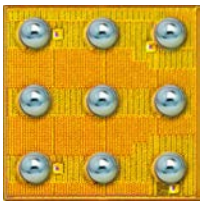
Max Die Size (µm):
1980 x 1980

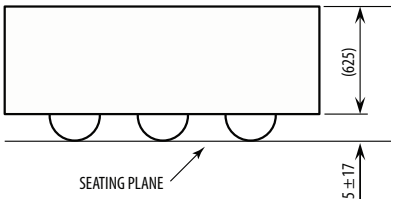




EPC Die Part Number:
EPC2039

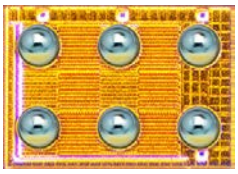
Max Die Size (µm):
1380 x 1380

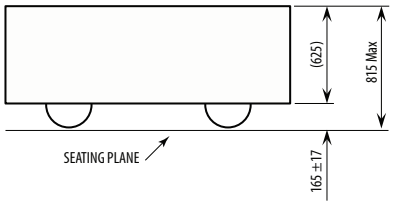




EPC Die Part Number:
EPC2040

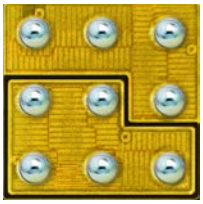
Max Die Size (µm):
880 x 1230

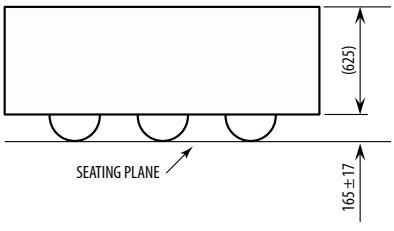




EPC Die Part Number:
EPC2106

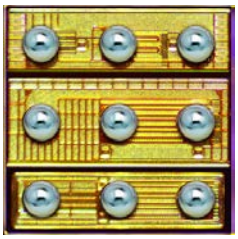
Max Die Size (µm):
1380 x 1380

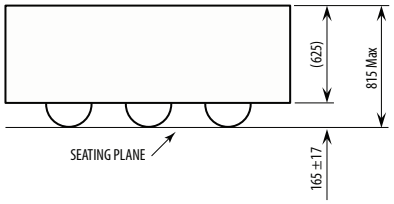




EPC Die Part Number:
EPC2107, EPC2108

Max Die Size (µm):
1380 x 1380





EPC designed these devices such that they are quite robust. In figure 4 are some examples of devices that were intentionally tested after extreme mechanical abuse.

Figure 4a, b, and c: EPC transistors with extreme mechanical damage successfully completed long term reliability testing. It should be noted that the substrate is not electrically active with respect to the device.

Fig 4c: EPC1001 part (above) passed 1000 Cycle TC -40˚C to 125˚C . Die width ~1900µm Back side chip >250µm

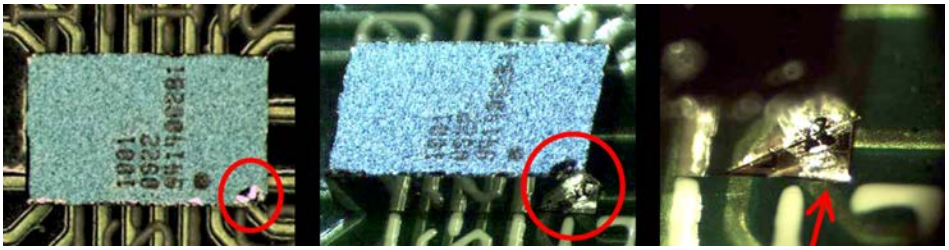


Fig 4a: Visual reject part shown in pictures above – EPC1001 part above passed 1000Hr HTRB 100 V bias 125˚C. Back side chip extends down to the front of the chip. ***Far right:*** *(area indicated with arrow) Unsupported chip structure hanging out over corner passed 1000Hr HTRB.*

Fig 4b: Visual reject part shown in pictures above – EPC1001 part with severe corner chip. Back side chip extends all the way through the chip. Die was still functioning in application. Die is shown post dismount from PCB board.

The edge protection structure reduces the risk of damage to the active portion of the device. Figure 5 is a set of microscope images of the typical edge structures and, for clarity, the original design plots are also shown to the left. Care should be taken during assembly such that chips or cracks do not go beyond the two dummy metal rings.

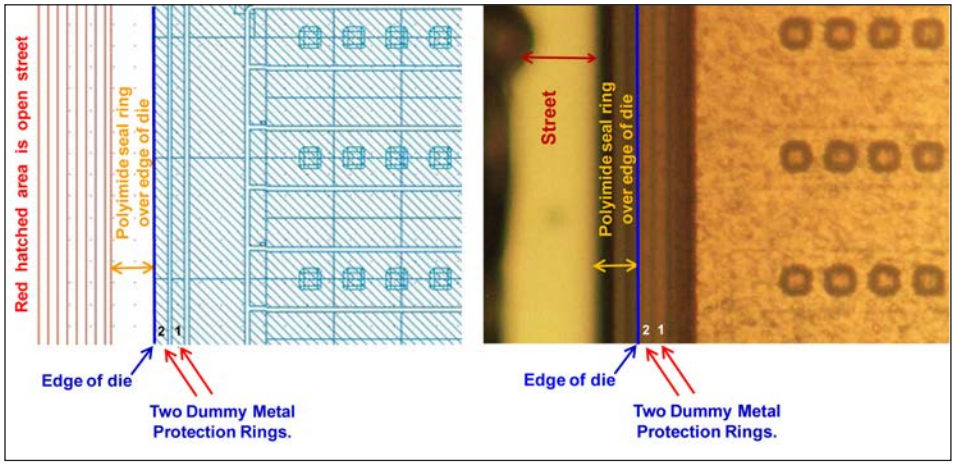


Fig 5: EPC's die top surface is designed to reduce the probability that chips will intrude into the active portion of the device. Pictured is the edge structure which includes two dummy metal rings and a polyimide coating.

SHIPMENT CRITERIA

Prior to shipment, 100% of EPC devices are electrically tested and visually inspected. Tables 3a and 3b show a summary of the visual Acceptance/Rejection criteria used as of the date of this writing. Tables 4a and 4b, over the following pages, contain several examples of both good and bad die measured against these criteria.

Table 2a: Front Side Visual Criteria

Die Front Side Visual Inspection Category	Reject Criteria
Amount of remaining street	Amount of remaining street can be zero providing no chip / crack is beyond second (outer) metal dummy ring
Chips / Cracks	Chip / crack is beyond second (outer, #2) metal dummy ring
Damaged Solder Bumps	Solder drag or displacement >50% of original distance between bumps; defect which reduces bump height by 30% of original height
Foreign material	Foreign material linking any two bumps
Contamination /defect / metal residue / bridging material (can appear as stains or severe discolorations)	Any contamination, defect, metal residue or bridging material that is >50% of original distance between bumps or eliminates the separation between adjacent metal lines
Ink dots	Ink on front of chip
Missing Bumps	Any missing bumps
Particles	Reject if particle reduces the original distance between bumps by 50%
Polyimide peeling, incomplete	Area bridging two adjacent top metal layers
Probe Marks	Reject if no probe marks
Probe Needle Drag	Solder drag or displacement >50% of original distance between bumps or crossing metal lines
Scratches	Scratches through the polyimide > 25% of the width of the metallization block under the bump

Table 2b: Back Side Visual Criteria

Note : substrate is not electrically active with respect to the device

Die Back Side Visual Inspection Category	Reject Criteria
Chips / Cracks	Chip thickness is nominal 700µm without the bump. MIL883 says reject if chip is >50% of total die thickness deep. Reject if chip is >250µm wide.
Correct back side marking for part number EPCXXXX, first line of back side laser mark will be XXXX	Reject if EPC part number is not correct in first scribe line or if marking is not legible
Orientation in pocket	Incorrectly oriented in pocket (locator dot should be on side near carrier tape holes)
Particles	Specification in development
Scratches	Specification in development
Stains / Discoloration / Burn Marks	Laser mark not readable

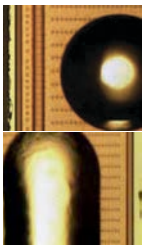
TABLE 3a: Some EPC Die Front Side Visual Examples

EPC Die Front Side
Visual Inspection Category:
Amount of remaining street

Reject Criteria:
Amount of remaining street can be zero providing no chip/crack is beyond second (outer) metal dummy ring.

See section on chips and cracks

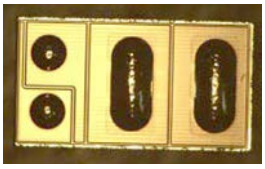
ACCEPTABLE

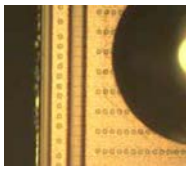


40X

200X

Street (thin white line) seen all the way around die in above pictures. Remaining street width can vary.

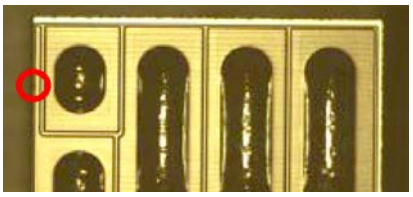




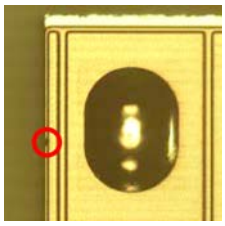
40X **200X**

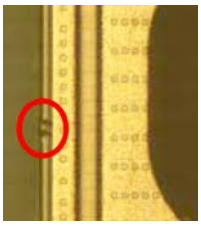
No street visible at 40X on left side of die, but no cracks into the outer metal dummy ring at 200X

REJECT



No street visible at 40X on left side of die. Chip can be seen. This chip extends past both metal dummy rings when checked at higher magnifications





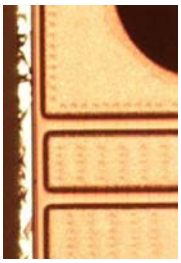
100X **200X**

Chip on left side can be seen at 100X is past both dummy metal rings. At 200X, defect is shown certainly past both the dummy metal rings.

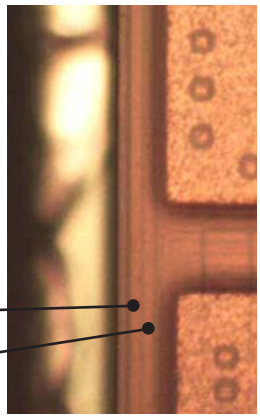
EPC Die Front Side
Visual Inspection Category:
Chips / Cracks

Reject Criteria:
chip/crack is beyond second (outer, #2) metal dummy ring

ACCEPTABLE

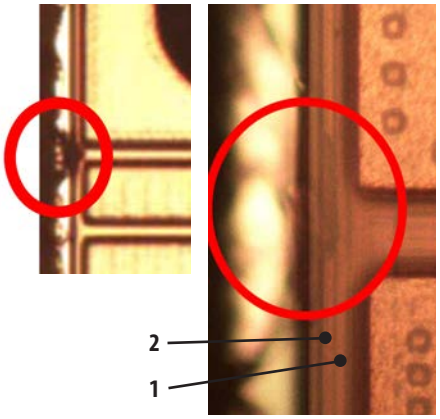


40X



At 400X, showing the two metal dummy rings in one die edge design type

REJECT

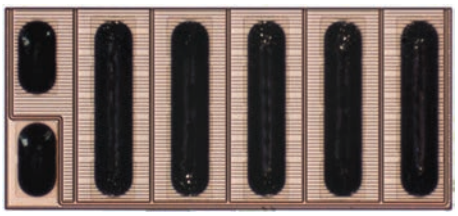


Shown at 400X. Defect is past the outer the metal dummy ring #2.

EPC Die Front Side
Visual Inspection Category:
Damaged solder bumps

Reject Criteria:
solder drag or displacement >50% of original distance between bumps; defect which reduces bump height by 30% of original height

ACCEPTABLE



Clean die

REJECT

Solder drag

Squashed bumps

TABLE 3a, continued: Some EPC Die Front Side Visual Examples

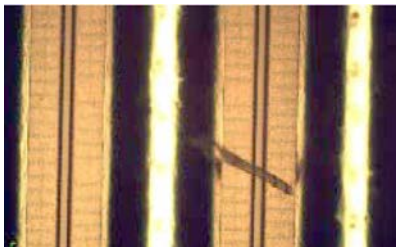
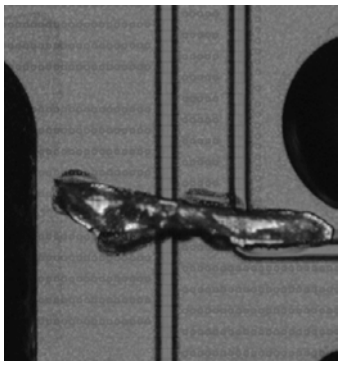
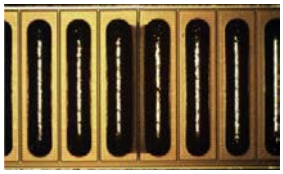
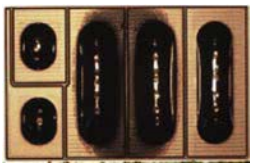
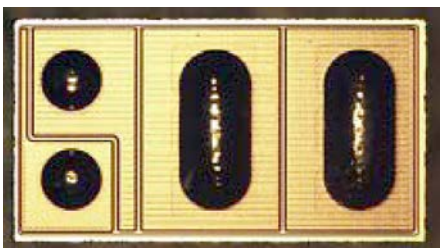
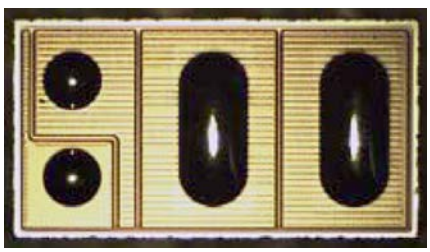
	ACCEPTABLE	REJECT
EPC Die Front Side **Visual Inspection Category:** Foreign material **Reject Criteria:** Foreign material linking any two bumps	 No foreign material (street not shown in picture)	 Foreign material bridging bumps
EPC Die Front Side **Visual Inspection Category:** Contamination /defect / metal residue / bridging material (can appear as stains or severe discolorations) **Reject Criteria:** Any contamination, defect, metal residue or bridging material that is >50% of original distance between bumps or eliminates the separation between adjacent metal lines	 No bridging, no contamination (street not shown in picture)	 [Picture courtesy of KYEC]
EPC Die Front Side **Visual Inspection Category:** Ink dots **Reject Criteria:** Ink on front of chip	  No ink on these chips	  Ink dot seen on chips
EPC Die Front Side **Visual Inspection Category:** Probe marks **Reject Criteria:** Reject if no probe marks	 This die has probe marks on the bumps	 No probe marks – this is a reject

TABLE 3a, continued: Some EPC Die Front Side Visual Examples

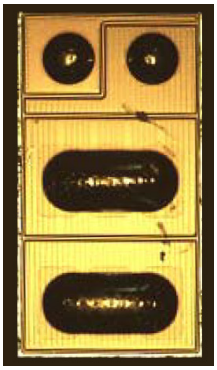
EPC Die Front Side Visual Inspection Category:
Scratches

Reject Criteria:
Scratches through the polyimide > 25% of the width of the metallization block under the bump or bridging metal lines

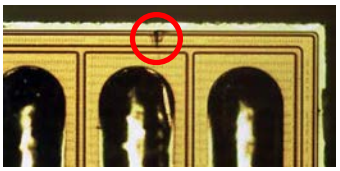
ACCEPTABLE

No scratches

REJECT



Scratch straddling metal lines



Scratch cuts across all the metal dummy rings and first metal 3 ring

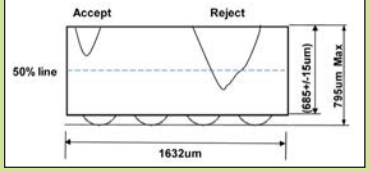
TABLE 3b: Some EPC Die Back Side Visual Examples

Note : substrate is not electrically active with respect to the device

EPC Die Back Side Visual Inspection Category:
Back Side Chips / Cracks

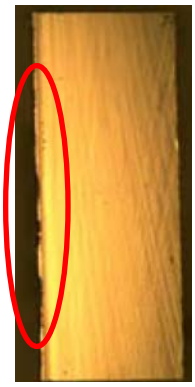
Reject Criteria:
Chip thickness is nominal 700µm without the bump. MIL883 says reject if chip is >50% of total chip thickness deep. Reject if chip is >250µm wide.

Die Back Side Chipping Details
Chip thickness is nominal 700µm without the bump. MIL883 says reject if chip is >50% of total die thickness deep; reject if chip is >250µm wide. Example against part number EPC1007 that has max length of 1632µm is shown below:



ACCEPTABLE

Die is > 0.9mm wide
Chips< 250µm wide



Same die as at left: Backside chips are very shallow

REJECT

Die is 1.6mm wide, chip is >250µm wide. Lower left corner is broken down to front side of die

TABLE 3b, continued: : Some EPC Die Back Side Visual Examples

Note : substrate is not electrically active with respect to the device

EPC Die Back Side
Visual Inspection Category:
Correct back side marking for part number EPCXXXX, first line of back side laser mark will be XXXX*

Reject Criteria:
Reject if EPC part number is not correct in first scribe line or if marking is not legible

The second and third lines of the back side laser mark are for lot traceability

**see datasheet for part marking spec of specific device*

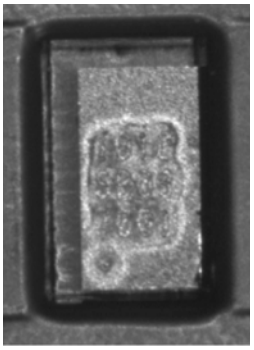
ACCEPTABLE

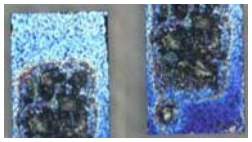
EPC1010: Top line is 1010

EPC1012: Top line is 1012

Color variation, but readable

REJECT

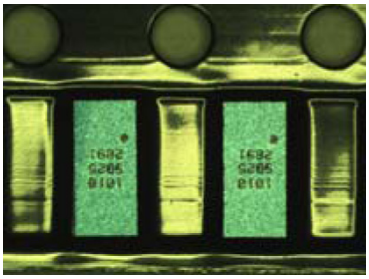



Unreadable
[Pictures courtesy of KYEC]

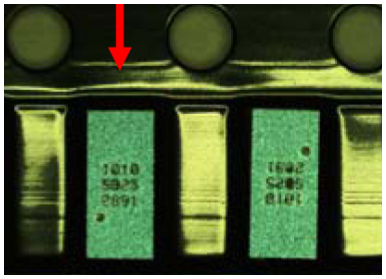
EPC Die Back Side
Visual Inspection Category:
Orientation in pocket

Reject Criteria:
Incorrectly oriented in pocket (locator dot should be on side near carrier tape holes)

ACCEPTABLE


Carrier tape holes and locator dot are both on this side of tape

REJECT


Die on left is incorrectly oriented. Locator dot is on opposite side of carrier tape holes

EPC Die Back Side
Visual Inspection Category:
Stains / Discoloration / Burn marks

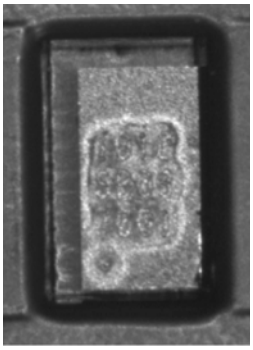
Reject Criteria:
Laser mark not readable

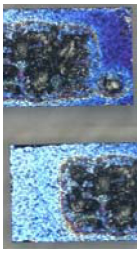
ACCEPTABLE

laser mark readable

Color variation, but readable

REJECT




Unreadable
[Pictures courtesy of KYEC]

References:

[1] http://epc-co.com/epc/documents/product-training/Appnote_GaNassembly.pdf
[2] http://epc-co.com/epc/documents/product-training/Characterization_guide.pdf
[3] http://epc-co.com/epc/documents/product-training/Appnote_GaNfundamentals.pdf