CSD25501F3 –20-V P-Channel FemtoFET™ MOSFET

1 Features

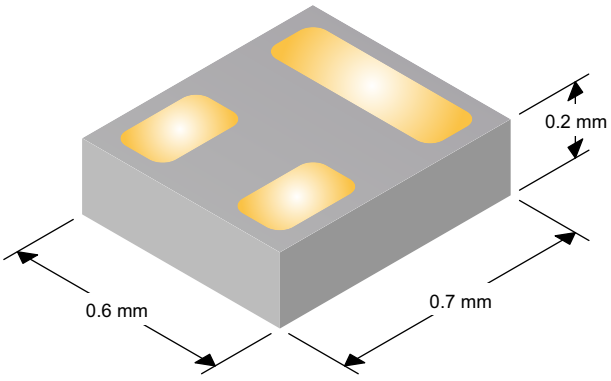
- Low on-resistance
- Ultra-low Q_g and Q_{gd}
- Ultra-small footprint
  - 0.7 mm × 0.6 mm
- Low profile
  - 0.22-mm max height
- Integrated ESD protection diode
- Lead and halogen free
- RoHS compliant

2 Applications

- Optimized for load switch applications
- Battery applications
- Handheld and mobile applications

3 Description

This –20-V, 64-mΩ, P-Channel FemtoFET™ MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing a substantial reduction in footprint size. The integrated 10-kΩ clamp resistor (R_C) allows the gate voltage (V_{GS}) to be operated above the maximum internal gate oxide value of –6 V, depending on duty cycle. The gate leakage (I_{GSS}) through the diode increases as V_{GS} is increased above –6 V.



Typical Part Dimensions

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	–20		V
Q_g	Gate Charge Total (–4.5 V)	1.02		nC
Q_{gd}	Gate Charge Gate-to-Drain	0.09		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –1.8 V	120	mΩ
		V_{GS} = –2.5 V	86	
		V_{GS} = –4.5 V	64	
$V_{GS(th)}$	Threshold Voltage	–0.75		V

Device Information

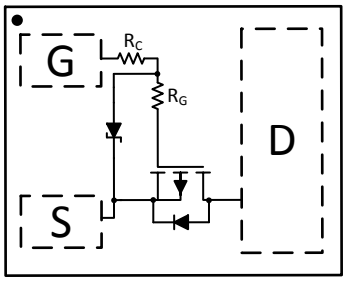
DEVICE(1)	QTY	MEDIA	PACKAGE	SHIP
CSD25501F3	3000	7-Inch Reel	Femto 0.73-mm × 0.64-mm Land Grid Array (LGA)	Tape and Reel
CSD25501F3T	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C (unless otherwise stated)		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	–20	V
V_{GS}	Gate-to-Source Voltage	–20	V
I_D	Continuous Drain Current(1)	–3.6	A
I_{DM}	Pulsed Drain Current(1) (2)	–13.6	A
P_D	Power Dissipation(1)	500	mW
$V_{(ESD)}$	Human Body Model (HBM)	4000	V
	Charged Device Model (CDM)	2000	
T_J, T_{stg}	Operating Junction, Storage Temperature	–55 to 150	°C

(1) Typical $R_{\theta JA}$ = 255°C/W mounted on FR4 material with minimum Cu mounting area.
(2) Pulse duration ≤ 100 µs, duty cycle ≤ 1%.



Top View

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2018) to Revision B (October 2021)	Page
• Added footnote with link to support document	8

Changes from Revision * (October 2017) to Revision A (January 2018)	Page
• Added mechanical dimension information and Table 7-1	7

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = –250 µA	–20			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = –16 V			–50	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = –6 V			–50	nA
		V_{DS} = 0 V, V_{GS} = –16 V			–1	mA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = –250 µA	–0.45	–0.75	–1.05	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = –1.8 V, I_{DS} = –0.1 A		120	260	mΩ
		V_{GS} = –2.5 V, I_{DS} = –0.4 A		86	125	
		V_{GS} = –4.5 V, I_{DS} = –0.4 A		64	76	
g_{fs}	Transconductance	V_{DS} = –2 V, I_{DS} = –0.4 A		3.4		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = –10 V, f = 100 kHz		295	385	pF
C_{oss}	Output capacitance			70	91	pF
C_{rss}	Reverse transfer capacitance			4.1	5.3	pF
R_G	Series gate resistance			33		Ω
R_C	Series clamp resistance			10,000		Ω
Q_g	Gate charge total (–4.5 V)	V_{DS} = –10 V, I_{DS} = –0.4 A		1.02	1.33	nC
Q_{gd}	Gate charge gate-to-drain			0.09		nC
Q_{gs}	Gate charge gate-to-source			0.45		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.36		nC
Q_{oss}	Output charge	V_{DS} = –10 V, V_{GS} = 0 V		1.8		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = –10 V, V_{GS} = –4.5 V, I_{DS} = –0.4 A, R_G = 0 Ω		474		ns
t_r	Rise time			428		ns
$t_{d(off)}$	Turnoff delay time			1154		ns
t_f	Fall time			945		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = –0.4 A, V_{GS} = 0 V		–0.73	–0.95	V
Q_{rr}	Reverse recovery charge	V_{DS} = –10 V, I_F = –0.4 A, di/dt = 200 A/µs		3.0		nC
t_{rr}	Reverse recovery time			7.4		ns

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	90	°C/W
	Junction-to-ambient thermal resistance(2)	255	°C/W

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

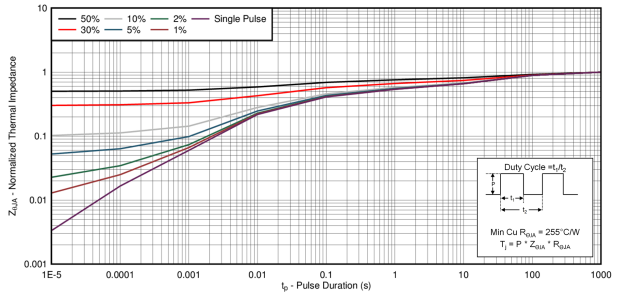


Figure 5-1. Transient Thermal Impedance

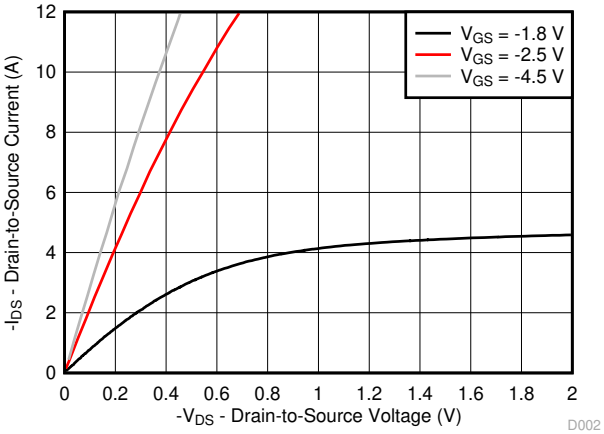
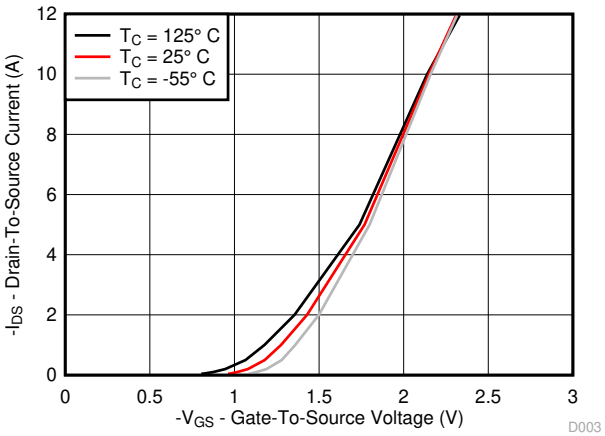
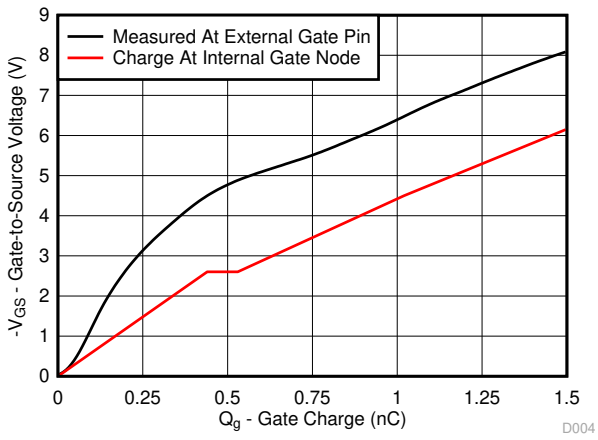


Figure 5-2. Saturation Characteristics



V_{DS} = –5 V

Figure 5-3. Transfer Characteristics



I_D = –0.4 A V_{DS} = –10 V

Figure 5-4. Gate Charge

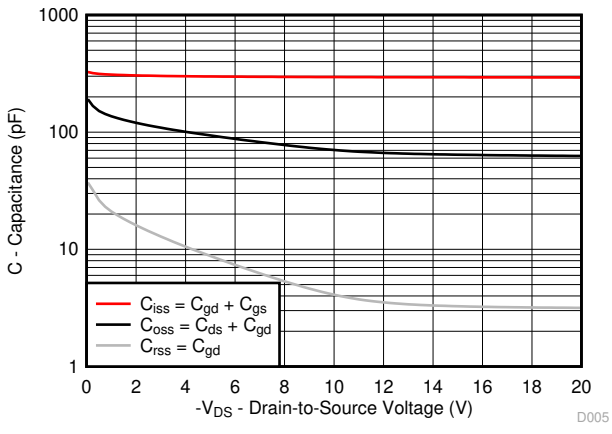
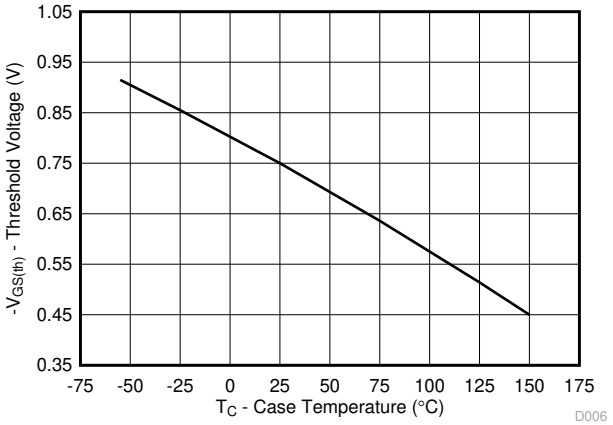


Figure 5-5. Capacitance

5.3 Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)



I_D = –250 µA

Figure 5-6. Threshold Voltage vs Temperature

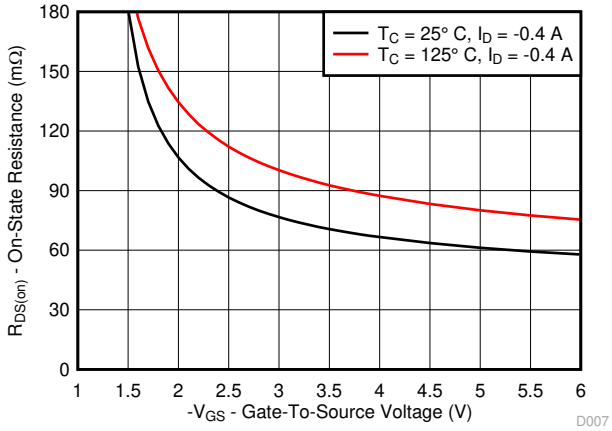
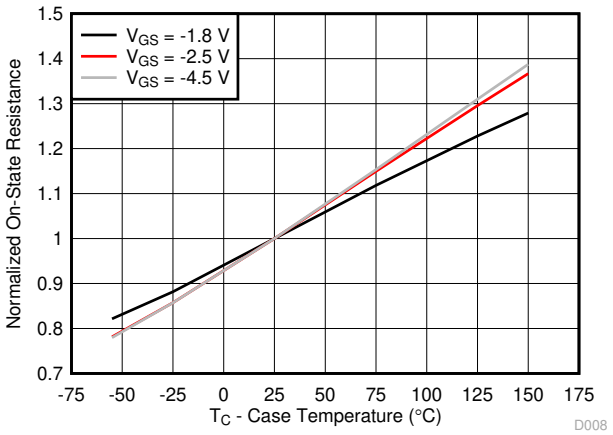


Figure 5-7. On-State Resistance vs Gate-to-Source Voltage



I_D = –0.4 A

Figure 5-8. Normalized On-State Resistance vs Temperature

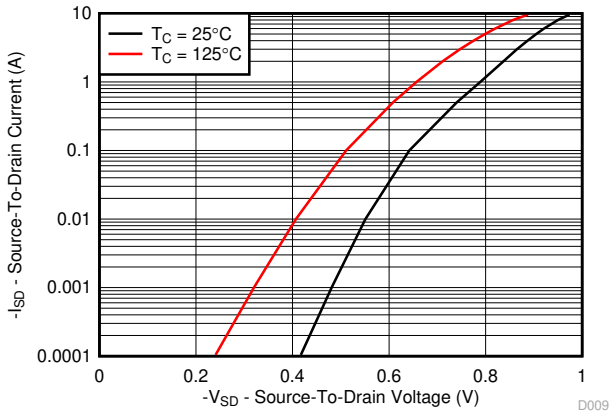
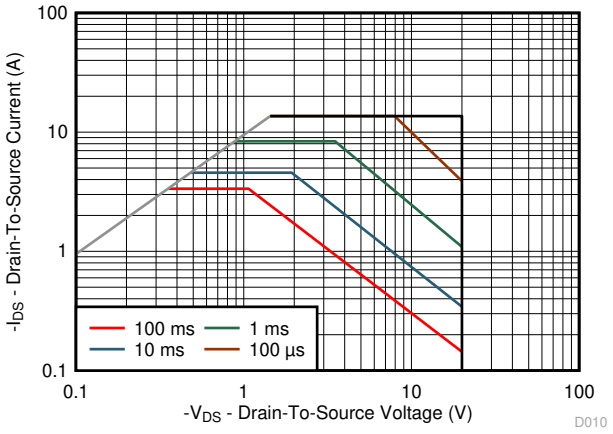
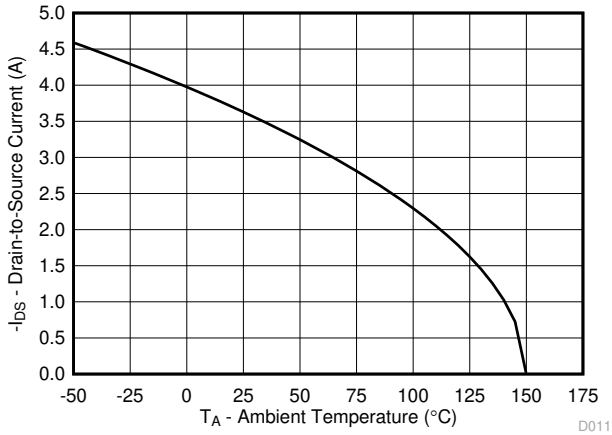


Figure 5-9. Typical Diode Forward Voltage



Single pulse, typical $R_{\theta JA}$ = 255°C/W

Figure 5-10. Maximum Safe Operating Area



Typical $R_{\theta JA}$ = 90°C/W

Figure 5-11. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.3 Trademarks

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6.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

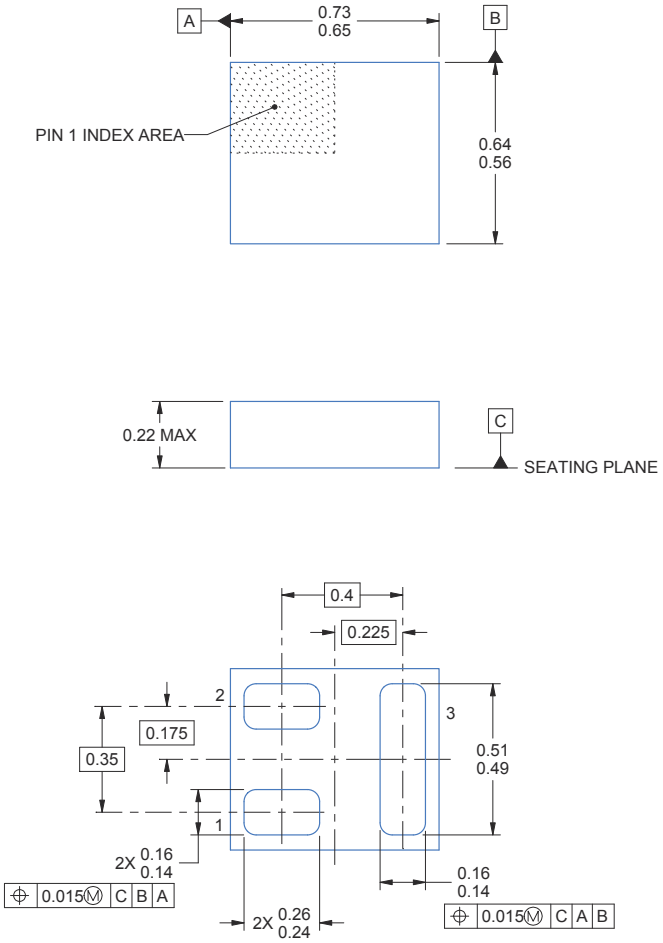
6.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



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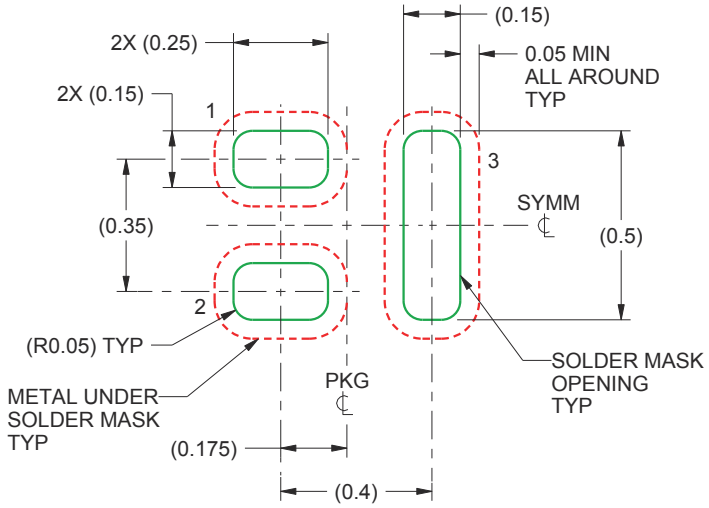
A. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
B. This drawing is subject to change without notice.
C. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device data sheet or contact a local TI representative.

Table 7-1. Pin Configuration

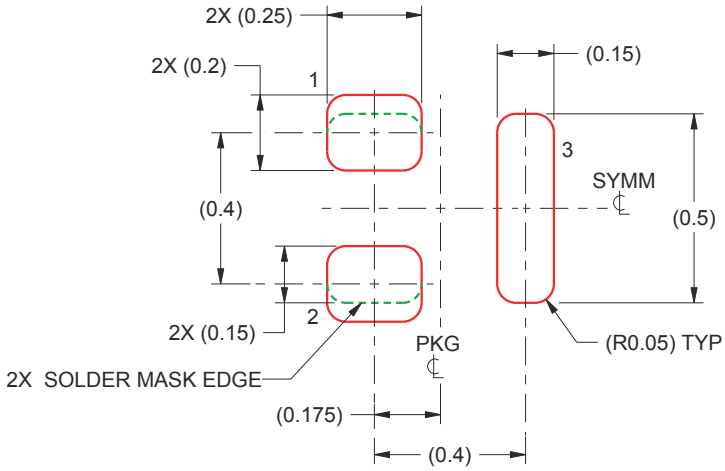
POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

7.2 Recommended Minimum PCB Layout



A. All dimensions are in millimeters.
B. For more information, see *FemtoFET Surface Mount Guide* (SLRA003D).

7.3 Recommended Stencil Pattern



A. All dimensions are in millimeters.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25501F3	ACTIVE	PICOSTAR	YJN	3	3000	RoHS & Green	Call TI	Level-1-260C-UNLIM	-55 to 150	V	Samples
CSD25501F3T	ACTIVE	PICOSTAR	YJN	3	250	RoHS & Green	Call TI	Level-1-260C-UNLIM	-55 to 150	V	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

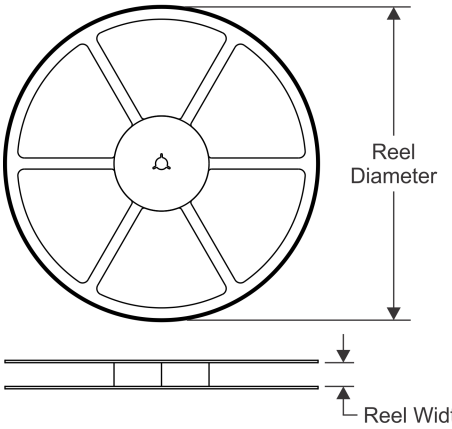
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

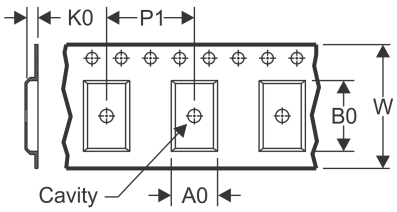
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

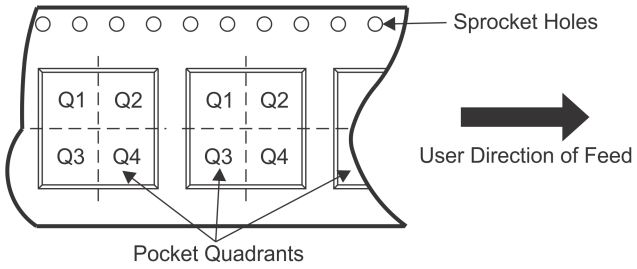


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

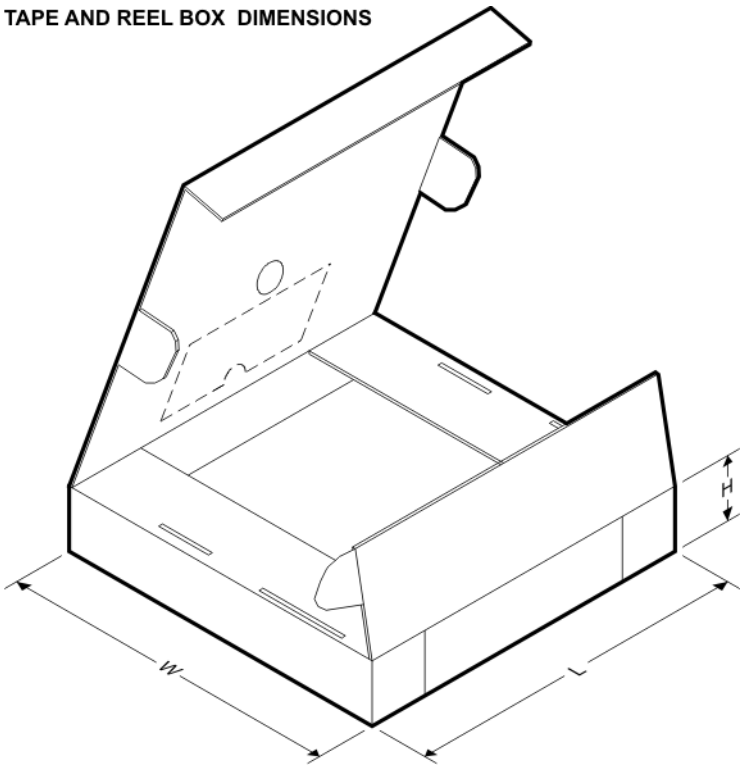
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25501F3	PICOSTAR	YJN	3	3000	180.0	8.4	0.7	0.79	0.31	4.0	8.0	Q2
CSD25501F3T	PICOSTAR	YJN	3	250	180.0	8.4	0.7	0.79	0.31	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25501F3	PICOSTAR	YJN	3	3000	182.0	182.0	20.0
CSD25501F3T	PICOSTAR	YJN	3	250	182.0	182.0	20.0

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