

## 行业标准双路运算放大器

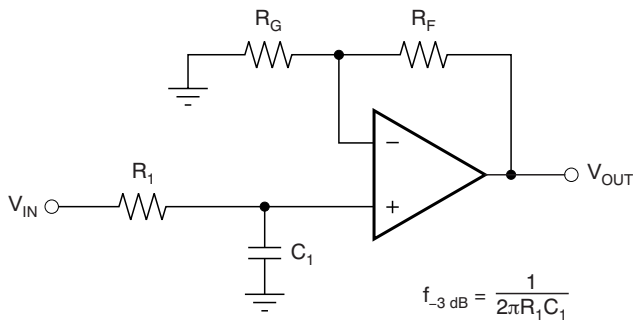
### 1 特性

- 3V 至 36V 宽电源范围 (B 版本)
- 静态电流: 每个放大器 300 $\mu$ A (B 版本, 典型值)
- 单位增益带宽为 1.2MHz (B 版本)
- 共模输入电压范围包括接地, 支持近地直接检测
- 3mV (25 $^{\circ}$ C 时) 的低输入失调电压 (A 和 B 版本, 最大值)
- 内部射频和 EMI 滤波器 (B 版本)
- 对于符合 MIL-PRF-38535 标准的产品, 所有参数均经过测试, 除非另外注明。对于所有其他产品, 生产流程不一定包含对所有参数的测试。

### 2 应用

- 商用网络和服务器电源单元
- 多功能打印机
- 电源和移动充电器
- 电机控制: 交流感应、刷式直流、无刷直流、高电压、低电压、永久磁性和步进电机
- 台式计算机和主板
- 室内外空调
- 洗衣机、烘干机和冰箱
- 交流逆变器、串式逆变器、中央逆变器和变频器
- 不间断电源
- 可编程逻辑控制器
- 电子销售点系统

单极低通滤波器



$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_1 C_1}\right)$$

### 3 说明

LM358B 和 LM2904B 是业界通用运算放大器 LM358 和 LM2904 的下一代版本, 其中包括两个高压 (36V) 运算放大器。这些器件为成本敏感型应用带来了出色的价值, 该器件的特性包括低失调电压 (300 $\mu$ V, 典型值)、接地共模输入范围以及高差分输入电压能力。

LM358B 和 LM2904B 运算放大器具有增强的功能, 例如单位增益稳定性、较低的 3mV (室温下的最大值) 失调电压和每个放大器 300 $\mu$ A (典型值) 的静态电流, 从而简化了电路设计。高 ESD (2kV, HBM) 和集成 EMI 以及射频滤波器可支持将 LM358B 和 LM2904B 器件用于最严苛、最具环境挑战性的应用。

LM358B 和 LM2904B 放大器采用行业通用封装 (包括 SOIC、TSSOP 和 VSSOP)。

器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
LM358B、LM2904B、LM358、LM358A、LM2904、LM2904V、LM258、LM258A	SOIC (8)	4.90mm × 3.90mm
LM358B <sup>(2)</sup> 、LM2904B <sup>(2)</sup> 、LM358、LM358A、LM2904、LM2490V	TSSOP (8)	3.00mm × 4.40mm
LM358B <sup>(2)</sup> 、LM2904B <sup>(2)</sup> 、LM358、LM358A、LM2904、LM2904V、LM258、LM258A	VSSOP (8)	3.00mm × 3.00mm
LM358、LM2904	SO (8)	5.20mm × 5.30mm
LM358、LM2904、LM358A、LM258、LM258A	PDIP (8)	9.81mm × 6.35mm
LM158、LM158A	CDIP (8)	9.60mm × 6.67mm
LM158、LM158A	LCCC (20)	8.89mm × 8.89mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

(2) 封装仅供预览。

## 目录

1 特性 .....	1	9.1 Overview .....	24
2 应用 .....	1	9.2 Functional Block Diagram - LM358B, LM358BA, LM2904B, LM2904BA .....	24
3 说明 .....	1	9.3 Feature Description .....	25
4 修订历史记录 .....	2	9.4 Device Functional Modes .....	25
5 <b>Device Comparison Table</b> .....	4	<b>10 Application and Implementation</b> .....	26
6 <b>Pin Configuration and Functions</b> .....	5	10.1 Application Information .....	26
7 <b>Specifications</b> .....	6	10.2 Typical Application .....	26
7.1 Absolute Maximum Ratings .....	6	<b>11 Power Supply Recommendations</b> .....	27
7.2 ESD Ratings .....	6	<b>12 Layout</b> .....	27
7.3 Recommended Operating Conditions .....	7	12.1 Layout Guidelines .....	27
7.4 Thermal Information .....	7	12.2 Layout Examples .....	28
7.5 Electrical Characteristics: LM358B and LM358BA ...	8	<b>13 器件和文档支持</b> .....	29
7.6 Electrical Characteristics: LM2904B and LM2904B..	9	13.1 文档支持 .....	29
7.7 Electrical Characteristics: LM358, LM358A .....	10	13.2 相关链接 .....	29
7.8 Electrical Characteristics: LM2904, LM2904V .....	11	13.3 接收文档更新通知 .....	29
7.9 Electrical Characteristics: LM158, LM158A .....	12	13.4 社区资源 .....	29
7.10 Electrical Characteristics: LM258, LM258A .....	13	13.5 商标 .....	29
7.11 Typical Characteristics .....	14	13.6 静电放电警告 .....	29
7.12 Typical Characteristics .....	21	13.7 术语表 .....	29
<b>8 Parameter Measurement Information</b> .....	23	<b>14 机械、封装和可订购信息</b> .....	30
<b>9 Detailed Description</b> .....	24		

## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision V (September 2018) to Revision W	Page
• Added specification in the <i>Device Comparison Table</i> .....	4
• Changed CDM ESD rating for LM358B and LM2904B in <i>ESD Ratings</i> .....	6
• Changed $V_S$ to $V_+$ in <i>Recommended Operating Conditions</i> .....	7
• Changed <i>Thermal Information</i> for the LM158FK and LM158JG devices .....	7
• 已添加 <i>Typical Characteristics</i> section for the LM358B and LM2490B op amps .....	14
• 已添加 test circuit for THD+N and small-signal step response, $G = -1$ in the <i>Parameter Measurement Information</i> section .....	23
• 已更改 the <a href="#">Functional Block Diagram</a> .....	24
• 已删除 在 <a href="#">相关链接</a> 部分中删除了 LM358B 和 LM2904B 的预览标识符 .....	29

Changes from Revision U (January 2017) to Revision V	Page
• 更改了数据表标题 .....	1
• 更改了特性 部分的前四个项目 .....	1
• 更改了应用 部分中的第一项并添加了四个新项 .....	1
• 在说明 部分的第一段中更改了电压值 .....	1
• 更改了说明 部分第二段中的文本 .....	1
• 已添加 在数据表中添加了器件 LM358B 和 LM2904B .....	1
• 更改了器件信息 表的前三行，并为预览状态器件添加了交叉引用的注释 .....	1
• Added <i>Device Comparison table</i> .....	4
• Added a table note to the <i>Pin Functions table</i> .....	5
• Changed "free-air temperature" to "ambient temperature" in the <i>Absolute Maximum Ratings</i> condition statement .....	6
• Changed all entries in the <i>Absolute Maximum Ratings table</i> except $T_J$ and $T_{stg}$ .....	6

• Deleted lead temperature and case temperature from <i>Absolute Maximum Ratings</i> .....	6
• Changed device listings and their voltage values in the <i>ESD Ratings</i> table .....	6
• Changed "free-air temperature" to "ambient temperature" in the <i>Recommended Operating Conditions</i> condition statement .....	7
• Changed table entries for all parameters in the <i>Recommended Operating Conditions</i> table .....	7
• Added rows to the Thermal Information table, and a table note regarding device-package combinations .....	7
• Deleted the <i>Operating Conditions</i> table.....	13
• Added a condition statement to the <i>Typical Characteristics</i> section .....	21
• Changed specific voltages to a <i>Recommended Operating Conditions</i> reference.....	24
• Changed unity-gain bandwidth from 0.7 MHz for all devices to 1.2 MHz for B-version devices.....	25
• Changed slew rate from 3 V/μs for all devices to 0.5 V/μs for B-version devices.....	25
• Changed the <b>Input Common Mode Range</b> section in multiple places throughout .....	25
• Changed $V_{CC}$ to $V_S$ in the <i>Application Information</i> section .....	26
• Subscripted the suffixes from $R_I$ and $R_F$ .....	26
• 已更改 <i>Operational Amplifier Board Layout for Noninverting Configuration</i> with an image that includes a dual op amp....	28
• 在表 1 .....	29

**Changes from Revision T (April 2015) to Revision U**
**Page**

• 已更改 数据表标题 .....	1
• 已添加 接收文档更新通知 部分和社区资源 部分 .....	29

**Changes from Revision S (January 2014) to Revision T**
**Page**

• 已添加 应用 部分、 <i>ESD</i> 额定值表、特性 说明 部分、器件功能模式、应用和实现 部分、电源推荐 部分、布局 部分、器件和文档支持 部分以及机械、封装和可订购信息 部分 .....	1
--	---

**Changes from Revision R (July 2010) to Revision S**
**Page**

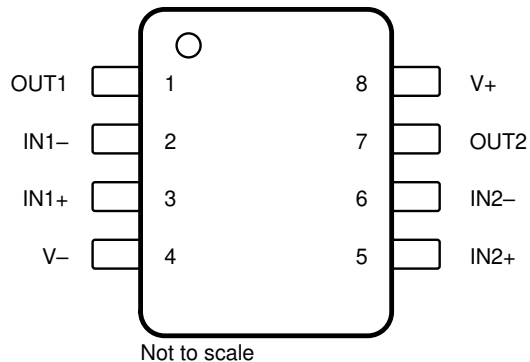
• 使用 Web 上的 PDF 将此数据表从 QS 格式转换为 DocZone.....	1
• 删除了订单信息表 .....	1
• 更新了特性 以包含“军用免责声明” .....	1
• 已添加 <i>Typical Characteristics</i> section .....	21
• 添加了 <i>ESD</i> 警告 .....	29

## 5 Device Comparison Table

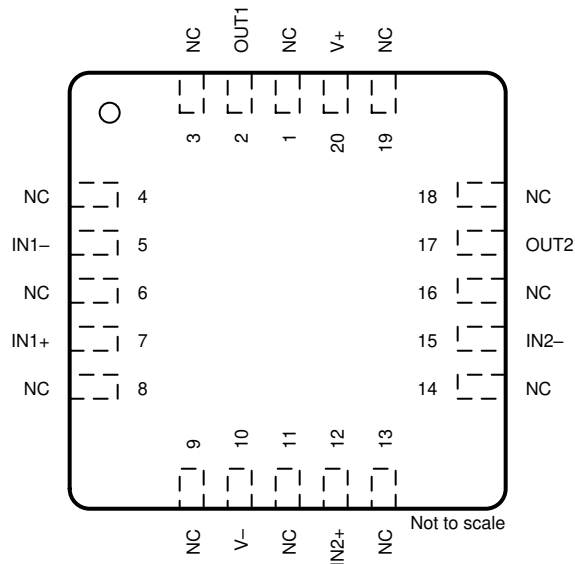
PART NUMBER	SUPPLY VOLTAGE	TEMPERATURE RANGE	V <sub>OS</sub> (MAXIMUM AT 25°C)	I <sub>Q</sub> / CH (TYPICAL AT 25°C)	INTEGRATED EMI FILTER	PACKAGE
LM358B	3 V–36 V	–40°C to 85°C	3 mV	300 µA	Yes	D, DGK, PW
LM2904B	3 V–36 V	–40°C to 125°C	3 mV	300 µA	Yes	D, DGK, PW
LM358	3 V–32 V	0°C to 70°C	7 mV	350 µA	No	D, PW, DGK, P, PS
LM2904	3 V–26 V	–40°C to 125°C	7 mV	350 µA	No	D, PW, DGK, P, PS
LM358A	3 V–32 V	0°C to 70°C	3 mV	350 µA	No	D, PW, DGK, P
LM2904V	3 V–32 V	–40°C to 125°C	7 mV	350 µA	No	D, PW
LM158	3 V–32 V	–55°C to 125°C	5 mV	350 µA	No	JG, FK
LM158A	3 V–32 V	–55°C to 125°C	3 mV	350 µA	No	JG, FK
LM258	3 V–32 V	–25°C to 85°C	5 mV	350 µA	No	D, DGK, P
LM258A	3 V–32 V	–25°C to 85°C	3 mV	350 µA	No	D, DGK, P

## 6 Pin Configuration and Functions

**D, DGK, P, PS, PW, and JG Packages**  
**8-Pin SOIC, VSSOP, PDIP, SO, TSSOP, and CDIP**  
**Top View**



**FK Package**  
**20-Pin LCCC**  
**Top View**



NC - No internal connection

### Pin Functions

NAME	PIN		I/O	DESCRIPTION
	LCCC <sup>(1)</sup>	SOIC, SSOP, CDIP, PDIP, SO, TSSOP, CFP <sup>(1)</sup>		
IN1-	5	2	I	Negative input
IN1+	7	3	I	Positive input
IN2-	15	6	I	Negative input
IN2+	12	5	I	Positive input
OUT1	2	1	O	Output
OUT2	17	7	O	Output
V-	10	4	—	Negative (lowest) supply or ground (for single-supply operation)
NC	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	—	—	No internal connection
V+	20	8	—	Positive (highest) supply

(1) For a listing of which devices are available in what packages, see [Device Comparison Table](#).

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT	
Supply voltage, $V_S = ([V+] - [V-])$	LM358B, LM358BA, LM2904B, LM2904BA		±20 or 40	V	
	LM158, LM258, LM358, LM158A, LM258A, LM358A, LM2904V		±16 or 32		
	LM2904		±13 or 26		
Differential input voltage, $V_{ID}$ <sup>(2)</sup>	LM358B, LM358BA, LM2904B, LM2904BA, LM158, LM258, LM358, LM158A, LM258A, LM358A, LM2904V	-32	32	V	
	LM2904	-26	26		
Input voltage, $V_I$	Either input	LM358B, LM358BA, LM2904B, LM2904BA	-0.3	40	V
		LM158, LM258, LM358, LM158A, LM258A, LM358A, LM2904V	-0.3	32	
		LM2904	-0.3	26	
Duration of output short circuit (one amplifier) to ground at (or below) $T_A = 25^\circ\text{C}$ , $V_S \leq 15\text{ V}$ <sup>(3)</sup>			Unlimited	s	
Operating ambient temperature, $T_A$	LM158, LM158A	-55	125	°C	
	LM258, LM258A	-25	85		
	LM358B, LM358BA	-40	85		
	LM358, LM358A	0	70		
	LM2904B, LM2904BA, LM2904, LM2904V	-40	125		
Operating virtual-junction temperature, $T_J$			150	°C	
Storage temperature, $T_{stg}$		-65	150	°C	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Differential voltages are at IN+, with respect to IN-.
- (3) Short circuits from outputs to  $V_S$  can cause excessive heating and eventual destruction.

### 7.2 ESD Ratings

		VALUE	UNIT
<b>LM358B, LM358BA, LM2904B, AND LM2904BA</b>			
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	
<b>LM158, LM258, LM358, LM158, LM258A, LM358A, LM2904, AND LM2904V</b>			
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V <sub>S</sub>	Supply voltage, V <sub>S</sub> = ([V+] – [V–])	LM358B, LM358BA, LM2904B, LM2904BA	3	36	V
		LM158, LM258, LM358, LM158A, LM258A, LM358A, LM2904V	3	30	
		LM2904	3	26	
V <sub>CM</sub>	Common-mode voltage	V–	V+ – 2	V	
T <sub>A</sub>	Operating ambient temperature	LM358B, LM358BA	–40	85	°C
		LM2904B, LM2904BA, LM2904, LM2904V	–40	125	
		LM358, LM358A	0	70	
		LM258, LM258A	–20	85	
		LM158, LM158A	–55	125	

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	LM258, LM258A, LM358, LM358A, LM358B, LM358BA, LM2904, LM2904B, LM2904BA, LM2904V <sup>(2)</sup>					LM158, LM158A		UNIT	
	D (SOIC)	DGK (VSSOP)	P (PDIP)	PS (SO)	PW (TSSOP)	FK (LCCC)	JG (CDIP)		
	8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	20 PINS	8 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	124.7	181.4	80.9	116.9	171.7	84.0	112.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	66.9	69.4	70.4	62.5	68.8	56.9	63.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	67.9	102.9	57.4	68.6	99.2	57.5	100.3	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	19.2	11.8	40	21.9	11.5	51.7	35.7	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	67.2	101.2	56.9	67.6	97.9	57.1	93.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	—	—	—	—	—	10.6	22.3	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

(2) For a listing of which devices are available in what packages, see [Device Comparison Table](#).

## 7.5 Electrical Characteristics: LM358B and LM358BA

$V_S = (V+) - (V-) = 5\text{ V} - 36\text{ V} (\pm 2.5\text{ V} - \pm 18\text{ V})$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = V_{OUT} = V_S/2$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S/2$   
(unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
<b>OFFSET VOLTAGE</b>								
$V_{OS}$	Input offset voltage	LM358B			$\pm 0.3$	$\pm 3.0$	mV	
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$				$\pm 4$	mV
		LM358BA					$\pm 2.0$	mV
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$					$\pm 2.5$
$dV_{OS}/dT$	Input offset voltage drift		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}^{(1)}$		$\pm 3.5$	11	$\mu\text{V}/^\circ\text{C}$	
PSRR	Power Supply Rejection Ratio				$\pm 2$	15	$\mu\text{V}/\text{V}$	
	Channel separation, dc	$f = 1\text{ kHz}$ to $20\text{ kHz}$			$\pm 1$		$\mu\text{V}/\text{V}$	
<b>INPUT VOLTAGE RANGE</b>								
$V_{CM}$	Common-mode voltage range	$V_S = 3\text{ V}$ to $36\text{ V}$			(V-)	(V+) - 1.5	V	
		$V_S = 5\text{ V}$ to $36\text{ V}$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		(V-)	(V+) - 2	V	
CMRR	Common-mode rejection ratio	$(V-) \leq V_{CM} \leq (V+) - 1.5\text{ V}$	$V_S = 3\text{ V}$ to $36\text{ V}$			20	100	$\mu\text{V}/\text{V}$
		$(V-) \leq V_{CM} \leq (V+) - 2.0\text{ V}$	$V_S = 5\text{ V}$ to $36\text{ V}$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			25	316
<b>INPUT BIAS CURRENT</b>								
$I_B$	Input bias current				$\pm 10$	$\pm 35$	nA	
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}^{(1)}$				$\pm 50$	nA
$I_{OS}$	Input offset current				0.5	4	nA	
			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}^{(1)}$				5	nA
$dI_{OS}/dT$	Input offset current drift		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		10		$\text{pA}/^\circ\text{C}$	
<b>NOISE</b>								
$E_n$	Input voltage noise	$f = 0.1$ to $10\text{ Hz}$			3		$\mu\text{V}_{PP}$	
$e_n$	Input voltage noise density	$f = 1\text{ kHz}$			40		$\text{nV}/\sqrt{\text{Hz}}$	
<b>INPUT IMPEDANCE</b>								
$Z_{ID}$	Differential				$10 \parallel 0.1$		$\text{M}\Omega \parallel \text{pF}$	
$Z_{IC}$	Common-mode				$4 \parallel 1.5$		$\text{G}\Omega \parallel \text{pF}$	
<b>OPEN-LOOP GAIN</b>								
$A_{OL}$	Open-loop voltage gain	$V_S = 15\text{ V}$ ; $V_O = 1\text{ V}$ to $11\text{ V}$ ; $R_L \geq 10\text{ k}\Omega$ , connected to (V-)			70	140	$\text{V}/\text{mV}$	
				$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			35	$\text{V}/\text{mV}$
<b>FREQUENCY RESPONSE</b>								
GBW	Gain bandwidth product				1.2		MHz	
SR	Slew rate	$G = +1$			0.5		$\text{V}/\mu\text{s}$	
$\theta_m$	Phase margin	$G = +1$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$			56		$^\circ$	
$t_{OR}$	Overload recovery time	$V_{IN} \times \text{gain} > V_S$			10		$\mu\text{s}$	
$t_s$	Settling time	To 0.1%, $V_S = 5\text{ V}$ , 2-V Step, $G = +1$ , $C_L = 100\text{ pF}$			4		$\mu\text{s}$	
THD+N	Total harmonic distortion + noise	$G = +1$ , $f = 1\text{ kHz}$ , $V_O = 3.53\text{ V}_{RMS}$ , $V_S = 36\text{ V}$ , $R_L = 100\text{ k}\Omega$ , $I_{OUT} \leq \pm 50\mu\text{A}$ , $\text{BW} = 80\text{ kHz}$			0.001		%	
<b>OUTPUT</b>								
$V_O$	Voltage output swing from rail	Positive Rail (V+)	$I_{OUT} = 50\mu\text{A}$		1.35	1.42	V	
			$I_{OUT} = 1\text{ mA}$		1.4	1.48	V	
			$I_{OUT} = 5\text{ mA}^{(1)}$		1.5	1.61	V	
		Negative Rail (V-)	$I_{OUT} = 50\mu\text{A}$		100	150	mV	
			$I_{OUT} = 1\text{ mA}$		0.75	1	V	
		$V_S = 5\text{ V}$ , $R_L \leq 10\text{ k}\Omega$ connected to (V-)	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		5	20	mV	
$I_O$	Output current	$V_S = 15\text{ V}$ ; $V_O = V_-$ ; $V_{ID} = 1\text{ V}$	Source <sup>(1)</sup>		-20	-30	mA	
				$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		-10		
		$V_S = 15\text{ V}$ ; $V_O = V_+$ ; $V_{ID} = -1\text{ V}$	Sink <sup>(1)</sup>		10	20		
				$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		5		
		$V_{ID} = -1\text{ V}$ ; $V_O = (V_-) + 200\text{ mV}$			60	100	$\mu\text{A}$	
$I_{SC}$	Short-circuit current	$V_S = 20\text{ V}$ , (V+) = $10\text{ V}$ , (V-) = $-10\text{ V}$ , $V_O = 0\text{ V}$			$\pm 40$	$\pm 60$	mA	
$C_{LOAD}$	Capacitive load drive				100		pF	
$R_O$	Open-loop output resistance	$f = 1\text{ MHz}$ , $I_O = 0\text{ A}$			300		$\Omega$	
<b>POWER SUPPLY</b>								
$I_Q$	Quiescent current per amplifier	$V_S = 5\text{ V}$ ; $I_O = 0\text{ A}$	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		300	460	$\mu\text{A}$	
							800	$\mu\text{A}$
$I_Q$	Quiescent current per amplifier	$V_S = 36\text{ V}$ ; $I_O = 0\text{ A}$					$\mu\text{A}$	

(1) Specified by characterization only

## 7.6 Electrical Characteristics: LM2904B and LM2904B

$V_S = (V+) - (V-) = 5\text{ V} - 36\text{ V} (\pm 2.5\text{ V} - \pm 18\text{ V})$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = V_{OUT} = V_S/2$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S/2$   
(unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
<b>OFFSET VOLTAGE</b>								
$V_{OS}$	Input offset voltage	LM2904B		$\pm 0.3$	$\pm 3.0$		mV	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			$\pm 4$		mV
		LM2904BA				$\pm 2.0$		mV
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			$\pm 2.5$		mV
$dV_{OS}/dT$	Input offset voltage drift		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}^{(1)}$	$\pm 3.5$	12		$\mu\text{V}/^\circ\text{C}$	
PSRR	Power Supply Rejection Ratio			$\pm 2$	15		$\mu\text{V}/\text{V}$	
	Channel separation, dc	$f = 1\text{ kHz}$ to $20\text{ kHz}$		$\pm 1$			$\mu\text{V}/\text{V}$	
<b>INPUT VOLTAGE RANGE</b>								
$V_{CM}$	Common-mode voltage range	$V_S = 3\text{ V}$ to $36\text{ V}$		(V-)	(V+) - 1.5		V	
		$V_S = 5\text{ V}$ to $36\text{ V}$		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	(V-)	(V+) - 2		V
CMRR	Common-mode rejection ratio	$(V-) \leq V_{CM} \leq (V+) - 1.5\text{ V}$	$V_S = 3\text{ V}$ to $36\text{ V}$		20	100	$\mu\text{V}/\text{V}$	
		$(V-) \leq V_{CM} \leq (V+) - 2.0\text{ V}$	$V_S = 5\text{ V}$ to $36\text{ V}$	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	25	316		
<b>INPUT BIAS CURRENT</b>								
$I_B$	Input bias current				$\pm 10$	$\pm 35$	nA	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}^{(1)}$			$\pm 50$	nA	
$I_{OS}$	Input offset current				0.5	4	nA	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}^{(1)}$			5	nA	
$dI_{OS}/dT$	Input offset current drift		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	10			$\text{pA}/^\circ\text{C}$	
<b>NOISE</b>								
$E_n$	Input voltage noise	$f = 0.1$ to $10\text{ Hz}$			3		$\mu\text{V}_{PP}$	
$e_n$	Input voltage noise density	$f = 1\text{ kHz}$			40		$\text{nV}/\sqrt{\text{Hz}}$	
<b>INPUT IMPEDANCE</b>								
$Z_{ID}$	Differential				$10 \parallel 0.1$		$\text{M}\Omega \parallel \text{pF}$	
$Z_{IC}$	Common-mode				$4 \parallel 1.5$		$\text{G}\Omega \parallel \text{pF}$	
<b>OPEN-LOOP GAIN</b>								
$A_{OL}$	Open-loop voltage gain	$V_S = 15\text{ V}$ ; $V_O = 1\text{ V}$ to $11\text{ V}$ ; $R_L \geq 10\text{ k}\Omega$ , connected to (V-)			70	140	V/mV	
				$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	35		V/mV	
<b>FREQUENCY RESPONSE</b>								
GBW	Gain bandwidth product				1.2		MHz	
SR	Slew rate	$G = +1$			0.5		V/ $\mu\text{s}$	
$\theta_m$	Phase margin	$G = +1$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$			56		°	
$t_{OR}$	Overload recovery time	$V_{IN} \times \text{gain} > V_S$			10		$\mu\text{s}$	
$t_s$	Settling time	To 0.1%, $V_S = 5\text{ V}$ , 2-V Step, $G = +1$ , $C_L = 100\text{ pF}$			4		$\mu\text{s}$	
THD+N	Total harmonic distortion + noise	$G = +1$ , $f = 1\text{ kHz}$ , $V_O = 3.53\text{ V}_{RMS}$ , $V_S = 36\text{ V}$ , $R_L = 100\text{ k}\Omega$ , $I_{OUT} \leq \pm 50\mu\text{A}$ , $\text{BW} = 80\text{ kHz}$			0.001		%	
<b>OUTPUT</b>								
$V_O$	Voltage output swing from rail	Positive Rail (V+)	$I_{OUT} = 50\mu\text{A}$		1.35	1.42	V	
			$I_{OUT} = 1\text{ mA}$		1.4	1.48	V	
			$I_{OUT} = 5\text{ mA}^{(1)}$		1.5	1.61	V	
		Negative Rail (V-)	$I_{OUT} = 50\mu\text{A}$		100	150	mV	
			$I_{OUT} = 1\text{ mA}$		0.75	1	V	
			$V_S = 5\text{ V}$ , $R_L \leq 10\text{ k}\Omega$ connected to (V-)	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		5	20	mV
$I_O$	Output current	$V_S = 15\text{ V}$ ; $V_O = V_-$ ; $V_{ID} = 1\text{ V}$	Source <sup>(1)</sup>		-20	-30	mA	
				$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		-10		
		$V_S = 15\text{ V}$ ; $V_O = V_+$ ; $V_{ID} = -1\text{ V}$	Sink <sup>(1)</sup>		10	20		
				$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		5		
$V_{ID} = -1\text{ V}$ ; $V_O = (V_-) + 200\text{ mV}$			60	100	$\mu\text{A}$			
$I_{SC}$	Short-circuit current	$V_S = 20\text{ V}$ , (V+) = $10\text{ V}$ , (V-) = $-10\text{ V}$ , $V_O = 0\text{ V}$			$\pm 40$	$\pm 60$	mA	
$C_{LOAD}$	Capacitive load drive				100		pF	
$R_O$	Open-loop output resistance	$f = 1\text{ MHz}$ , $I_O = 0\text{ A}$			300		$\Omega$	
<b>POWER SUPPLY</b>								
$I_Q$	Quiescent current per amplifier	$V_S = 5\text{ V}$ ; $I_O = 0\text{ A}$	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		300	460	$\mu\text{A}$	
							800	$\mu\text{A}$

(1) Specified by characterization only

## 7.7 Electrical Characteristics: LM358, LM358A

For  $V_S = (V_+) - (V_-) = 5\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ , (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP <sup>(2)</sup>	MAX	UNIT	
<b>OFFSET VOLTAGE</b>								
$V_{OS}$	Input offset voltage	$V_S = 5\text{ V to }30\text{ V}$ ; $V_{CM} = 0\text{ V}$ ; $V_O = 1.4\text{ V}$	LM358	$T_A = 0^\circ\text{C to }70^\circ\text{C}$	3	7	mV	
			LM358A		2	3		
$dV_{OS}/dT$	Input offset voltage drift		LM358	$T_A = 0^\circ\text{C to }70^\circ\text{C}$	7		$\mu\text{V}/^\circ\text{C}$	
			LM358A		7	20		
PSRR	Input offset voltage vs power supply ( $\Delta V_{IO}/\Delta V_S$ )	$V_S = 5\text{ V to }30\text{ V}$			65	100	dB	
$V_{O1}/V_{O2}$	Channel separation	$f = 1\text{ kHz to }20\text{ kHz}$				120	dB	
<b>INPUT VOLTAGE RANGE</b>								
$V_{CM}$	Common-mode voltage range	$V_S = 5\text{ V to }30\text{ V}$	LM358	$T_A = 0^\circ\text{C to }70^\circ\text{C}$	(V-)	(V+) - 1.5	V	
		$V_S = 30\text{ V}$	LM358A					
		$V_S = 5\text{ V to }30\text{ V}$	LM358		(V-)	(V+) - 2		
		$V_S = 30\text{ V}$	LM358A					
CMRR	Common-mode rejection ratio	$V_S = 5\text{ V to }30\text{ V}$ ; $V_{CM} = 0\text{ V}$			65	80	dB	
<b>INPUT BIAS CURRENT</b>								
$I_B$	Input bias current	$V_O = 1.4\text{ V}$	LM358	$T_A = 0^\circ\text{C to }70^\circ\text{C}$	-20	-250	nA	
			LM358A		-15	-100		
$I_{OS}$	Input offset current	$V_O = 1.4\text{ V}$	LM358	$T_A = 0^\circ\text{C to }70^\circ\text{C}$	2	50	nA	
			LM358A		2	30		
$dI_{OS}/dT$	Input offset current drift				10		$\mu\text{A}/^\circ\text{C}$	
			LM358A	$T_A = 0^\circ\text{C to }70^\circ\text{C}$		300		
<b>NOISE</b>								
$e_n$	Input voltage noise density	$f = 1\text{ kHz}$				40	$\text{nV}/\sqrt{\text{Hz}}$	
<b>OPEN-LOOP GAIN</b>								
$A_{OL}$	Open-loop voltage gain	$V_S = 15\text{ V}$ ; $V_O = 1\text{ V to }11\text{ V}$ ; $R_L \geq 2\text{ k}\Omega$			25	100	V/mV	
				$T_A = 0^\circ\text{C to }70^\circ\text{C}$	15			
<b>FREQUENCY RESPONSE</b>								
GBW	Gain bandwidth product					0.7	MHz	
SR	Slew rate	$G = +1$				0.3	V/ $\mu\text{s}$	
<b>OUTPUT</b>								
$V_O$	Voltage output swing from rail	Positive rail	$V_S = 30\text{ V}$ ; $R_L = 2\text{ k}\Omega$	$T_A = 0^\circ\text{C to }70^\circ\text{C}$		4	V	
			$V_S = 30\text{ V}$ ; $R_L \geq 10\text{ k}\Omega$			2		3
			$V_S = 5\text{ V}$ ; $R_L \geq 2\text{ k}\Omega$					1.5
		Negative rail	$V_S = 5\text{ V}$ ; $R_L \leq 10\text{ k}\Omega$	$T_A = 0^\circ\text{C to }70^\circ\text{C}$		5	20	mV
$I_O$	Output current	$V_S = 15\text{ V}$ ; $V_O = 0\text{ V}$ ; $V_{ID} = 1\text{ V}$	Source	LM358		-20	-30	mA
					$T_A = 0^\circ\text{C to }70^\circ\text{C}$	-10		
			Sink			10	20	
				$T_A = 0^\circ\text{C to }70^\circ\text{C}$	5			
		$V_{ID} = -1\text{ V}$ ; $V_O = 200\text{ mV}$			12	30	$\mu\text{A}$	
$I_{SC}$	Short-circuit current	$V_S = 10\text{ V}$ ; $V_O = V_S/2$				$\pm 40$	$\pm 60$	mA
<b>POWER SUPPLY</b>								
$I_Q$	Quiescent current per amplifier	$V_O = 2.5\text{ V}$ ; $I_O = 0\text{ A}$	$T_A = 0^\circ\text{C to }70^\circ\text{C}$		350	600	$\mu\text{A}$	
		$V_S = 30\text{ V}$ ; $V_O = 15\text{ V}$ ; $I_O = 0\text{ A}$			500	1000		

- (1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. Maximum  $V_S$  for testing purposes is 30 V for LM358 and LM358A.
- (2) All typical values are  $T_A = 25^\circ\text{C}$ .

## 7.8 Electrical Characteristics: LM2904, LM2904V

For  $V_S = (V+) - (V-) = 5\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ , (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP <sup>(2)</sup>	MAX	UNIT	
<b>OFFSET VOLTAGE</b>								
$V_{OS}$	Input offset voltage	$V_S = 5\text{ V}$ to maximum; $V_{CM} = 0\text{ V}$ ; $V_O = 1.4\text{ V}$	Non-A suffix devices	$T_A = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$	3	7	mV	
			A-suffix devices	$T_A = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$	1	2		
$dV_{OS}/dT$	Input offset voltage drift			$T_A = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$	7		$\mu\text{V}/^\circ\text{C}$	
PSRR	Input offset voltage vs power supply ( $\Delta V_{IO}/\Delta V_S$ )	$V_S = 5\text{ V}$ to $30\text{ V}$			65	100	dB	
$V_{O1}/V_{O2}$	Channel separation	$f = 1\text{ kHz}$ to $20\text{ kHz}$			120		dB	
<b>INPUT VOLTAGE RANGE</b>								
$V_{CM}$	Common-mode voltage range	$V_S = 5\text{ V}$ to maximum			(V-)	(V+) - 1.5	V	
			$T_A = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$		(V-)	(V+) - 2		
CMRR	Common-mode rejection ratio	$V_S = 5\text{ V}$ to maximum; $V_{CM} = 0\text{ V}$			65	80	dB	
<b>INPUT BIAS CURRENT</b>								
$I_B$	Input bias current	$V_O = 1.4\text{ V}$			-20	-250	nA	
			$T_A = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$			-500		
$I_{OS}$	Input offset current	$V_O = 1.4\text{ V}$	Non-V suffix device	$T_A = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$	2	50	nA	
			V-suffix device	$T_A = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$	2	50		
$dI_{OS}/dT$	Input offset current drift			$T_A = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$	10		$\text{pA}/^\circ\text{C}$	
<b>NOISE</b>								
$e_n$	Input voltage noise density	$f = 1\text{ kHz}$			40		$\text{nV}/\sqrt{\text{Hz}}$	
<b>OPEN-LOOP GAIN</b>								
$A_{OL}$	Open-loop voltage gain	$V_S = 15\text{ V}$ ; $V_O = 1\text{ V}$ to $11\text{ V}$ ; $R_L \geq 2\text{ k}\Omega$			25	100	V/mV	
			$T_A = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$			15		
<b>FREQUENCY RESPONSE</b>								
GBW	Gain bandwidth product				0.7		MHz	
SR	Slew rate	$G = +1$			0.3		$\text{V}/\mu\text{s}$	
<b>OUTPUT</b>								
$V_O$	Voltage output swing from rail	Positive rail	Non-V suffix device	$V_S = \text{maximum}$ ; $R_L = 2\text{ k}\Omega$	$T_A = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$	$V_S - 1.5$	4	V
						$V_S = \text{maximum}$ ; $R_L \geq 10\text{ k}\Omega$	2	
		V-suffix device	$V_S = \text{maximum}$ ; $R_L = 2\text{ k}\Omega$		6			
			$V_S = \text{maximum}$ ; $R_L \geq 10\text{ k}\Omega$		4	5		
Negative rail	$V_S = 5\text{ V}$ ; $R_L \leq 10\text{ k}\Omega$	$T_A = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$	5	20	mV			
$I_O$	Output current	$V_S = 15\text{ V}$ ; $V_O = 0\text{ V}$ ; $V_{ID} = 1\text{ V}$	Source			-20	-30	mA
				$T_A = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$			-10	
		$V_S = 15\text{ V}$ ; $V_O = 15\text{ V}$ ; $V_{ID} = -1\text{ V}$	Sink	$T_A = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$	10	20		
		$V_{ID} = -1\text{ V}$ ; $V_O = 200\text{ mV}$	Non-V suffix device		30			
	V-suffix device		12	40	$\mu\text{A}$			
$I_{SC}$	Short-circuit current	$V_S = 10\text{ V}$ ; $V_O = V_S / 2$			$\pm 40$	$\pm 60$	mA	
<b>POWER SUPPLY</b>								
$I_Q$	Quiescent current per amplifier	$V_O = 2.5\text{ V}$ ; $I_O = 0\text{ A}$	$T_A = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$		350	600	$\mu\text{A}$	
		$V_S = \text{maximum}$ ; $V_O = \text{maximum} / 2$ ; $I_O = 0\text{ A}$			500	1000		

- All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. Maximum  $V_S$  for testing purposes is  $26\text{ V}$  for LM2904 and  $32\text{ V}$  for LM2904V.
- All typical values are  $T_A = 25\text{ }^\circ\text{C}$ .

## 7.9 Electrical Characteristics: LM158, LM158A

For  $V_S = (V_+) - (V_-) = 5\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ , (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP <sup>(2)</sup>	MAX	UNIT	
<b>OFFSET VOLTAGE</b>								
$V_{OS}$	Input offset voltage	$V_S = 5\text{ V to }30\text{ V}$ ; $V_{CM} = 0\text{ V}$ ; $V_O = 1.4\text{ V}$	LM158	$T_A = -55^\circ\text{C to }125^\circ\text{C}$	3	5	mV	
					7			
			LM158A	$T_A = -55^\circ\text{C to }125^\circ\text{C}$		2		
					4			
$dV_{OS}/dT$	Input offset voltage drift		LM158	$T_A = -55^\circ\text{C to }125^\circ\text{C}$	7		$\mu\text{V}/^\circ\text{C}$	
			LM158A	$T_A = -55^\circ\text{C to }125^\circ\text{C}$	7	15 <sup>(3)</sup>		
PSRR	Input offset voltage vs power supply ( $\Delta V_{IO}/\Delta V_S$ )	$V_S = 5\text{ V to }30\text{ V}$			65	100	dB	
$V_{O1}/V_{O2}$	Channel separation	$f = 1\text{ kHz to }20\text{ kHz}$				120	dB	
<b>INPUT VOLTAGE RANGE</b>								
$V_{CM}$	Common-mode voltage range	$V_S = 5\text{ V to }30\text{ V}$	LM158		(V-)	(V+) - 1.5	V	
		$V_S = 30\text{ V}$	LM158A					
		$V_S = 5\text{ V to }30\text{ V}$	LM158	$T_A = -55^\circ\text{C to }125^\circ\text{C}$	(V-)	(V+) - 2		
		$V_S = 30\text{ V}$	LM158A					
CMRR	Common-mode rejection ratio	$V_S = 5\text{ V to }30\text{ V}$ ; $V_{CM} = 0\text{ V}$			70	80	dB	
<b>INPUT BIAS CURRENT</b>								
$I_B$	Input bias current	$V_O = 1.4\text{ V}$	LM158	$T_A = -55^\circ\text{C to }125^\circ\text{C}$	-20	-150	nA	
					-300			
			LM158A	$T_A = -55^\circ\text{C to }125^\circ\text{C}$	-15	-50		
					-100			
$I_{OS}$	Input offset current	$V_O = 1.4\text{ V}$	LM158	$T_A = -55^\circ\text{C to }125^\circ\text{C}$	2	30	nA	
					100			
			LM158A	$T_A = -55^\circ\text{C to }125^\circ\text{C}$	2	10		
					30			
$dI_{OS}/dT$	Input offset current drift				10		$\text{pA}/^\circ\text{C}$	
			LM158A	$T_A = -55^\circ\text{C to }125^\circ\text{C}$		200		
<b>NOISE</b>								
$e_n$	Input voltage noise density	$f = 1\text{ kHz}$			40		$\text{nV}/\sqrt{\text{Hz}}$	
<b>OPEN-LOOP GAIN</b>								
$A_{OL}$	Open-loop voltage gain	$V_S = 15\text{ V}$ ; $V_O = 1\text{ V to }11\text{ V}$ ; $R_L \geq 2\text{ k}\Omega$			50	100	V/mV	
				$T_A = -55^\circ\text{C to }125^\circ\text{C}$	25			
<b>FREQUENCY RESPONSE</b>								
GBW	Gain bandwidth product				0.7		MHz	
SR	Slew rate	$G = +1$			0.3		V/ $\mu\text{s}$	
<b>OUTPUT</b>								
$V_O$	Voltage output swing from rail	Positive rail	$V_S = 30\text{ V}$ ; $R_L = 2\text{ k}\Omega$	$T_A = -55^\circ\text{C to }125^\circ\text{C}$		4	V	
			$V_S = 30\text{ V}$ ; $R_L \geq 10\text{ k}\Omega$		2	3		
		Negative rail	$V_S = 5\text{ V}$ ; $R_L \geq 2\text{ k}\Omega$		1.5			
			$V_S = 5\text{ V}$ ; $R_L \leq 10\text{ k}\Omega$	$T_A = -55^\circ\text{C to }125^\circ\text{C}$	5	20		
$I_O$	Output current	$V_S = 15\text{ V}$ ; $V_O = 0\text{ V}$ ; $V_{ID} = 1\text{ V}$	Source	LM158A		-20	-30	mA
					$T_A = -55^\circ\text{C to }125^\circ\text{C}$	-10		
		$V_S = 15\text{ V}$ ; $V_O = 15\text{ V}$ ; $V_{ID} = -1\text{ V}$	Sink		10	20		
				$T_A = -55^\circ\text{C to }125^\circ\text{C}$	5			
	$V_{ID} = -1\text{ V}$ ; $V_O = 200\text{ mV}$		12	30	$\mu\text{A}$			
$I_{SC}$	Short-circuit current	$V_S = 10\text{ V}$ ; $V_O = V_S/2$			$\pm 40$	$\pm 60$	mA	
<b>POWER SUPPLY</b>								
$I_Q$	Quiescent current per amplifier	$V_O = 2.5\text{ V}$ ; $I_O = 0\text{ A}$	$T_A = -55^\circ\text{C to }125^\circ\text{C}$		350	600	$\mu\text{A}$	
		$V_S = 30\text{ V}$ ; $V_O = 15\text{ V}$ ; $I_O = 0\text{ A}$			500	1000		

- All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. Maximum  $V_S$  for testing purposes is 30 V for LM158 and LM158A.
- All typical values are  $T_A = 25^\circ\text{C}$ .
- On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 7.10 Electrical Characteristics: LM258, LM258A

 For  $V_S = (V_+) - (V_-) = 5\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ , (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP <sup>(2)</sup>	MAX	UNIT	
<b>OFFSET VOLTAGE</b>								
$V_{OS}$	Input offset voltage	$V_S = 5\text{ V to }30\text{ V}$ ; $V_{CM} = 0\text{ V}$ ; $V_O = 1.4\text{ V}$	LM258	$T_A = -25^\circ\text{C to }85^\circ\text{C}$	3	5	mV	
					7			
			LM258A	$T_A = -25^\circ\text{C to }85^\circ\text{C}$	2	3		
					4			
$dV_{OS}/dT$	Input offset voltage drift		LM258	$T_A = -25^\circ\text{C to }85^\circ\text{C}$	7		$\mu\text{V}/^\circ\text{C}$	
					LM258A	7		15
PSRR	Input offset voltage vs power supply ( $\Delta V_{IO}/\Delta V_S$ )	$V_S = 5\text{ V to }30\text{ V}$			65	100	dB	
$V_{O1}/V_{O2}$	Channel separation	$f = 1\text{ kHz to }20\text{ kHz}$				120	dB	
<b>INPUT VOLTAGE RANGE</b>								
$V_{CM}$	Common-mode voltage range	$V_S = 5\text{ V to }30\text{ V}$	LM258		(V-)	(V+) - 1.5	V	
		$V_S = 30\text{ V}$	LM258A					
		$V_S = 5\text{ V to }30\text{ V}$	LM258	$T_A = -25^\circ\text{C to }85^\circ\text{C}$	(V-)	(V+) - 2		
		$V_S = 30\text{ V}$	LM258A					
CMRR	Common-mode rejection ratio	$V_S = 5\text{ V to }30\text{ V}$ ; $V_{CM} = 0\text{ V}$			70	80	dB	
<b>INPUT BIAS CURRENT</b>								
$I_B$	Input bias current	$V_O = 1.4\text{ V}$	LM258	$T_A = -25^\circ\text{C to }85^\circ\text{C}$	-20	-150	nA	
					-300			
			LM258A	$T_A = -25^\circ\text{C to }85^\circ\text{C}$	-15	-80		
					-100			
$I_{OS}$	Input offset current	$V_O = 1.4\text{ V}$	LM258	$T_A = -25^\circ\text{C to }85^\circ\text{C}$	2	30	nA	
					100			
			LM258A	$T_A = -25^\circ\text{C to }85^\circ\text{C}$	2	15		
					30			
$dI_{OS}/dT$	Input offset current drift		LM258A	$T_A = -25^\circ\text{C to }85^\circ\text{C}$	10		$\text{pA}/^\circ\text{C}$	
					200			
<b>NOISE</b>								
$e_n$	Input voltage noise density	$f = 1\text{ kHz}$			40		$\text{nV}/\sqrt{\text{Hz}}$	
<b>OPEN-LOOP GAIN</b>								
$A_{OL}$	Open-loop voltage gain	$V_S = 15\text{ V}$ ; $V_O = 1\text{ V to }11\text{ V}$ ; $R_L \geq 2\text{ k}\Omega$			50	100	V/mV	
				$T_A = -25^\circ\text{C to }85^\circ\text{C}$	25			
<b>FREQUENCY RESPONSE</b>								
GBW	Gain bandwidth product				0.7		MHz	
SR	Slew rate	$G = +1$			0.3		V/ $\mu\text{s}$	
<b>OUTPUT</b>								
$V_O$	Voltage output swing from rail	Positive rail	$V_S = 30\text{ V}$ ; $R_L = 2\text{ k}\Omega$	$T_A = -25^\circ\text{C to }85^\circ\text{C}$		4	V	
			$V_S = 30\text{ V}$ ; $R_L \geq 10\text{ k}\Omega$		2	3		
		Negative rail	$V_S = 5\text{ V}$ ; $R_L \geq 2\text{ k}\Omega$			1.5		
			$V_S = 5\text{ V}$ ; $R_L \leq 10\text{ k}\Omega$	$T_A = -25^\circ\text{C to }85^\circ\text{C}$	5	20		
$I_O$	Output current	$V_S = 15\text{ V}$ ; $V_O = 0\text{ V}$ ; $V_{ID} = 1\text{ V}$	Source	LM258A		-20	-30	mA
					$T_A = -25^\circ\text{C to }85^\circ\text{C}$	-10		
		$V_S = 15\text{ V}$ ; $V_O = 15\text{ V}$ ; $V_{ID} = -1\text{ V}$	Sink			10	20	
					$T_A = -25^\circ\text{C to }85^\circ\text{C}$	5		
	$V_{ID} = -1\text{ V}$ ; $V_O = 200\text{ mV}$			12	30	$\mu\text{A}$		
$I_{SC}$	Short-circuit current	$V_S = 10\text{ V}$ ; $V_O = V_S/2$				$\pm 40$	$\pm 60$	mA
<b>POWER SUPPLY</b>								
$I_Q$	Quiescent current per amplifier	$V_O = 2.5\text{ V}$ ; $I_O = 0\text{ A}$	$T_A = -25^\circ\text{C to }85^\circ\text{C}$		350	600	$\mu\text{A}$	
		$V_S = 30\text{ V}$ ; $V_O = 15\text{ V}$ ; $I_O = 0\text{ A}$			500	1000		

- All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. Maximum  $V_S$  for testing purposes is 30 V for LM258 and LM258A.
- All typical values are  $T_A = 25^\circ\text{C}$ .

## 7.11 Typical Characteristics

Typical characteristics section is applicable for LM358B and LM2904B. The typical characteristics data section was taken with  $T_A = 25^\circ\text{C}$ ,  $V_S = 36\text{ V}$  ( $\pm 18\text{ V}$ ),  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$  (unless otherwise noted).

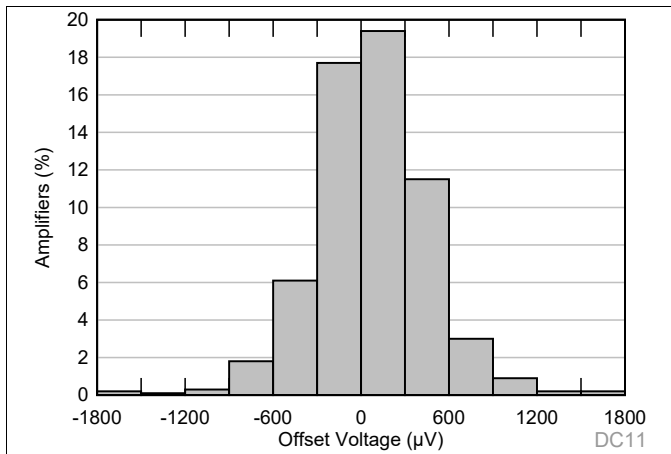


图 1. Offset Voltage Production Distribution

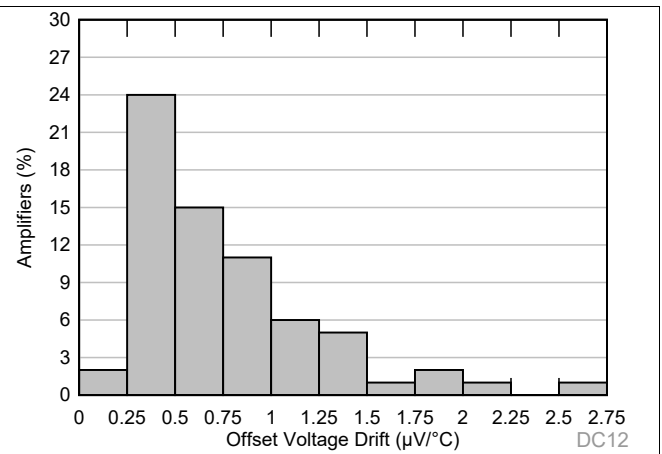


图 2. Offset Voltage Drift Distribution

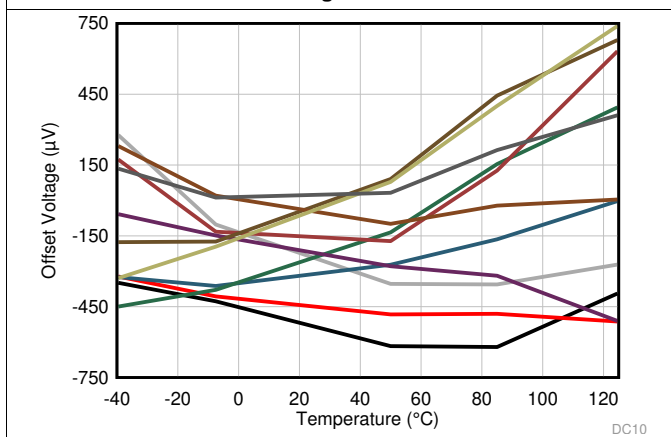


图 3. Offset Voltage vs Temperature

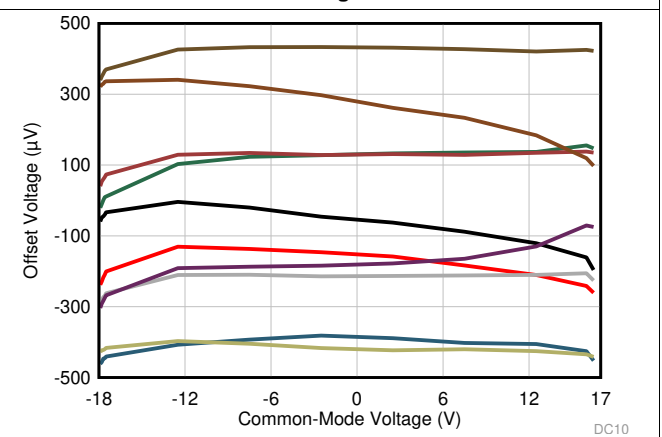


图 4. Offset Voltage vs Common-Mode Voltage

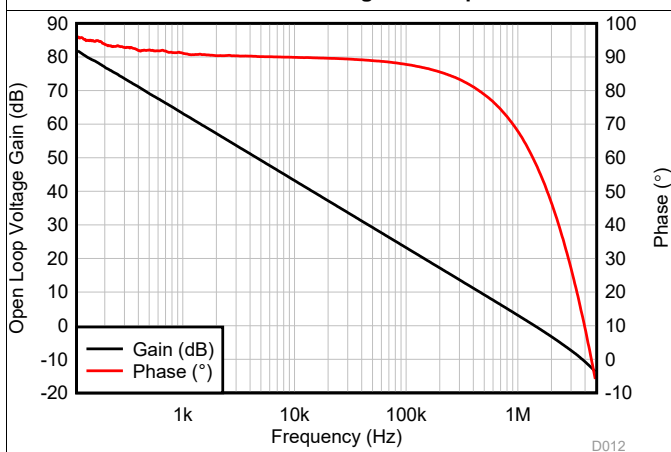


图 5. Open-Loop Gain and Phase vs Frequency

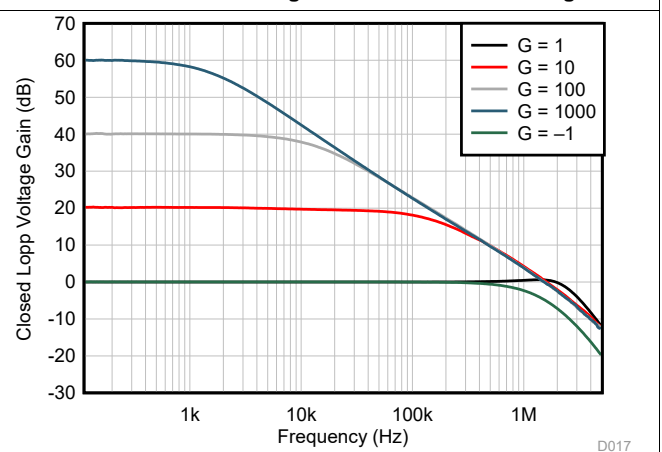


图 6. Closed-Loop Gain vs Frequency

Typical Characteristics (接下页)

Typical characteristics section is applicable for LM358B and LM2904B. The typical characteristics data section was taken with  $T_A = 25^\circ\text{C}$ ,  $V_S = 36\text{ V} (\pm 18\text{ V})$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$  (unless otherwise noted).

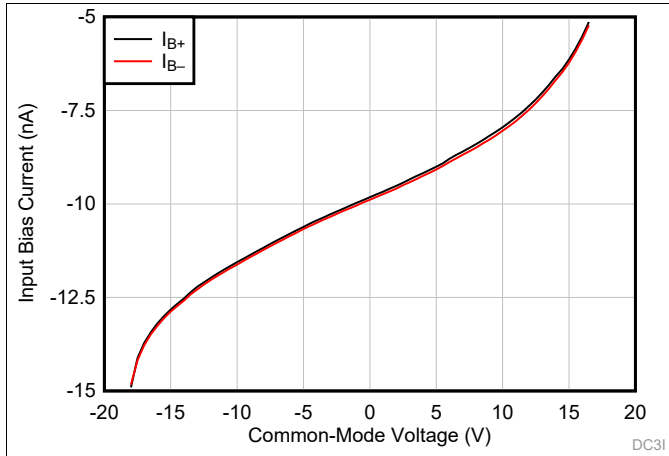


图 7. Input Bias Current vs Common-Mode Voltage

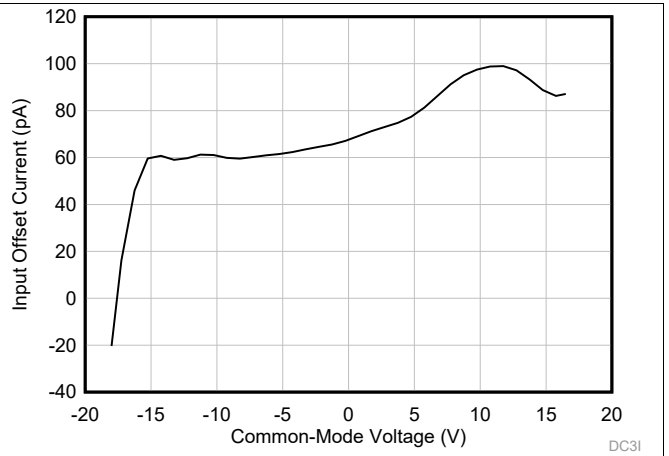


图 8. Input Offset Current vs Common-Mode Voltage

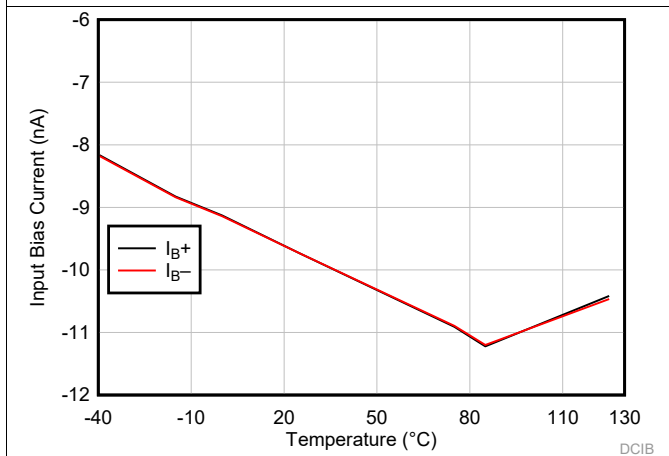


图 9. Input Bias Current vs Temperature

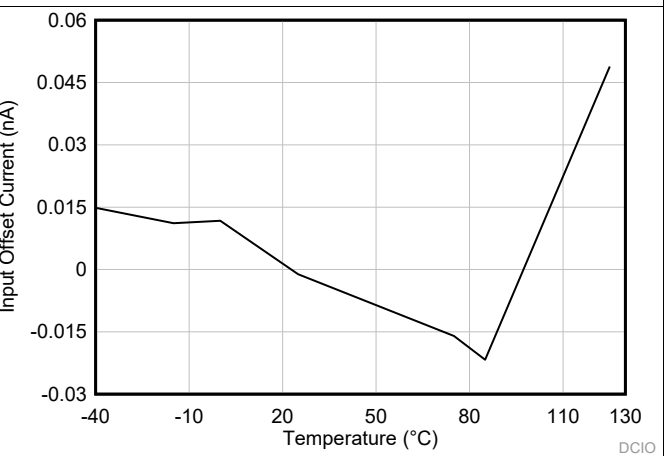


图 10. Input Offset Current vs Temperature

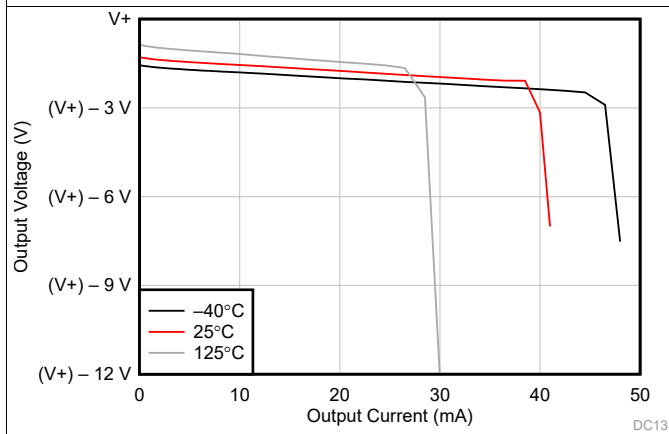


图 11. Output Voltage Swing vs Output Current (Sourcing)

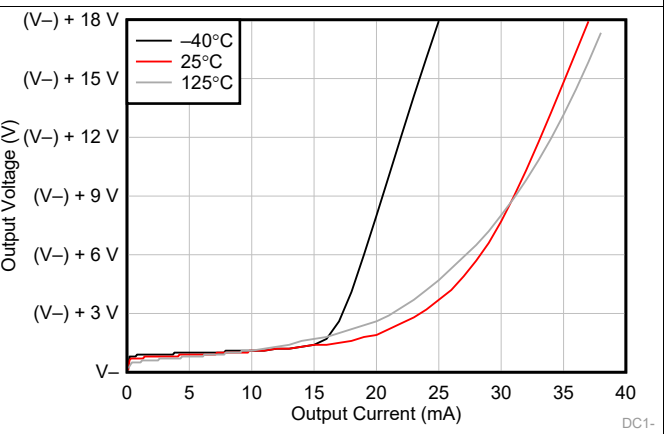
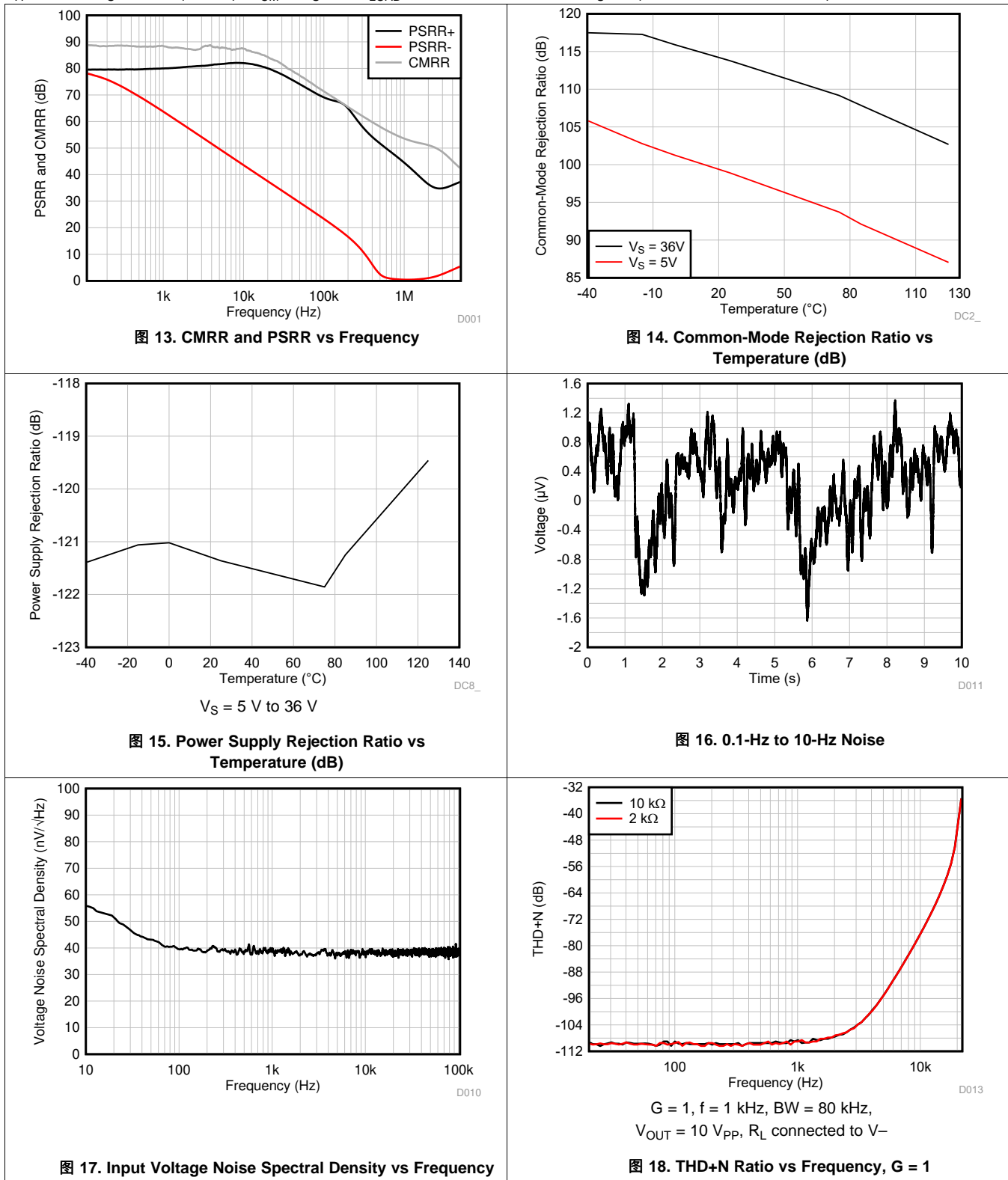


图 12. Output Voltage Swing vs Output Current (Sinking)

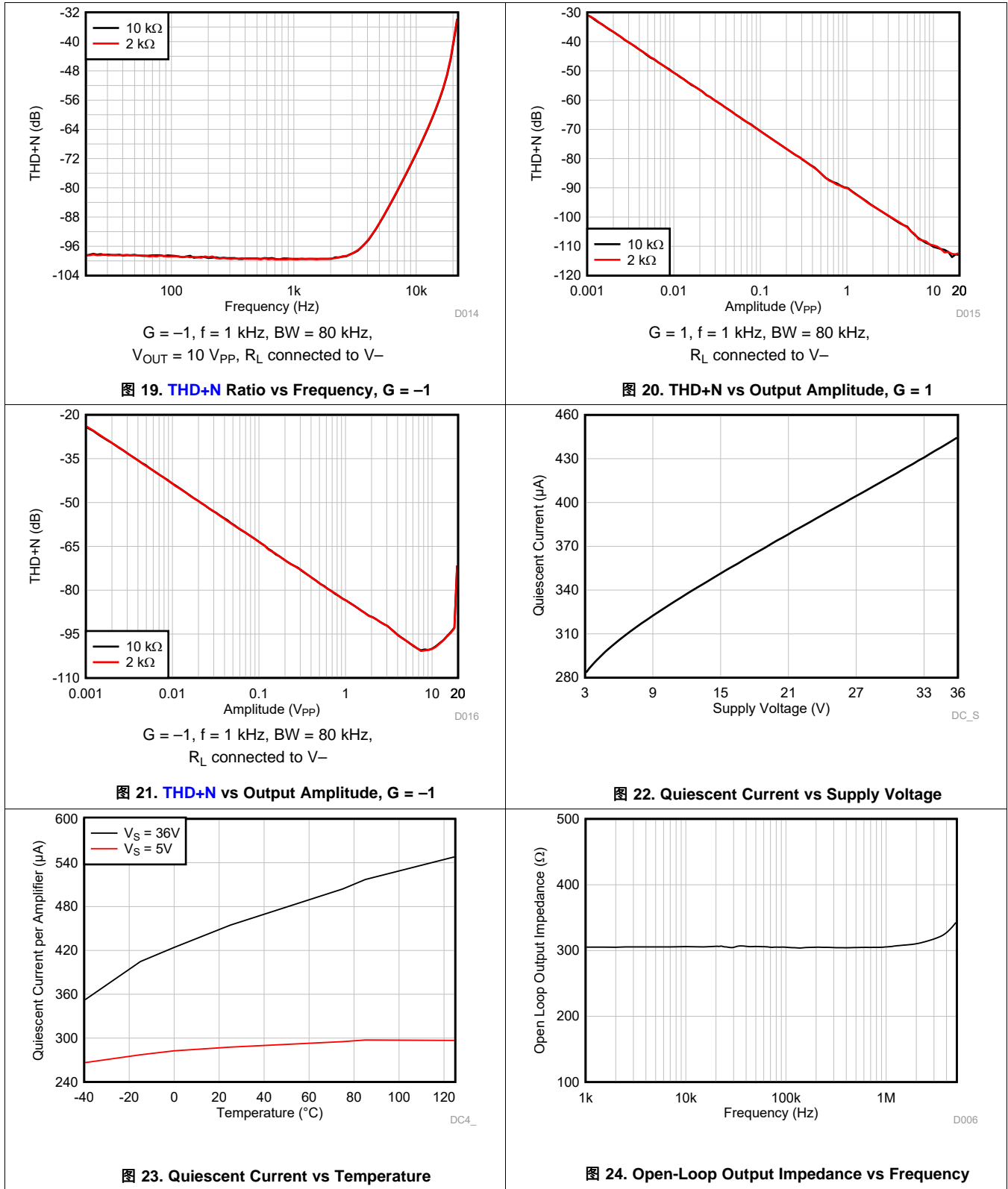
Typical Characteristics (接下页)

Typical characteristics section is applicable for LM358B and LM2904B. The typical characteristics data section was taken with  $T_A = 25^\circ\text{C}$ ,  $V_S = 36\text{ V}$  ( $\pm 18\text{ V}$ ),  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$  (unless otherwise noted).



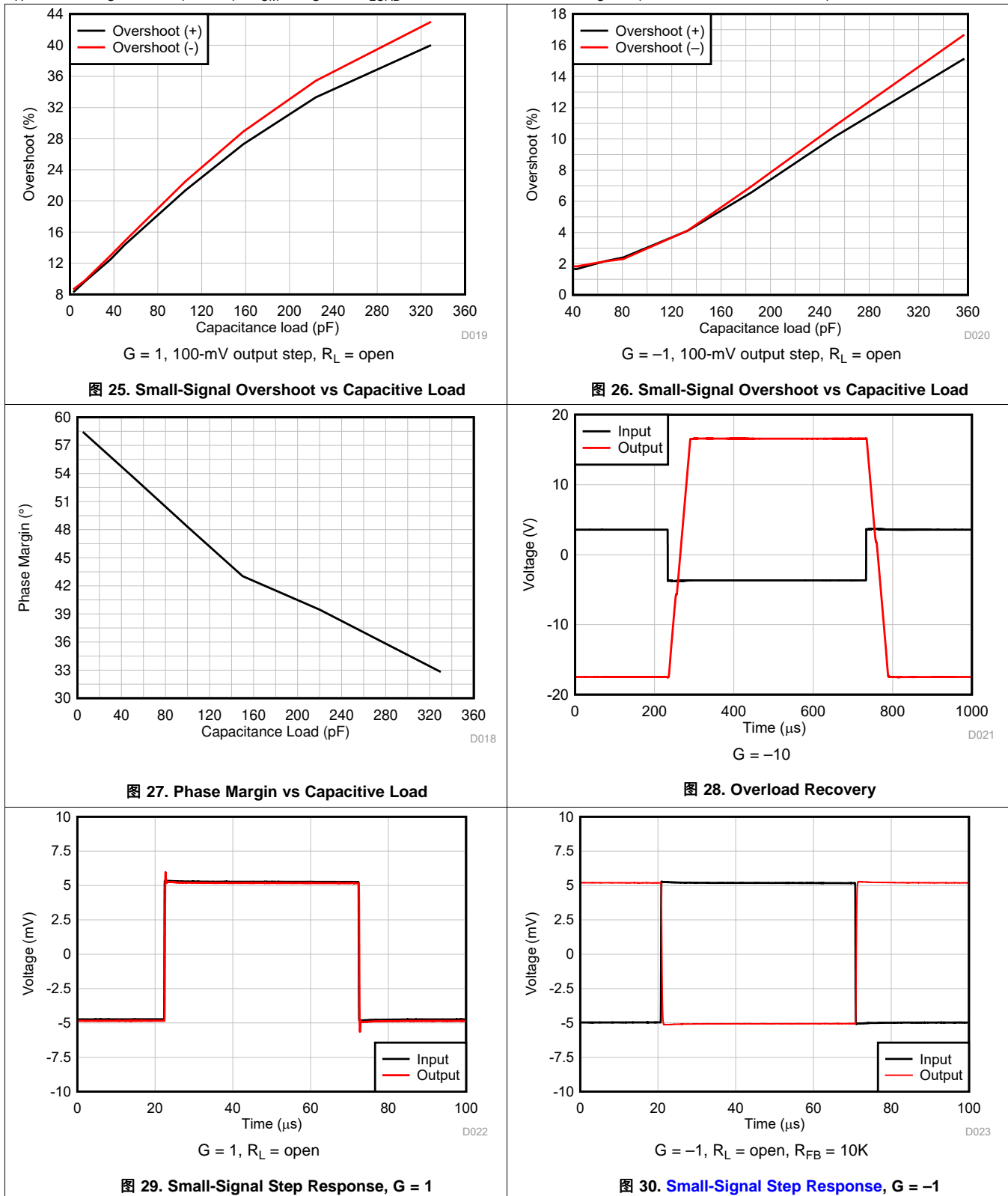
Typical Characteristics (接下页)

Typical characteristics section is applicable for LM358B and LM2904B. The typical characteristics data section was taken with  $T_A = 25^\circ\text{C}$ ,  $V_S = 36\text{ V}$  ( $\pm 18\text{ V}$ ),  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$  (unless otherwise noted).



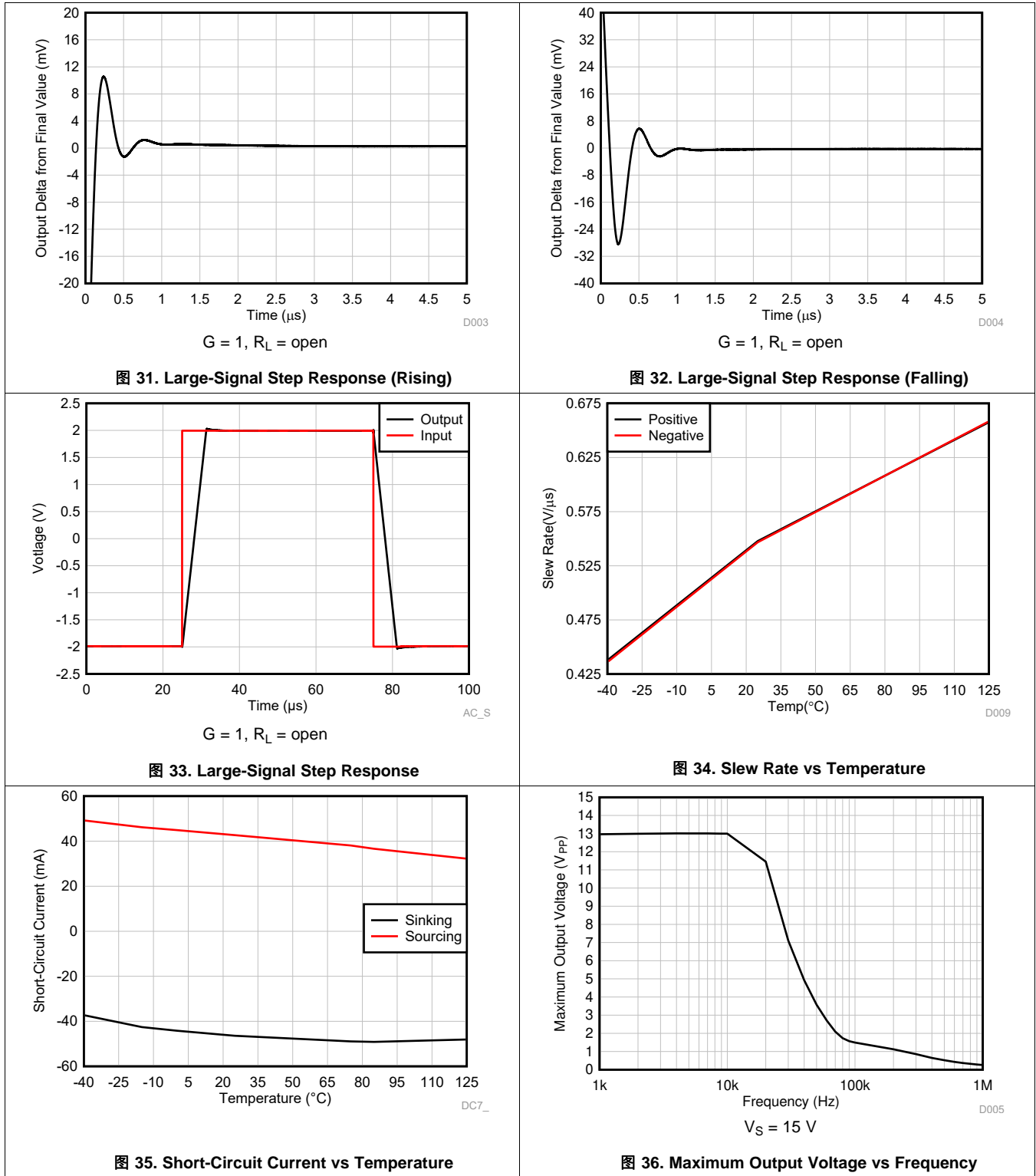
Typical Characteristics (接下页)

Typical characteristics section is applicable for LM358B and LM2904B. The typical characteristics data section was taken with  $T_A = 25^\circ\text{C}$ ,  $V_S = 36\text{ V} (\pm 18\text{ V})$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$  (unless otherwise noted).



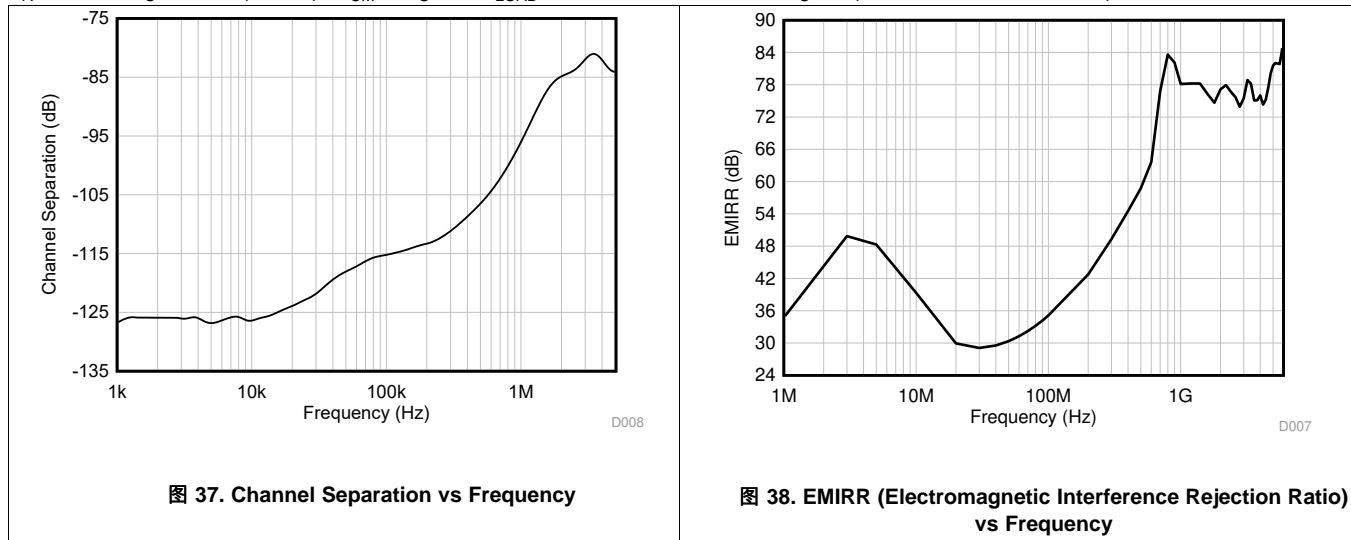
Typical Characteristics (接下页)

Typical characteristics section is applicable for LM358B and LM2904B. The typical characteristics data section was taken with  $T_A = 25^\circ\text{C}$ ,  $V_S = 36\text{ V} (\pm 18\text{ V})$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$  (unless otherwise noted).



### Typical Characteristics (接下页)

Typical characteristics section is applicable for LM358B and LM2904B. The typical characteristics data section was taken with  $T_A = 25^\circ\text{C}$ ,  $V_S = 36\text{ V} (\pm 18\text{ V})$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$  (unless otherwise noted).



### 7.12 Typical Characteristics

Typical characteristics section is applicable for LM158, LM158A, LM258, LM258A, LM358, LM358A, LM2904, and LM2904V.

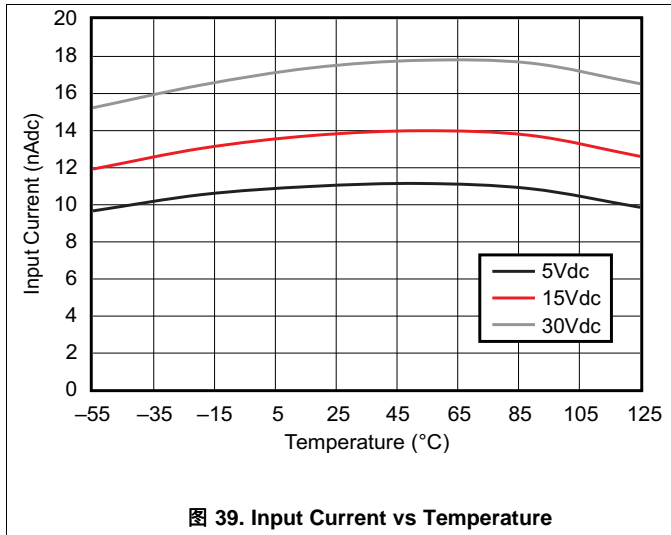


图 39. Input Current vs Temperature

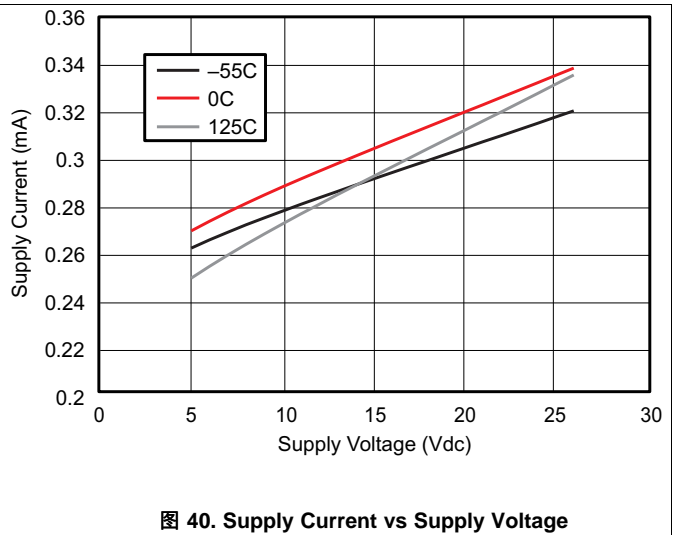


图 40. Supply Current vs Supply Voltage

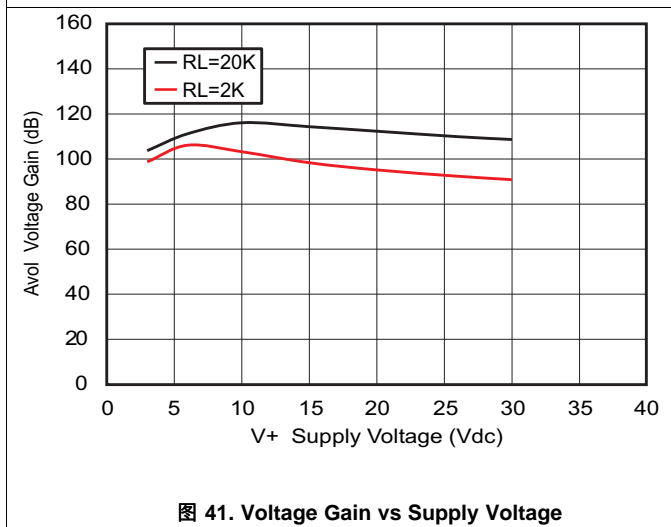


图 41. Voltage Gain vs Supply Voltage

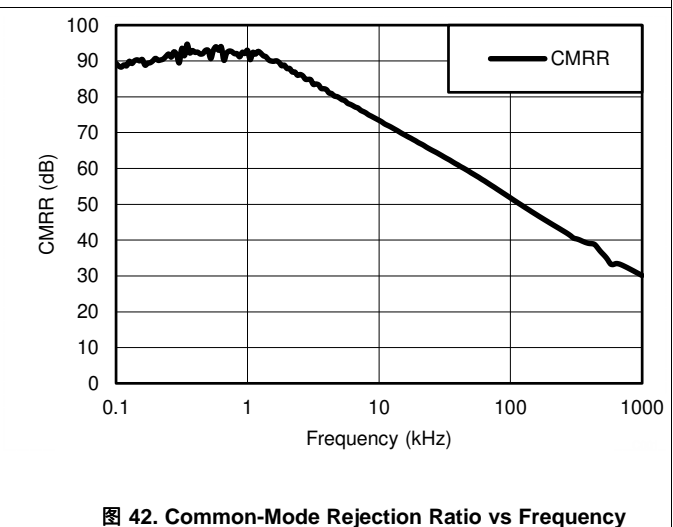


图 42. Common-Mode Rejection Ratio vs Frequency

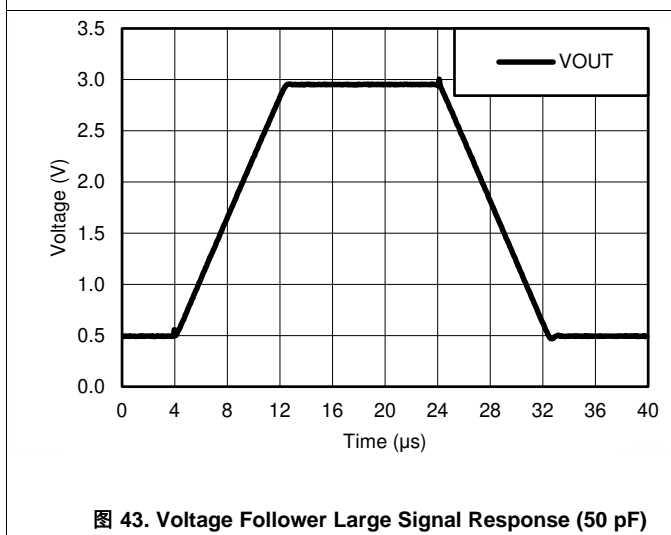


图 43. Voltage Follower Large Signal Response (50 pF)

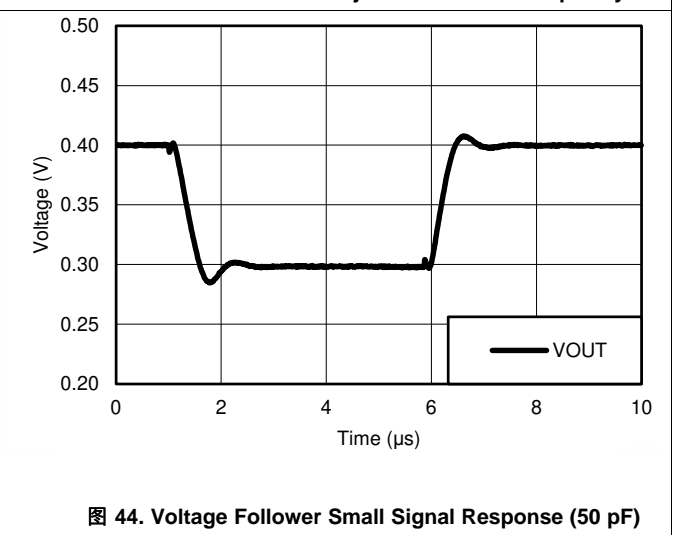


图 44. Voltage Follower Small Signal Response (50 pF)

**Typical Characteristics (接下页)**

Typical characteristics section is applicable for LM158, LM158A, LM258, LM258A, LM358, LM358A, LM2904, and LM2904V.

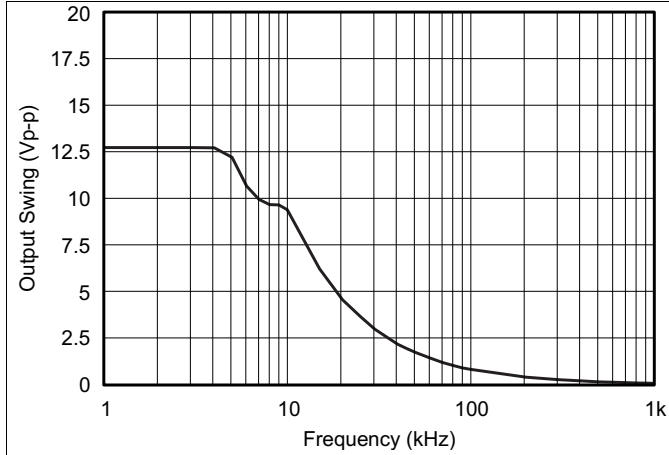


图 45. Maximum Output Swing vs Frequency  
 ( $V_{CC} = 15\text{ V}$ )

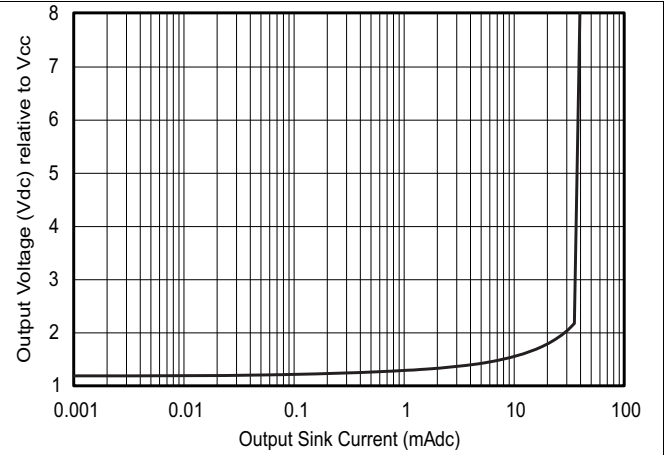


图 46. Output Sourcing Characteristics

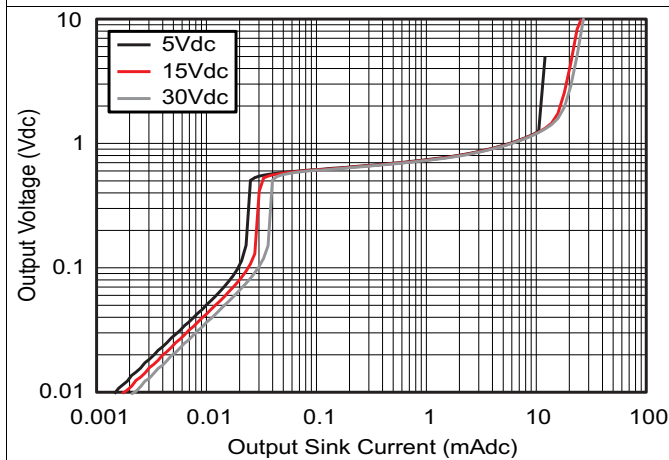


图 47. Output Sinking Characteristics

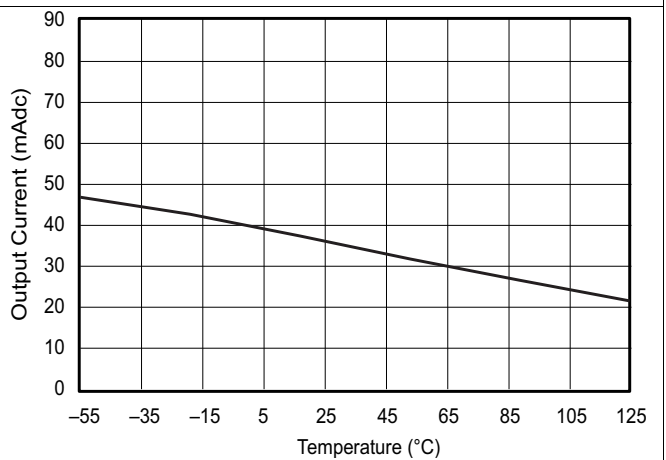


图 48. Source Current Limiting

## 8 Parameter Measurement Information

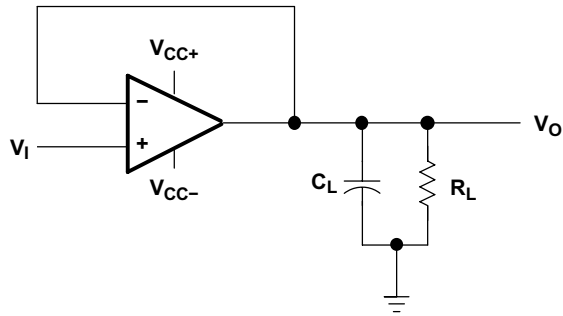


图 49. Unity-Gain Amplifier

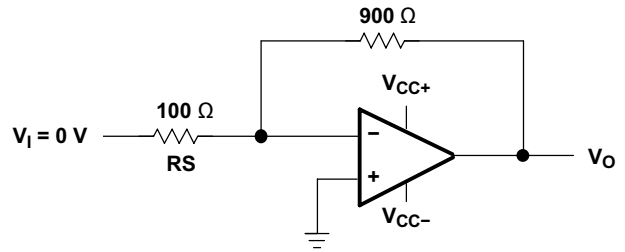


图 50. Noise-Test Circuit

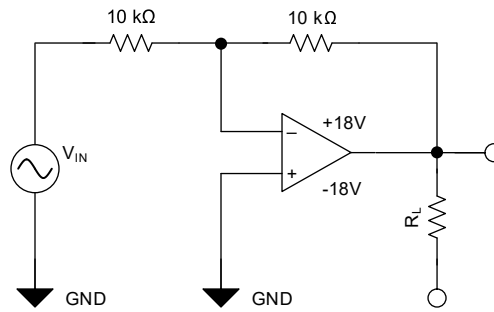


图 51. Test Circuit,  $G = -1$ , for THD+N and Small-Signal Step Response

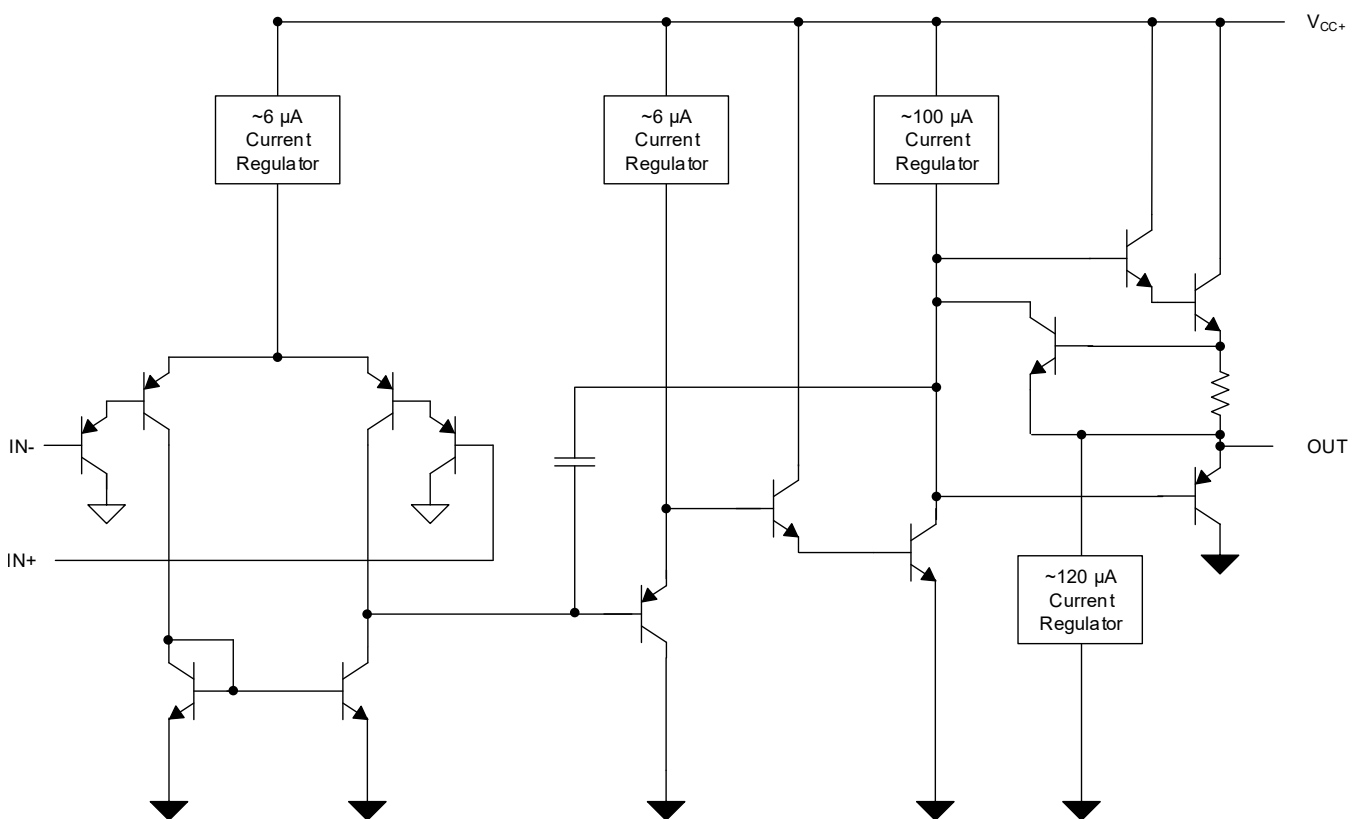
## 9 Detailed Description

### 9.1 Overview

These devices consist of two independent, high-gain frequency-compensated operational amplifiers designed to operate from a single supply over a wide range of voltages. Operation from split supplies also is possible if the difference between the two supplies is within the supply voltage range specified in the [Recommended Operating Conditions](#) section, and  $V_S$  is at least 1.5 V more positive than the input common-mode voltage. The low supply-current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, dc amplification blocks, and all the conventional operational amplifier circuits that now can be implemented more easily in single-supply-voltage systems. For example, these devices can be operated directly from the standard 5-V supply used in digital systems and easily can provide the required interface electronics without additional  $\pm 5$ -V supplies.

### 9.2 Functional Block Diagram - LM358B, LM358BA, LM2904B, LM2904BA



## 9.3 Feature Description

### 9.3.1 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. These devices have a 1.2-MHz unity-gain bandwidth (B Version).

### 9.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 0.5-V/ $\mu$ s slew rate (B Version).

### 9.3.3 Input Common Mode Range

The valid common mode range is from device ground to  $V_S - 1.5$  V ( $V_S - 2$  V across temperature). Inputs may exceed  $V_S$  up to the maximum  $V_S$  without device damage. At least one input must be in the valid input common-mode range for the output to be the correct phase. If both inputs exceed the valid range, then the output phase is undefined. If either input more than 0.3 V below  $V_-$  then input current should be limited to 1 mA and the output phase is undefined.

## 9.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single-supply operational amplifier or dual-supply amplifier, depending on the application.

## 10 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The LMx58 and LM2904 operational amplifiers are useful in a wide range of signal conditioning applications. Inputs can be powered before  $V_S$  for flexibility in multiple supply circuits.

### 10.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

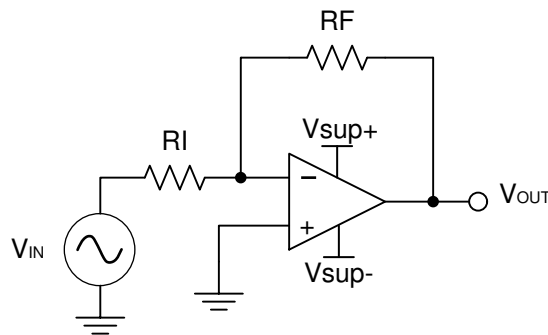


图 52. Application Schematic

#### 10.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application scales a signal of  $\pm 0.5$  V to  $\pm 1.8$  V. Setting the supply at  $\pm 12$  V is sufficient to accommodate this application.

#### 10.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using [公式 1](#) and [公式 2](#):

$$A_V = \frac{V_{OUT}}{V_{IN}} \tag{1}$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \tag{2}$$

Once the desired gain is determined, choose a value for  $R_I$  or  $R_F$ . [Subscripts should be fixed in the accompanying figures and equations also.] Choosing a value in the kilohm range is desirable because the amplifier circuit uses currents in the milliampere range. This ensures the part does not draw too much current. This example uses 10 k $\Omega$  for  $R_I$  which means 36 k $\Omega$  is used for  $R_F$ . This was determined by [公式 3](#).

$$A_V = -\frac{R_F}{R_I} \tag{3}$$

## Typical Application (接下页)

### 10.2.3 Application Curve

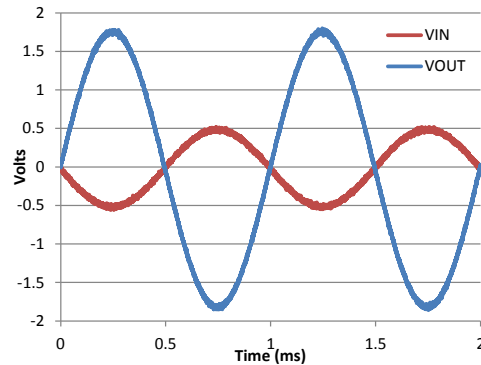


图 53. Input and Output Voltages of the Inverting Amplifier

## 11 Power Supply Recommendations

### CAUTION

Supply voltages larger than specified in the recommended operating region can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1- $\mu$ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the [Layout](#) section.

## 12 Layout

### 12.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace. [Things in parallel never cross, by definition]
- Place the external components as close to the device as possible. Keeping  $R_F$  and  $R_G$  close to the inverting input minimizes parasitic capacitance, as shown in [Layout Examples](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

## 12.2 Layout Examples

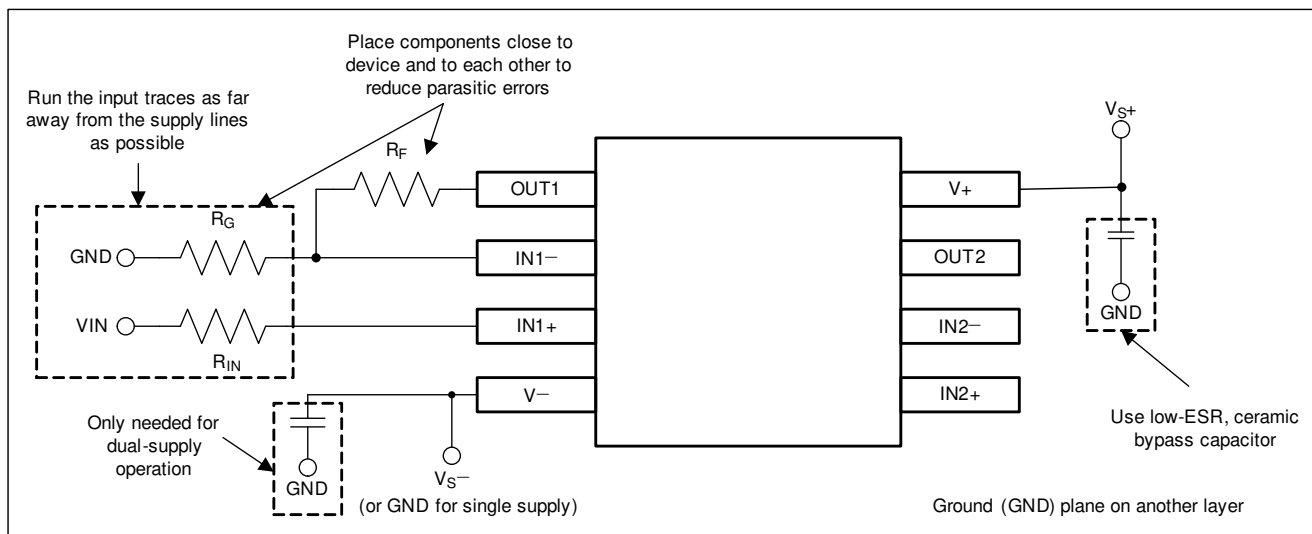


图 54. Operational Amplifier Board Layout for Noninverting Configuration

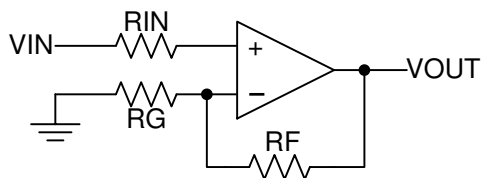


图 55. Operational Amplifier Schematic for Noninverting Configuration

## 13 器件和文档支持

### 13.1 文档支持

#### 13.1.1 相关文档

- 德州仪器 (TI), 《电路板布局技巧》。

### 13.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即订购快速访问。

表 1. 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
LM158	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>
LM158A	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>
LM258	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>
LM258A	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>
LM358	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>
LM358A	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>
LM358B中为 LM358B 和 LM2904B 器件添 加了预览标识	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>
LM2904	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>
LM2904B	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>
LM2904V	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>

### 13.3 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。单击右上角的 [通知我进行注册](#)，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 13.4 社区资源

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 13.5 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 13.6 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 13.7 术语表

[SLYZ022 - TI 术语表](#)。

本术语表列出并解释了术语、首字母缩略词和定义。

## 14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。数据如有变更，恕不另行通知和修订此文档。如需获取此数据表的浏览器版本，请查看左侧的导航面板。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87710012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87710012A LM158FKB	<a href="#">Samples</a>
5962-8771001PA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8771001PA LM158	<a href="#">Samples</a>
5962-87710022A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87710022A LM158AFKB	<a href="#">Samples</a>
5962-8771002PA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8771002PA LM158A	<a href="#">Samples</a>
LM158 MW8	ACTIVE	WAFERSALE	YS	0	1	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125		<a href="#">Samples</a>
LM158AFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87710022A LM158AFKB	<a href="#">Samples</a>
LM158AJG	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM158AJG	<a href="#">Samples</a>
LM158AJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8771002PA LM158A	<a href="#">Samples</a>
LM158FKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87710012A LM158FKB	<a href="#">Samples</a>
LM158JG	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM158JG	<a href="#">Samples</a>
LM158JGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8771001PA LM158	<a href="#">Samples</a>
LM258AD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258A	
LM258ADGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-25 to 85	(M3L, M3P, M3S, M3U)	<a href="#">Samples</a>
LM258ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-25 to 85	LM258A	<a href="#">Samples</a>
LM258ADRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258A	<a href="#">Samples</a>
LM258ADRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM258AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU   SN	N / A for Pkg Type	-25 to 85	LM258AP	<a href="#">Samples</a>
LM258APE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	LM258AP	<a href="#">Samples</a>
LM258D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258	
LM258DG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258	
LM258DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-25 to 85	(M2L, M2P, M2S, M2U)	<a href="#">Samples</a>
LM258DGKRG4	LIFEBUY	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-25 to 85		
LM258DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-25 to 85	LM258	<a href="#">Samples</a>
LM258DRG3	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-25 to 85	LM258	<a href="#">Samples</a>
LM258DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM258	<a href="#">Samples</a>
LM258P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU   SN	N / A for Pkg Type	-25 to 85	LM258P	<a href="#">Samples</a>
LM258PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	LM258P	<a href="#">Samples</a>
LM2904AVQDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	<a href="#">Samples</a>
LM2904AVQDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	<a href="#">Samples</a>
LM2904AVQPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	<a href="#">Samples</a>
LM2904AVQPWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904AV	<a href="#">Samples</a>
LM2904BAIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2904BA	<a href="#">Samples</a>
LM2904BIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28BB	<a href="#">Samples</a>
LM2904BIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	L2904B	<a href="#">Samples</a>
LM2904BIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904B	<a href="#">Samples</a>
LM2904D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	
LM2904DE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	<a href="#">Samples</a>
LM2904DG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2904DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(MBL, MBP, MBS, MB U)	<a href="#">Samples</a>
LM2904DGKRG4	LIFEBUY	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(MBL, MBP, MBS, MB U)	
LM2904DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	LM2904	<a href="#">Samples</a>
LM2904DRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	<a href="#">Samples</a>
LM2904DRG3	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM2904	<a href="#">Samples</a>
LM2904DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2904	<a href="#">Samples</a>
LM2904P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU   SN	N / A for Pkg Type	-40 to 125	LM2904P	<a href="#">Samples</a>
LM2904PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	LM2904P	<a href="#">Samples</a>
LM2904PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904	<a href="#">Samples</a>
LM2904PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904	<a href="#">Samples</a>
LM2904PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	L2904	<a href="#">Samples</a>
LM2904PWRG3	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L2904	<a href="#">Samples</a>
LM2904PWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904	<a href="#">Samples</a>
LM2904PWRG4-JF	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904	<a href="#">Samples</a>
LM2904QDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904Q1	<a href="#">Samples</a>
LM2904QDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2904Q1	<a href="#">Samples</a>
LM2904VQDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	<a href="#">Samples</a>
LM2904VQDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	<a href="#">Samples</a>
LM2904VQPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	<a href="#">Samples</a>
LM2904VQPWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904V	<a href="#">Samples</a>
LM358AD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM358ADE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	<a href="#">Samples</a>
LM358ADG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	
LM358ADGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(M6L, M6P, M6S, M6U)	<a href="#">Samples</a>
LM358ADGKRG4	LIFEBUY	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	0 to 70		
LM358ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	0 to 70	LM358A	<a href="#">Samples</a>
LM358ADRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358A	<a href="#">Samples</a>
LM358AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU   SN	N / A for Pkg Type	0 to 70	LM358AP	<a href="#">Samples</a>
LM358APE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM358AP	<a href="#">Samples</a>
LM358APW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L358A	<a href="#">Samples</a>
LM358APWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	0 to 70	L358A	<a href="#">Samples</a>
LM358APWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L358A	<a href="#">Samples</a>
LM358BAIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	L358BA	<a href="#">Samples</a>
LM358BIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	358B	<a href="#">Samples</a>
LM358BIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LM358B	<a href="#">Samples</a>
LM358BIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM358B	<a href="#">Samples</a>
LM358D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	
LM358D-JF	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	
LM358DG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	
LM358DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(M5L, M5P, M5S, M5U)	<a href="#">Samples</a>
LM358DGKRG4	LIFEBUY	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	(M5L, M5P, M5S, M5U)	
LM358DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	0 to 70	LM358	<a href="#">Samples</a>
LM358DRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM358DRG3	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	LM358	<a href="#">Samples</a>
LM358DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM358	<a href="#">Samples</a>
LM358P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU   SN	N / A for Pkg Type	0 to 70	LM358P	<a href="#">Samples</a>
LM358PE3	ACTIVE	PDIP	P	8	50	RoHS & Non-Green	SN	N / A for Pkg Type	0 to 70	LM358P	<a href="#">Samples</a>
LM358PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM358P	<a href="#">Samples</a>
LM358PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L358	<a href="#">Samples</a>
LM358PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L358	<a href="#">Samples</a>
LM358PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	0 to 70	L358	<a href="#">Samples</a>
LM358PWRG3	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	L358	<a href="#">Samples</a>
LM358PWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L358	<a href="#">Samples</a>
LM358PWRG4-JF	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L358	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

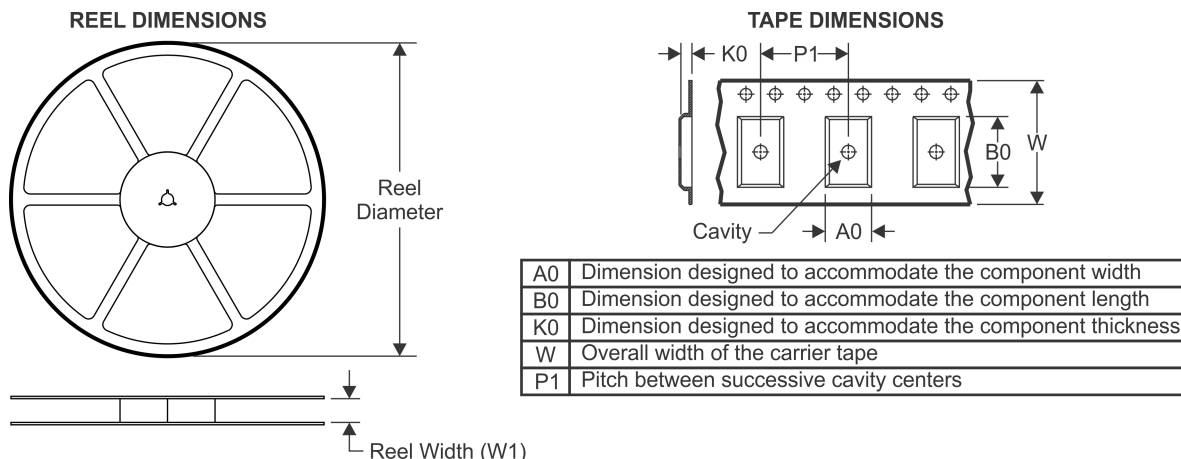
**OTHER QUALIFIED VERSIONS OF LM258A, LM2904, LM2904B :**

- Automotive : [LM2904-Q1](#), [LM2904B-Q1](#)
- Enhanced Product : [LM258A-EP](#), [LM2904-EP](#)

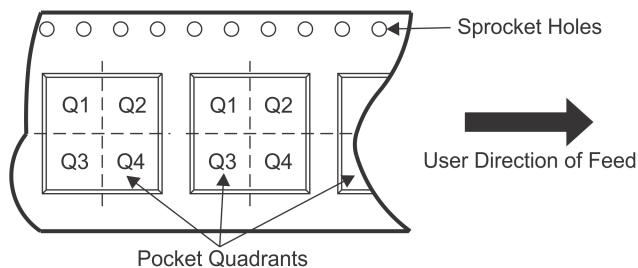
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

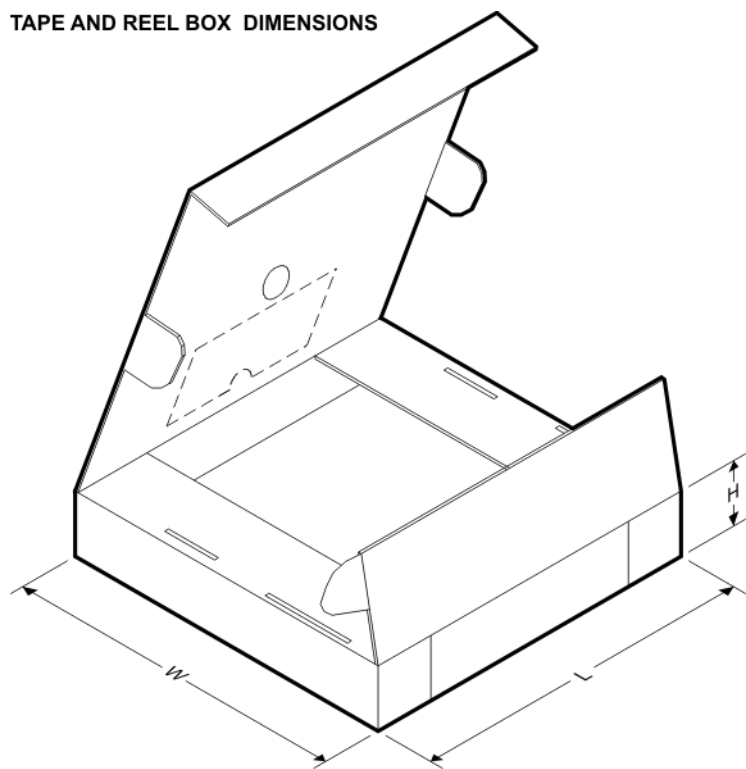


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM258ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM258ADR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM258DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM258DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG3	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM258DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQDRG4	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904AVQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904AVQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2904BAIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904BIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904BIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DRG3	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM2904PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904PWRG3	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904PWRG4-JF	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2904VQDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2904VQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2904VQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358APWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358BAIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358BIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358BIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM358DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM358DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM358DRG3	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM358DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM358PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM358PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358PWRG3	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM358PWRG4-JF	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM258ADGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM258ADR	SOIC	D	8	2500	364.0	364.0	27.0
LM258ADR	SOIC	D	8	2500	853.0	449.0	35.0
LM258ADR	SOIC	D	8	2500	340.5	336.1	25.0
LM258ADRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM258ADRG4	SOIC	D	8	2500	853.0	449.0	35.0
LM258DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM258DR	SOIC	D	8	2500	853.0	449.0	35.0
LM258DR	SOIC	D	8	2500	364.0	364.0	27.0

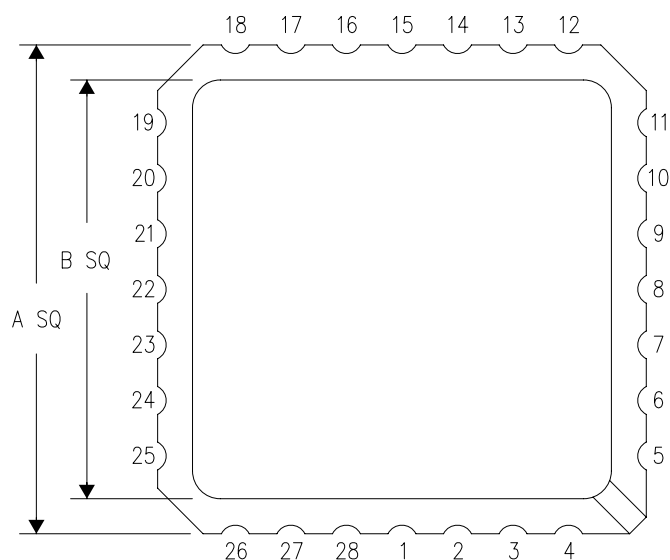
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM258DR	SOIC	D	8	2500	340.5	336.1	25.0
LM258DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM258DRG3	SOIC	D	8	2500	333.2	345.9	28.6
LM258DRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM258DRG4	SOIC	D	8	2500	853.0	449.0	35.0
LM2904AVQDR	SOIC	D	8	2500	340.5	336.1	25.0
LM2904AVQDRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM2904AVQPWR	TSSOP	PW	8	2000	853.0	449.0	35.0
LM2904AVQPWRG4	TSSOP	PW	8	2000	853.0	449.0	35.0
LM2904BAIDR	SOIC	D	8	2500	340.5	336.1	25.0
LM2904BIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2904BIDR	SOIC	D	8	2500	340.5	336.1	25.0
LM2904BIPWR	TSSOP	PW	8	2000	853.0	449.0	35.0
LM2904DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM2904DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LM2904DR	SOIC	D	8	2500	340.5	336.1	25.0
LM2904DR	SOIC	D	8	2500	853.0	449.0	35.0
LM2904DR	SOIC	D	8	2500	364.0	364.0	27.0
LM2904DRG3	SOIC	D	8	2500	333.2	345.9	28.6
LM2904DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM2904DRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM2904DRG4	SOIC	D	8	2500	853.0	449.0	35.0
LM2904PSR	SO	PS	8	2000	853.0	449.0	35.0
LM2904PWR	TSSOP	PW	8	2000	853.0	449.0	35.0
LM2904PWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM2904PWRG3	TSSOP	PW	8	2000	364.0	364.0	27.0
LM2904PWRG4	TSSOP	PW	8	2000	853.0	449.0	35.0
LM2904PWRG4-JF	TSSOP	PW	8	2000	853.0	449.0	35.0
LM2904QDR	SOIC	D	8	2500	350.0	350.0	43.0
LM2904VQDR	SOIC	D	8	2500	340.5	336.1	25.0
LM2904VQPWR	TSSOP	PW	8	2000	853.0	449.0	35.0
LM2904VQPWRG4	TSSOP	PW	8	2000	853.0	449.0	35.0
LM358ADGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM358ADR	SOIC	D	8	2500	340.5	336.1	25.0
LM358ADR	SOIC	D	8	2500	364.0	364.0	27.0
LM358ADR	SOIC	D	8	2500	853.0	449.0	35.0
LM358ADRG4	SOIC	D	8	2500	853.0	449.0	35.0
LM358ADRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM358APWR	TSSOP	PW	8	2000	853.0	449.0	35.0
LM358APWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM358APWRG4	TSSOP	PW	8	2000	853.0	449.0	35.0
LM358BAIDR	SOIC	D	8	2500	340.5	336.1	25.0
LM358BIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM358BIDR	SOIC	D	8	2500	340.5	336.1	25.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM358BIPWR	TSSOP	PW	8	2000	853.0	449.0	35.0
LM358DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LM358DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM358DR	SOIC	D	8	2500	364.0	364.0	27.0
LM358DR	SOIC	D	8	2500	853.0	449.0	35.0
LM358DR	SOIC	D	8	2500	340.5	336.1	25.0
LM358DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM358DRG3	SOIC	D	8	2500	333.2	345.9	28.6
LM358DRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM358DRG4	SOIC	D	8	2500	853.0	449.0	35.0
LM358PSR	SO	PS	8	2000	853.0	449.0	35.0
LM358PWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM358PWR	TSSOP	PW	8	2000	853.0	449.0	35.0
LM358PWRG3	TSSOP	PW	8	2000	364.0	364.0	27.0
LM358PWRG4	TSSOP	PW	8	2000	853.0	449.0	35.0
LM358PWRG4-JF	TSSOP	PW	8	2000	853.0	449.0	35.0

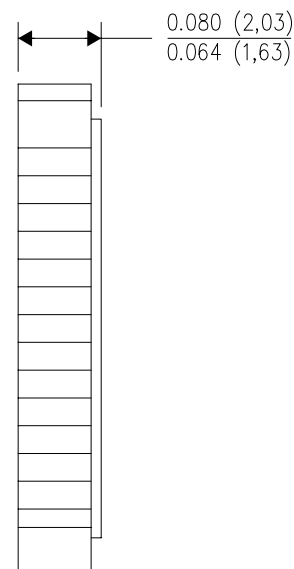
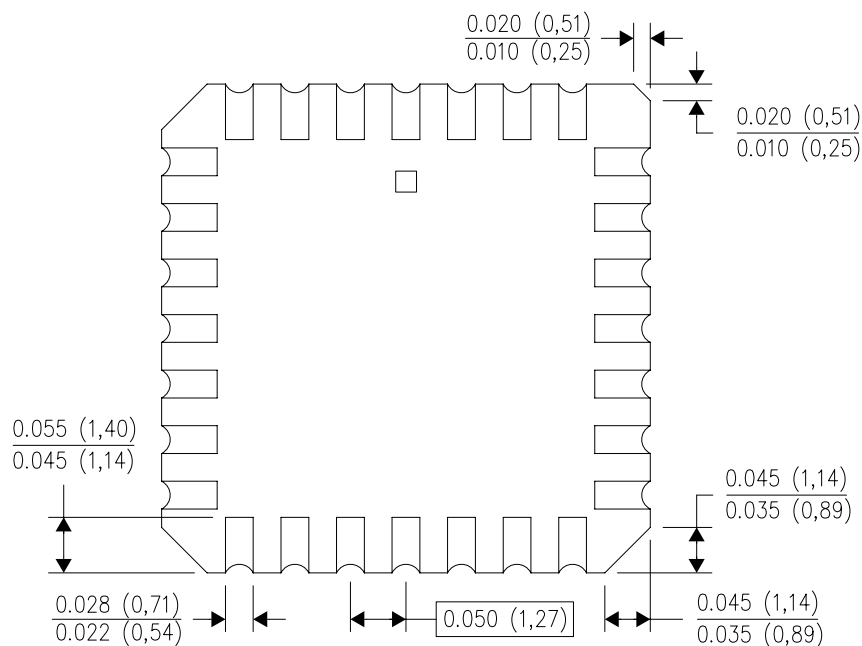
FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

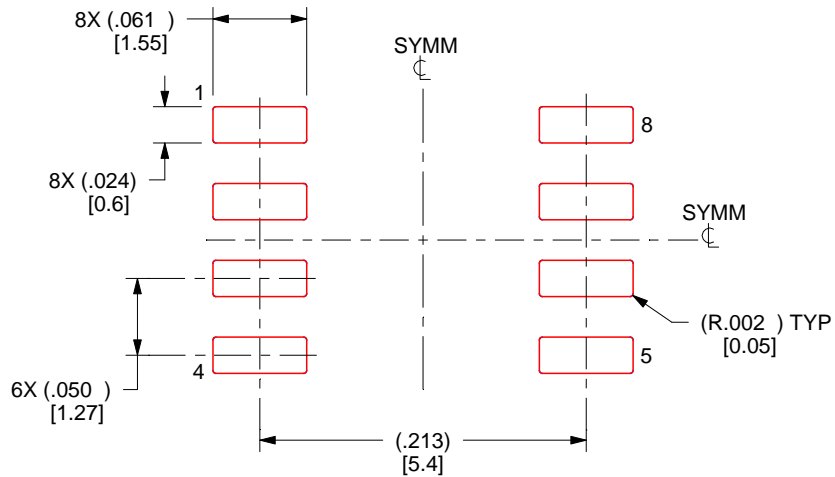
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

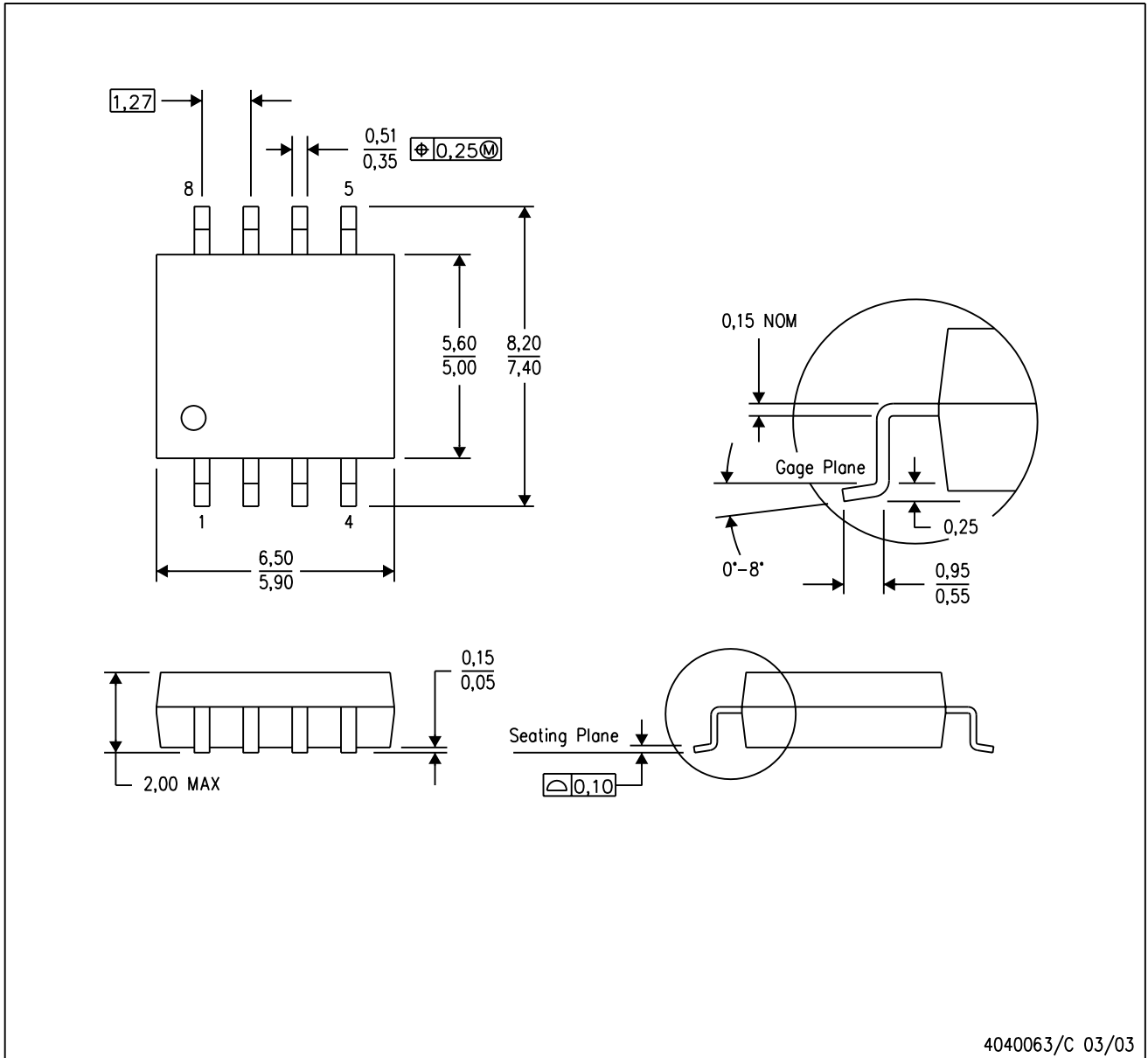
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

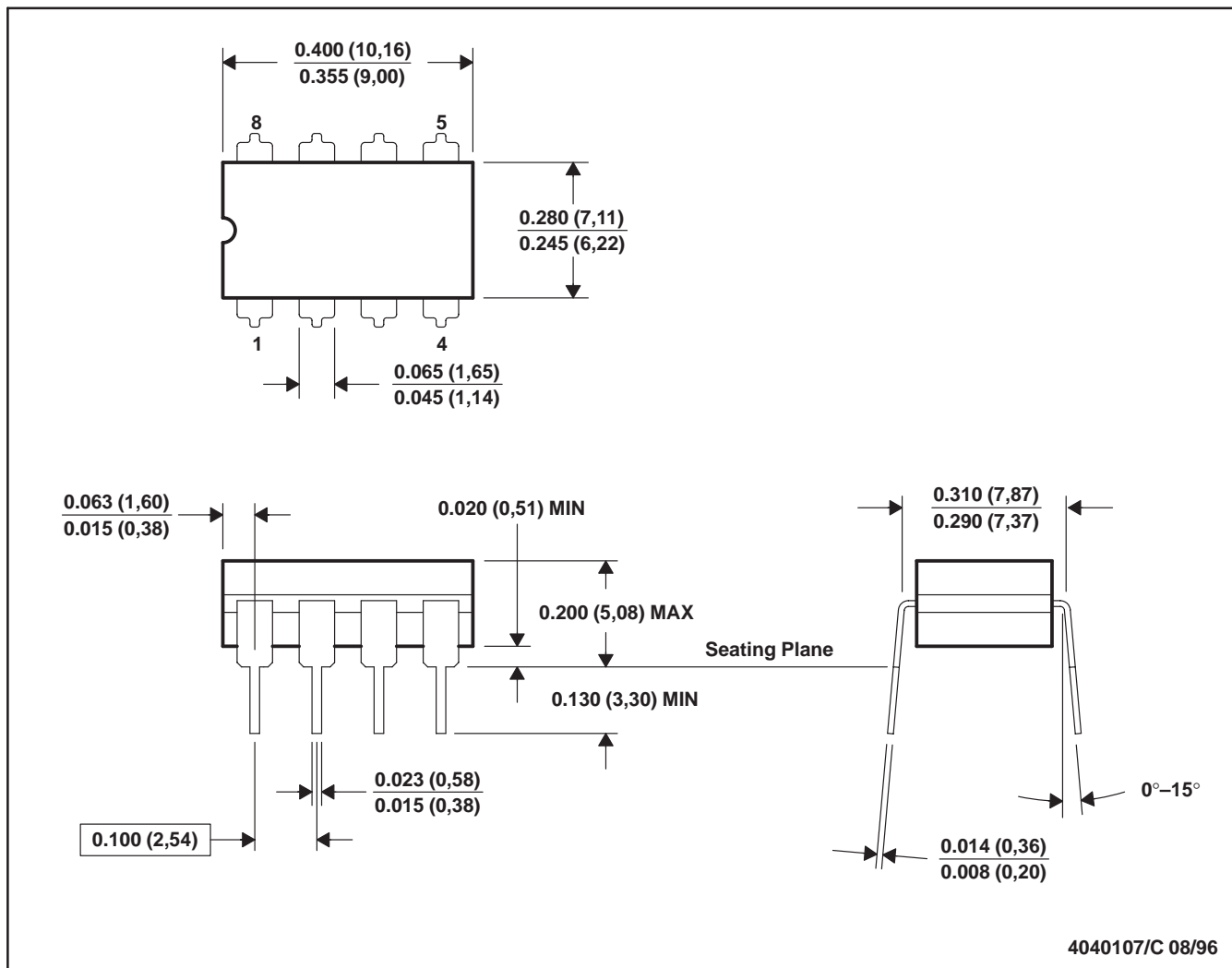
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP1-T8

P (R-PDIP-T8)

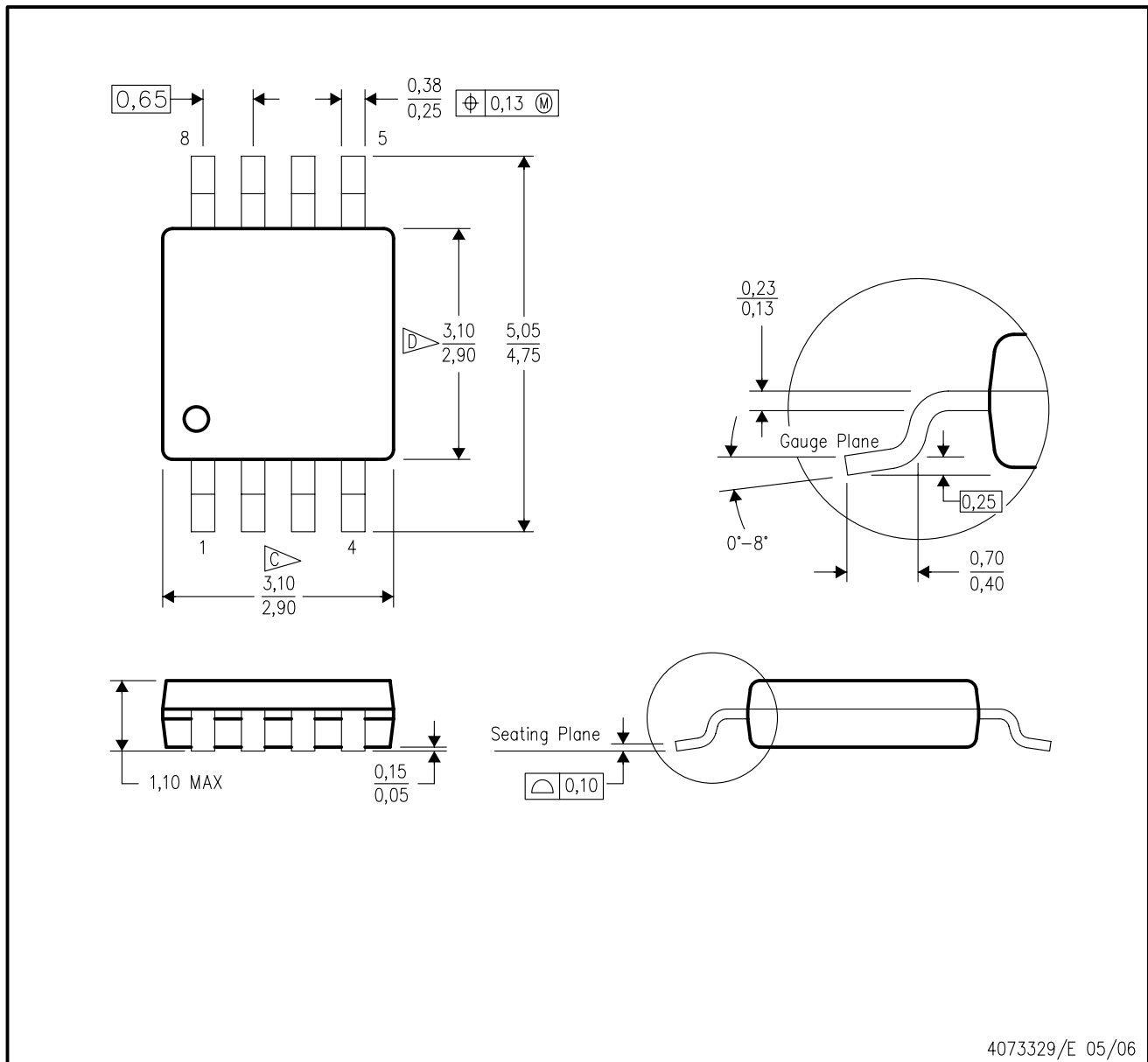
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



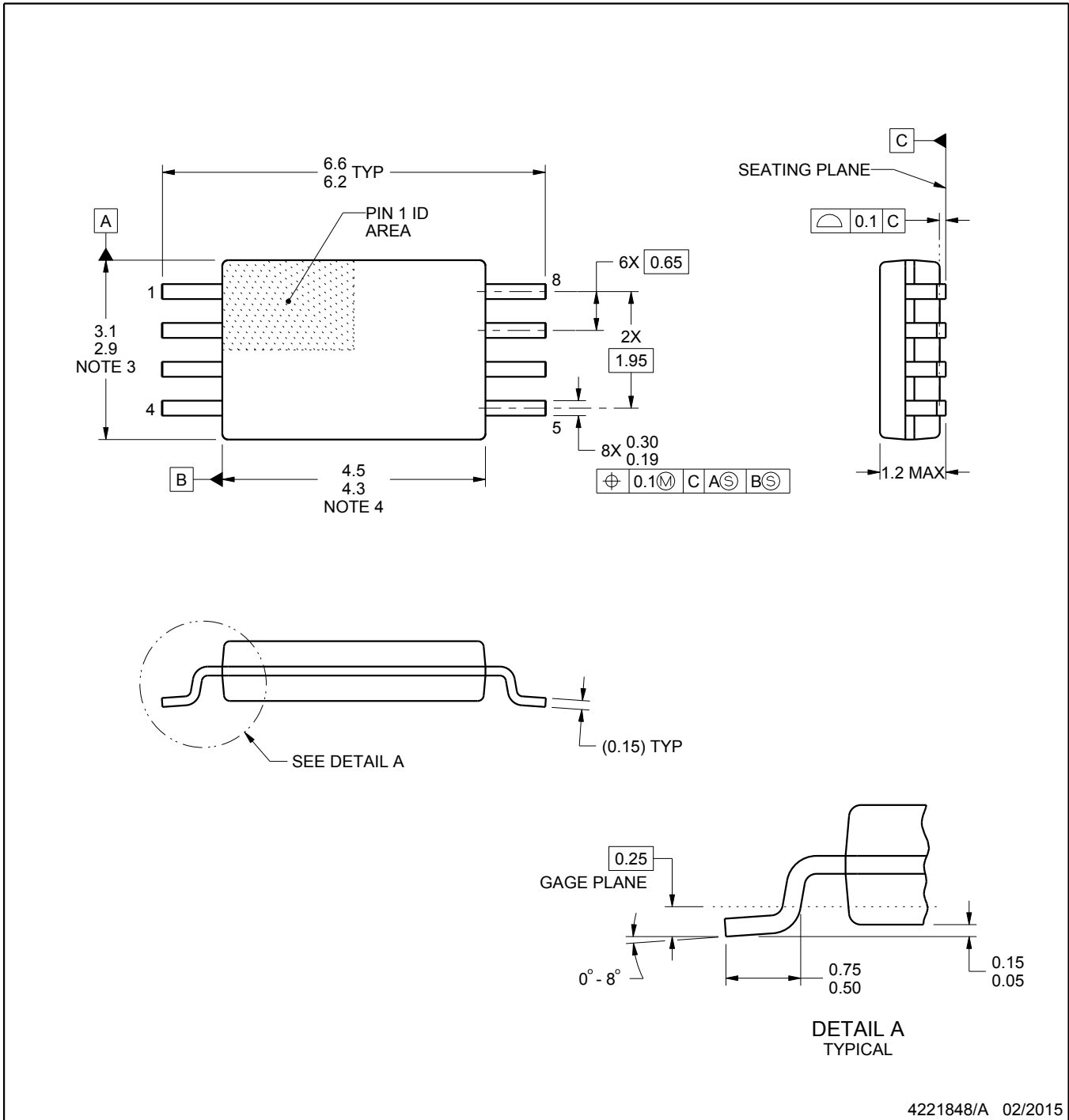
- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW0008A



PACKAGE OUTLINE  
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

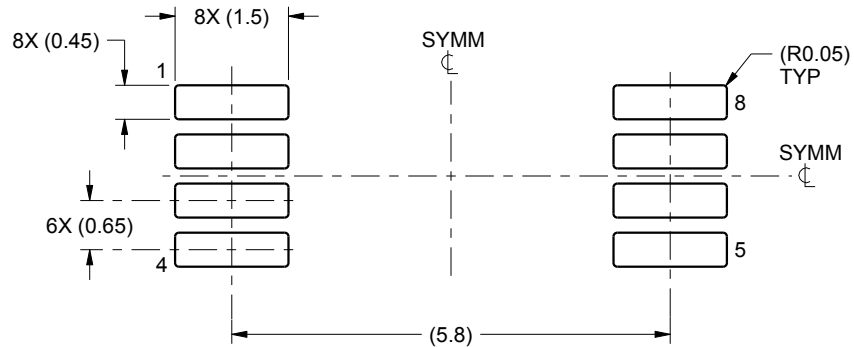
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

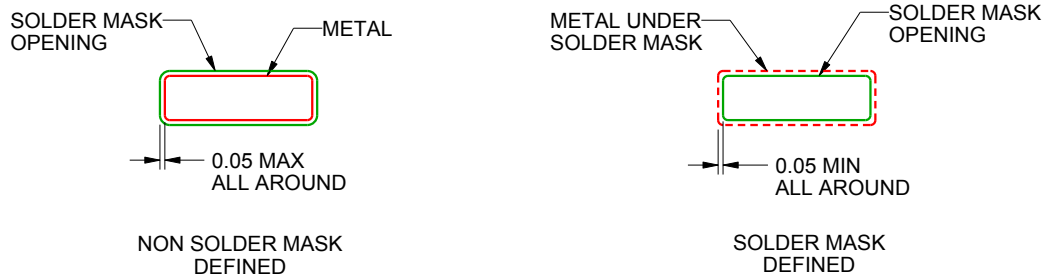
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (<https://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 或 [ti.com.cn](https://www.ti.com.cn) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122  
Copyright © 2021 德州仪器半导体技术（上海）有限公司