TLV320AIC3204 Ultra Low Power Stereo Audio Codec

1 Features

- Stereo Audio DAC with 100dB SNR
- 4.1mW Stereo 48ksps DAC Playback
- Stereo Audio ADC with 93dB SNR
- 6.1mW Stereo 48ksps ADC Record
- PowerTune™
- Extensive Signal Processing Options
- Six Single-Ended or 3 Fully-Differential Analog Inputs
- Stereo Analog and Digital Microphone Inputs
- Stereo Headphone Outputs
- Stereo Line Outputs
- Very Low-Noise PGA
- Low Power Analog Bypass Mode
- Programmable Microphone Bias
- Programmable PLL
- Integrated LDO
- 5-mm × 5-mm, 32-Pin VQFN Package

2 Applications

- Portable Navigation Devices (PND)
- Portable Media Player (PMP)
- Mobile Handsets
- Communication
- Portable Computing

3 Description

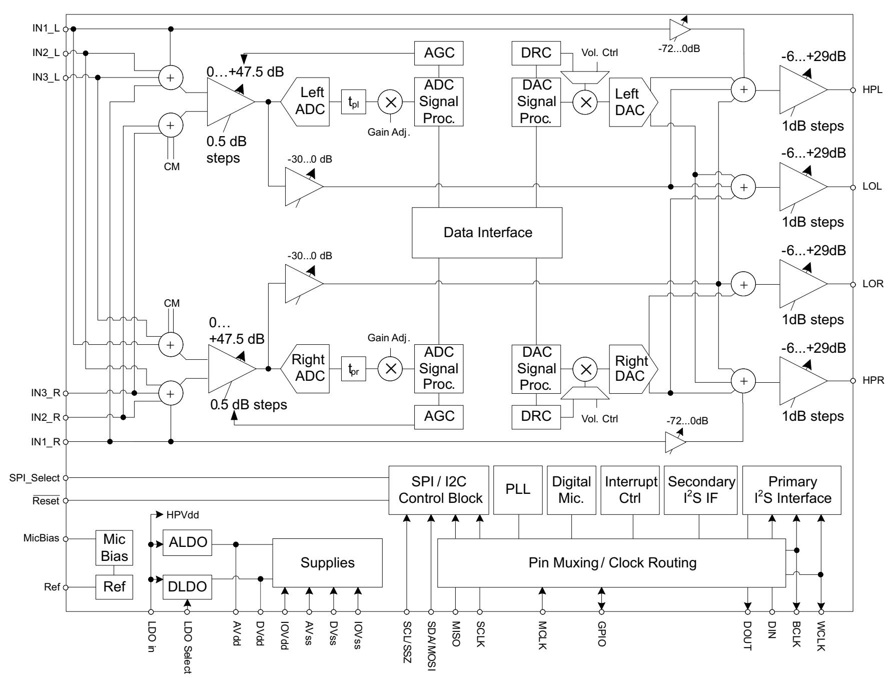
The TLV320AIC3204 (also called the AIC3204) is a flexible, low-power, low-voltage stereo audio codec with programmable inputs and outputs, PowerTune capabilities, fixed predefined and parameterizable signal-processing blocks, integrated PLL, integrated LDOs and flexible digital interfaces.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV320AIC3204	VQFN (32)	5.00 mm x 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 2019) to Revision E — **Page**

- Added BCLK to rise and fall time parameter names in *I^{2}S LJF and RJF Timing in Master Mode* table 17
- Added BCLK to rise and fall time parameter names in *I^{2}S LJF and RJF Timing in Slave Mode* table 18
- Added BCLK to rise and fall time parameter names in *DSP Timing in Master Mode* table 19
- Added BCLK to rise and fall time parameter names in *DSP Timing in Slave Mode* table 20
- Added CLK to rise and fall time parameter names in *Digital Microphone PDM Timing* table 20

Changes from Revision C (November 2014) to Revision D — **Page**

- Changed *ESD Ratings* title and format to current standards 8
- Added footnote to *I^{2}S LJF and RJF Timing in Slave Mode* table 18
- Added footnote to *DSP Timing in Slave Mode* table 20

Changes from Revision B (October 2012) to Revision C — **Page**

- Added the Device information table, Handling Ratings table, Applications and Implementation section, Layout section, and the Device and Documentation Support section 1
- Changed the pin description From: connect to DVss. To: D-LDO enable signal 7
- Added "DVDD" to LDOs disabled in operating conditions statement 8
- Added "Audio input max ac signal swing" to the Recommended Operating Conditions table 8

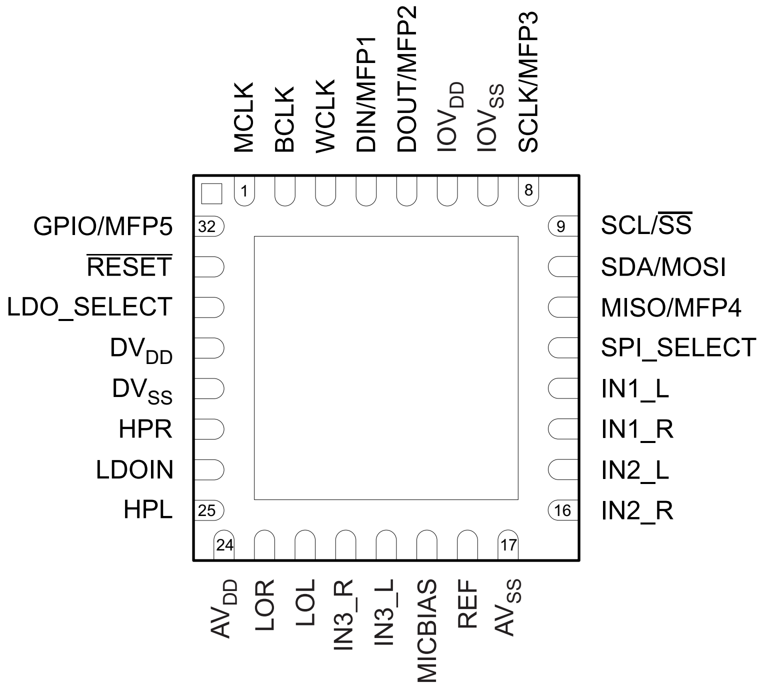
5 Device Comparison Table

ORDER NUMBER	DESCRIPTION
TLV320AIC3254	Low power stereo audio codec with miniDSP.
TLV320AIC3204	Same as TLV320AIC3204 but without miniDSP.
TLV320AIC3256	Similar to TLV320AIC3254 but with ground centered headphone output.
TLV320AIC3206	Same as TLV320AIC3256 but without miniDSP.

6 Pin Configuration and Functions

This document describes signals that take on different names depending on how they are configured. In such cases, the different names are placed together and separated by slash (/) characters. For example, "SCL/$\overline{SS}$". Active low signals are represented by overbars.

RHB Package
(Bottom View)



Pin Functions

PIN	NAME	TYPE(1)	DESCRIPTION
1	MCLK	DI	Master Clock Input
2	BCLK	DIO	Audio serial data bus (primary) bit clock
3	WCLK	DIO	Audio serial data bus (primary) word clock
4	DIN / MFP1	DI	Primary function: Audio serial data bus data input Secondary function: Digital Microphone Input General Purpose Clock Input General Purpose Input
5	DOUT / MFP2	DO	Primary function: Audio serial data bus data output Secondary function: General Purpose Output Clock Output INT1 Output INT2 Output Audio serial data bus (secondary) bit clock output Audio serial data bus (secondary) word clock output
6	IOV_{DD}	Power	IO voltage supply 1.1V – 3.6V
7	IOV_{SS}	Ground	IO ground supply

(1) DI (Digital Input), DO (Digital Output), DIO (Digital Input/Output), AI (Analog Input), AO (Analog Output), AIO (Analog Input/Output)

Pin Functions (continued)

PIN	NAME	TYPE(1)	DESCRIPTION
8	SCLK / MFP3	DI	Primary function: (SPI_Select = 1) SPI serial clock Secondary function: (SPI_Select = 0) Headphone-detect input Digital microphone input Audio serial data bus (secondary) bit clock input Audio serial data bus (secondary) DAC or common word clock input Audio serial data bus (secondary) ADC word clock input Audio serial data bus (secondary) data input General Purpose Input
9	SCL/$\overline{SS}$	DI	I^2C interface serial clock (SPI_Select = 0) SPI interface mode chip-select signal (SPI_Select = 1)
10	SDA/MOSI	DI	I^2C interface mode serial data input (SPI_Select = 0) SPI interface mode serial data input (SPI_Select = 1)
11	MISO / MFP4	DO	Primary function: (SPI_Select = 1) Serial data output Secondary function: (SPI_Select = 0) General purpose output CLKOUT output INT1 output INT2 output Audio serial data bus (primary) ADC word clock output Digital microphone clock output Audio serial data bus (secondary) data output Audio serial data bus (secondary) bit clock output Audio serial data bus (secondary) word clock output
12	SPI_ SELECT	DI	Control mode select pin (1 = SPI, 0 = I^2C)
13	IN1_L	AI	Multifunction Analog Input, or Single-ended configuration: MIC 1 or Line 1 left or Differential configuration: MIC or Line right, negative
14	IN1_R	AI	Multifunction Analog Input, or Single-ended configuration: MIC 1 or Line 1 right or Differential configuration: MIC or Line right, positive
15	IN2_L	AI	Multifunction Analog Input, or Single-ended configuration: MIC 2 or Line 2 left or Differential configuration: MIC or Line left, positive
16	IN2_R	AI	Multifunction Analog Input, or Single-ended configuration: MIC 2 or Line 2 right or Differential configuration: MIC or Line left, negative
17	AV_{SS}	Ground	Analog ground supply
18	REF	AO	Reference voltage output for filtering
19	MICBIAS	AO	Microphone bias voltage output
20	IN3_L	AI	Multifunction Analog Input, or Single-ended configuration: MIC3 or Line 3 left, or Differential configuration: MIC or Line left, positive, or Differential configuration: MIC or Line right, negative
21	IN3_R	AI	Multifunction Analog Input, or Single-ended configuration: MIC3 or Line 3 right, or Differential configuration: MIC or Line left, negative, or Differential configuration: MIC or Line right, positive
22	LOL	AO	Left line output
23	LOR	AO	Right line output
24	AV_{DD}	Power	Analog voltage supply 1.5V–1.95V Input when A-LDO disabled, Filtering output when A-LDO enabled

Pin Functions (continued)

PIN	NAME	TYPE[(1)]	DESCRIPTION
25	HPL	AO	Left high power output driver
26	LDOIN / HPVDD	Power	LDO Input supply and Headphone Power supply 1.9V– 3.6V
27	HPR	AO	Right high power output driver
28	DV_{SS}	Ground	Digital Ground and Chip-substrate
29	DV_{DD}	Power	If LDO_SELECT Pin = 0 (D-LDO disabled) Digital voltage supply 1.26V – 1.95V If LDO_SELECT Pin = 1 (D-LDO enabled) Digital voltage supply filtering output
30	LDO_ SELECT	DI	D-LDO enable signal (1 = D-LDO enable, 0 = D-LDO disabled)
31	$\overline{\text{RESET}}$	DI	Reset (active low)
32	GPIO / MFP5	DI	Primary function: General Purpose digital IO Secondary function: CLKOUT Output INT1 Output INT2 Output Audio serial data bus ADC word clock output Audio serial data bus (secondary) bit clock output Audio serial data bus (secondary) word clock output Digital microphone clock output
Thermal Pad	Thermal Pad	N/A	Connect to PCB ground plane. Not internally connected.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	AV_{DD} to AV_{SS}	–0.3	2.2	V
	DV_{DD} to DV_{SS}	–0.3	2.2	V
	IOV_{DD} to IOV_{SS}	–0.3	3.9	V
	LDOIN to AV_{SS}	–0.3	3.9	V
Digital Input voltage to ground		–0.3	IOV_{DD} + 0.3	V
Analog input voltage to ground		–0.3	AV_{DD} + 0.3	V
Operating temperature range		–40	85	°C
Junction temperature (T_J Max)			105	°C
Storage temperature, T_{stg}		–55	125	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
LDOIN	Power Supply Voltage Range	Referenced to AV_{SS}(1)	1.9		3.6	V
AV_{DD}			1.5	1.8	1.95	
IOV_{DD}		Referenced to IOV_{SS}(1)	1.1		3.6	
DV_{DD}(2)		Referenced to DV_{SS}(1)	1.26	1.8	1.95	
	PLL Input Frequency	Clock divider uses fractional divide (D > 0), P = 1, DV_{DD} ≥ 1.65V (Refer to the table in SLAA557, *Maximum TLV320AIC3204 Clock Frequencies*)	10		20	MHz
		Clock divider uses integer divide (D = 0), P = 1, DV_{DD} ≥ 1.65V (Refer to the table in SLAA557, *Maximum TLV320AIC3204 Clock Frequencies*)	0.512		20	MHz
MCLK	Master Clock Frequency	MCLK; Master Clock Frequency; DV_{DD} ≥ 1.65V			50	MHz
		MCLK; Master Clock Frequency; DV_{DD} ≥ 1.26V			25	
SCL	SCL Clock Frequency				400	kHz
	Audio input max ac signal swing (IN1_L, IN1_R, IN2_L, IN2_R, IN3_L, IN3_R)	CM = 0.75 V	0	0.530	0.75 or AVDD-0.75(3)	Vpeak
		CM = 0.9 V	0	0.707	0.9 or AVDD-0.9(3)	Vpeak
LOL, LOR	Stereo line output load resistance		0.6	10		kΩ
HPL, HPR	Stereo headphone output load resistance	Single-ended configuration	14.4	16		Ω
	Headphone output load resistance	Differential configuration	24.4	32		Ω
C_{Lout}	Digital output load capacitance			10		pF
T_{OPR}	Operating Temperature Range		–40		85	°C

(1) All grounds on board are tied together to prevent voltage differences of more than 0.2V maximum for any combination of ground signals.
(2) At DV_{DD} values lower than 1.65V, the PLL does not function. Refer to the *Maximum TLV320AIC3204 Clock Frequencies* table in the *TLV320AIC3204 Application Reference Guide* (SLAA557) for details on maximum clock frequencies.
(3) Whichever is smaller.

7.4 Thermal Information

THERMAL METRIC(1)		TLV320AIC3204 RHB (32 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.4	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	21.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.4	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics, ADC

At 25°C, AV_{DD}, DV_{DD}, IOV_{DD} = 1.8V, LDOIN = 3.3V, AV_{DD} and DV_{DD} LDO disabled, f_s (Audio) = 48kHz, C_{ref} = 10µF on REF pin, PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO ADC						
	Input signal level (0dB)	Single-ended, CM = 0.9V		0.5		V_{RMS}
	Device Setup	1kHz sine wave input , Single-ended Configuration IN1_R to Right ADC and IN1_L to Left ADC, R_{in} = 20K, f_s = 48kHz, AOSR = 128, MCLK = 256 x f_s, PLL Disabled; AGC = OFF, Channel Gain = 0dB, Processing Block = PRB_R1, Power Tune = PTM_R4				
SNR	Signal-to-noise ratio, A-weighted(1)(2)	Inputs ac-shorted to ground	80	93		dB
		IN2_R, IN3_R routed to Right ADC and ac-shorted to ground IN2_L, IN3_L routed to Left ADC and ac-shorted to ground		93		
DR	Dynamic range A-weighted(1)(2)	–60dB full-scale, 1-kHz input signal		92		dB
THD+N	Total Harmonic Distortion plus Noise	–3 dB full-scale, 1-kHz input signal		–85	–70	dB
		IN2_R, IN3_R routed to Right ADC IN2_L, IN3_L routed to Left ADC –3dB full-scale, 1-kHz input signal		–85		
AUDIO ADC						
	Input signal level (0dB)	Single-ended, CM = 0.75V, AV_{DD} = 1.5V		0.375		V_{RMS}
	Device Setup	1kHz sine wave input, Single-ended Configuration IN1_R, IN2_R, IN3_R routed to Right ADC IN1_L, IN2_L, IN3_L routed to Left ADC R_{in} = 20kΩ, f_s = 48kHz, AOSR = 128, MCLK = 256 x f_s, PLL Disabled, AGC = OFF, Channel Gain = 0dB, Processing Block = PRB_R1 Power Tune = PTM_R4				
SNR	Signal-to-noise ratio, A-weighted (1)(2)	Inputs ac-shorted to ground		91		dB
DR	Dynamic range A-weighted(1)(2)	–60dB full-scale, 1-kHz input signal		90		dB
THD+N	Total Harmonic Distortion plus Noise	–3dB full-scale, 1-kHz input signal		–80		dB

(1) Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.
(2) All performance measured with 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

Electrical Characteristics, ADC (continued)

At 25°C, AV_{DD}, DV_{DD}, IOV_{DD} = 1.8V, LDOIN = 3.3V, AV_{DD} and DV_{DD} LDO disabled, f_s (Audio) = 48kHz, C_{ref} = 10µF on REF pin, PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO ADC						
	Input signal level (0dB)	Differential Input, CM = 0.9V		10		mV
	Device Setup	1kHz sine wave input, Differential configuration IN1_L and IN1_R routed to Right ADC IN2_L and IN2_R routed to Left ADC R_{in} = 10K, f_s = 48kHz, AOSR = 128 MCLK = 256* f_s PLL Disabled AGC = OFF, Channel Gain = 40dB Processing Block = PRB_R1, Power Tune = PTM_R4				
ICN	Idle-Channel Noise, A-weighted[(1)(2)]	Inputs ac-shorted to ground, input referred noise		2		μV_{RMS}
AUDIO ADC						
	Gain Error	1kHz sine wave input , Single-ended configuration R_{in} = 20kΩ f_s = 48kHz, AOSR = 128, MCLK = 256 x f_s, PLL Disabled AGC = OFF, Channel Gain = 0dB Processing Block = PRB_R1, Power Tune = PTM_R4, CM = 0.9V		–0.05		dB
	Input Channel Separation	1kHz sine wave input at -3dBFS Single-ended configuration IN1_L routed to Left ADC IN1_R routed to Right ADC, R_{in} = 20kΩ AGC = OFF, AOSR = 128, Channel Gain = 0dB, CM = 0.9V		108		dB
	Input Pin Crosstalk	1kHz sine wave input at –3dBFS on IN2_L, IN2_L internally not routed. IN1_L routed to Left ADC ac-coupled to ground 1kHz sine wave input at –3dBFS on IN2_R, IN2_R internally not routed. IN1_R routed to Right ADC ac-coupled to ground Single-ended configuration R_{in} = 20kΩ, AOSR = 128 Channel, Gain = 0dB, CM = 0.9V		115		dB
	PSRR	217Hz, 100mVpp signal on AV_{DD}, Single-ended configuration, R_{in} = 20kΩ, Channel Gain = 0dB; CM = 0.9V		55		dB
	ADC programmable gain amplifier gain	Single-Ended, R_{in} = 10kΩ, PGA gain set to 0dB		0		dB
		Single-Ended, R_{in} = 10kΩ, PGA gain set to 47.5dB		47.5		dB
		Single-Ended, R_{in} = 20kΩ, PGA gain set to 0dB		–6		dB
		Single-Ended, R_{in} = 20kΩ, PGA gain set to 47.5dB		41.5		dB
		Single-Ended, R_{in} = 40kΩ, PGA gain set to 0dB		–12		dB
		Single-Ended, R_{in} = 40kΩ, PGA gain set to 47.5dB		35.5		dB
	ADC programmable gain amplifier step size	1-kHz tone		0.5		dB

7.6 Electrical Characteristics, Bypass Outputs

At 25°C, AV_{DD}, DV_{DD}, IOV_{DD} = 1.8V, LDOIN = 3.3V, AV_{DD} and DV_{DD} LDO disabled, f_s (Audio) = 48kHz, C_{ref} = 10µF on REF pin, PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG BYPASS TO HEADPHONE AMPLIFIER, DIRECT MODE						
	Device Setup	Load = 16Ω (single-ended), 50pF; Input and Output CM = 0.9V; Headphone Output on LDOIN Supply; IN1_L routed to HPL and IN1_R routed to HPR; Channel Gain = 0dB				
	Gain Error			–0.8		dB
	Noise, A-weighted(1)	Idle Channel, IN1_L and IN1_R ac-shorted to ground		3		μV_{RMS}
THD	Total Harmonic Distortion	446mVrms, 1kHz input signal		–89		dB
ANALOG BYPASS TO LINE-OUT AMPLIFIER, PGA MODE						
	Device Setup	Load = 10kΩ (single-ended), 56pF; Input and Output CM = 0.9V; LINE Output on LDOIN Supply; IN1_L routed to ADCPGA_L and IN1_R routed to ADCPGA_R; R_{in} = 20kΩ ADCPGA_L routed to LOL and ADCPGA_R routed to LOR; Channel Gain = 0dB				
	Gain Error			0.6		dB
	Noise, A-weighted(1)	Idle Channel, IN1_L and IN1_R ac-shorted to ground		7		μV_{RMS}
		Channel Gain = 40dB, Input Signal (0dB) = 5mV_{rms} Inputs ac-shorted to ground, Input Referred		3.4		μV_{RMS}

(1) All performance measured with 20kHz low-pass filter and, where noted, A-weighted filter. Testing without such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

7.7 Electrical Characteristics, Microphone Interface

At 25°C, AV_{DD}, DV_{DD}, IOV_{DD} = 1.8V, LDOIN = 3.3V, AV_{DD} and DV_{DD} LDO disabled, f_s (Audio) = 48kHz, C_{ref} = 10µF on REF pin, PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MICROPHONE BIAS						
	Bias voltage	Bias voltage CM = 0.9V, LDOIN = 3.3V				
		Micbias Mode 0, Connect to AV_{DD} or LDOIN		1.25		V
		Micbias Mode 1, Connect to LDOIN		1.7		V
		Micbias Mode 2, Connect to LDOIN		2.5		V
		Micbias Mode 3, Connect to AV_{DD}		AV_{DD}		V
		Micbias Mode 3, Connect to LDOIN		LDOIN		V
		CM = 0.75V, LDOIN = 3.3V				
		Micbias Mode 0, Connect to AV_{DD} or LDOIN		1.04		V
		Micbias Mode 1, Connect to AV_{DD} or LDOIN		1.425		V
		Micbias Mode 2, Connect to LDOIN		2.075		V
		Micbias Mode 3, Connect to AV_{DD}		AV_{DD}		V
		Micbias Mode 3, Connect to LDOIN		LDOIN		V
	Output Noise	CM = 0.9V, Micbias Mode 2, A-weighted, 20Hz to 20kHz bandwidth, Current load = 0mA.		10		μV_{RMS}
	Current Sourcing	Micbias Mode 2, Connect to LDOIN		3		mA
	Inline Resistance	Micbias Mode 3, Connect to AV_{DD}		140		Ω
		Micbias Mode 3, Connect to LDOIN		87		

7.8 Electrical Characteristics, Audio DAC Outputs

At 25°C, AV_{DD}, DV_{DD}, IOV_{DD} = 1.8V, LDOIN = 3.3V, AV_{DD} and DV_{DD} LDO disabled, f_s (Audio) = 48kHz, C_{ref} = 10µF on REF pin, PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO DAC – STEREO SINGLE-ENDED LINE OUTPUT						
	Device Setup	Load = 10kΩ (single-ended), 56pF Line Output on AV_{DD} Supply Input and Output CM = 0.9V DOSR = 128, MCLK = 256 x f_S, Channel Gain = 0dB, word length = 16 bits, Processing Block = PRB_P1, Power Tune = PTM_P3				
	Full scale output voltage (0dB)			0.5		V_{RMS}
SNR	Signal-to-noise ratio A-weighted (1) (2)	All zeros fed to DAC input	87	100		dB
DR	Dynamic range, A-weighted (1) (2)	–60dB 1kHz input full-scale signal, Word length = 20 bits		100		dB
THD+N	Total Harmonic Distortion plus Noise	–3dB full-scale, 1kHz input signal		–83	–70	dB
	DAC Gain Error	0 dB, 1kHz input full scale signal		0.3		dB
	DAC Mute Attenuation	Mute		119		dB
	DAC channel separation	–1 dB, 1kHz signal, between left and right HP out		113		dB
	DAC PSRR	100mVpp, 1kHz signal applied to AV_{DD}		73		dB
		100mVpp, 217Hz signal applied to AV_{DD}		77		dB
AUDIO DAC – STEREO SINGLE-ENDED LINE OUTPUT						
	Device Setup	Load = 10kΩ (single-ended), 56pF Line Output on AV_{DD} Supply Input and Output CM = 0.75V; AV_{DD} = 1.5V DOSR = 128 MCLK = 256 * fs Channel Gain = –2dB word length = 20 bits Processing Block = PRB_P1 Power Tune = PTM_P4				
	Full scale output voltage (0dB)			0.375		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted (1) (2)	All zeros fed to DAC input		99		dB
DR	Dynamic range, A-weighted (1) (2)	–60dB 1 kHz input full-scale signal		97		dB
THD+N	Total Harmonic Distortion plus Noise	–1 dB full-scale, 1-kHz input signal		–85		dB
AUDIO DAC – STEREO SINGLE-ENDED HEADPHONE OUTPUT						
	Device Setup	Load = 16Ω (single-ended), 50pF Headphone Output on AV_{DD} Supply, Input and Output CM = 0.9V, DOSR = 128, MCLK = 256 * f_S, Channel Gain = 0dB word length = 16 bits; Processing Block = PRB_P1 Power Tune = PTM_P3				
	Full scale output voltage (0dB)			0.5		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted (1) (2)	All zeros fed to DAC input	87	100		dB
DR	Dynamic range, A-weighted (1) (2)	–60dB 1kHz input full-scale signal, Word Length = 20 bits, Power Tune = PTM_P4		99		dB
THD+N	Total Harmonic Distortion plus Noise	–3dB full-scale, 1kHz input signal		–83	–70	dB
	DAC Gain Error	0dB, 1kHz input full scale signal		–0.3		dB
	DAC Mute Attenuation	Mute		122		dB

(1) Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.
(2) All performance measured with 20kHz low-pass filter and, where noted, A-weighted filter. Testing without such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

Electrical Characteristics, Audio DAC Outputs (continued)

At 25°C, AV_{DD}, DV_{DD}, IOV_{DD} = 1.8V, LDOIN = 3.3V, AV_{DD} and DV_{DD} LDO disabled, f_s (Audio) = 48kHz, C_{ref} = 10µF on REF pin, PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	DAC channel separation	–1dB, 1kHz signal, between left and right HP out		110		dB
	DAC PSRR	100mVpp, 1kHz signal applied to AV_{DD}		73		dB
		100mVpp, 217Hz signal applied to AV_{DD}		78		dB
	Power Delivered	R_L = 16Ω, Output Stage on AV_{DD} = 1.8V THDN < 1%, Input CM = 0.9V, Output CM = 0.9V		15		mW
		R_L = 16Ω Output Stage on LDOIN = 3.3V, THDN < 1% Input CM = 0.9V, Output CM = 1.65V		64		
AUDIO DAC – STEREO SINGLE-ENDED HEADPHONE OUTPUT						
	Device Setup	Load = 16Ω (single-ended), 50pF, Headphone Output on AV_{DD} Supply, Input and Output CM = 0.75V; AV_{DD} = 1.5V, DOSR = 128, MCLK = 256 * f_s, Channel Gain = –2dB, word length = 20-bits; Processing Block = PRB_P1, Power Tune = PTM_P4				
	Full scale output voltage (0dB)			0.375		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted (1) (2)	All zeros fed to DAC input		99		dB
DR	Dynamic range, A-weighted (1) (2)	-60dB 1kHz input full-scale signal		98		dB
THD+N	Total Harmonic Distortion plus Noise	–1dB full-scale, 1kHz input signal		–83		dB
AUDIO DAC – MONO DIFFERENTIAL HEADPHONE OUTPUT						
	Device Setup	Load = 32Ω (differential), 50pF, Headphone Output on LDOIN Supply Input CM = 0.75V, Output CM = 1.5V, AV_{DD} = 1.8V, LDOIN = 3.0V, DOSR = 128 MCLK = 256 * f_s, Channel (headphone driver) Gain = 5dB for full scale output signal, word length = 16 bits, Processing Block = PRB_P1, Power Tune = PTM_P3				
	Full scale output voltage (0dB)			1778		mV_{RMS}
SNR	Signal-to-noise ratio, A-weighted (1) (2)	All zeros fed to DAC input		98		dB
DR	Dynamic range, A-weighted (1) (2)	–60dB 1kHz input full-scale signal		96		dB
THD	Total Harmonic Distortion	–3dB full-scale, 1kHz input signal		–82		dB
	Power Delivered	R_L = 32Ω, Output Stage on LDOIN = 3.3V, THDN < 1%, Input CM = 0.9V, Output CM = 1.65V		136		mW
		R_L = 32Ω Output Stage on LDOIN = 3.0V, THDN < 1% Input CM = 0.9V, Output CM = 1.5V		114		mW

7.9 Electrical Characteristics, LDO

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOW DROPOUT REGULATOR (AVdd)						
	Output Voltage	LDOMode = 1, LDOIN > 1.95V		1.67		V
		LDOMode = 0, LDOIN > 2.0V		1.72		
		LDOMode = 2, LDOIN > 2.05V		1.77		
	Output Voltage Accuracy			±2%		
	Load Regulation	Load current range 0 to 50mA		15		mV
	Line Regulation	Input Supply Range 1.9V to 3.6V		5		mV
	Decoupling Capacitor		1			μF
	Bias Current			60		μA
LOW DROPOUT REGULATOR (DVdd)						
	Output Voltage	LDOMode = 1, LDOIN > 1.95V		1.67		V
		LDOMode = 0, LDOIN > 2.0V		1.72		
		LDOMode = 2, LDOIN > 2.05V		1.77		
	Output Voltage Accuracy			±%2		
	Load Regulation	Load current range 0 to 50mA		15		mV
	Line Regulation	Input Supply Range 1.9V to 3.6V		5		mV
	Decoupling Capacitor		1			μF
	Bias Current			60		μA

7.10 Electrical Characteristics, Misc.

At 25°C, AV_{DD}, DV_{DD}, IOV_{DD} = 1.8V, LDOIN = 3.3V, AV_{DD} and DV_{DD} LDO disabled, f_s (Audio) = 48kHz, C_{ref} = 10µF on REF pin, PLL disabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE						
	Reference Voltage Settings	CMMode = 0 (0.9V)		0.9		V
		CMMode = 1 (0.75V)		0.75		
	Reference Noise	CM = 0.9V, A-weighted, 20Hz to 20kHz bandwidth, C_{ref} = 10µF		1		$µV_{RfcMS}$
	Decoupling Capacitor		1	10		µF
	Bias Current			120		µA
Shutdown Current						
	Device Setup	Coarse AV_{DD} supply turned off, LDO_select held at ground, No external digital input is toggled				
	$I(DV_{DD})$			0.9		µA
	$I(AV_{DD})$			<0.9		µA
	I(LDOIN)			<0.9		µA
	I(IOVDD)			13		nA

7.11 Electrical Characteristics, Logic Levels[(1)]

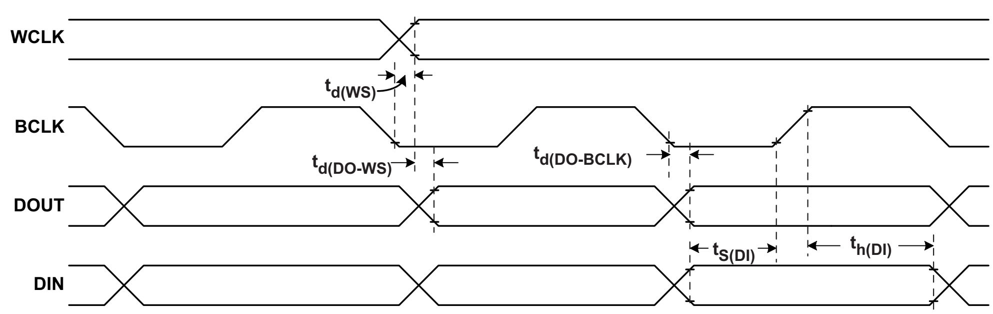
At 25°C, AV_{DD}, DV_{DD}, IOV_{DD} = 1.8V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC FAMILY (CMOS)						
V_{IH}	Logic Level	I_{IH} = 5 μA, IOV_{DD} > 1.6V	0.7 × IOV_{DD}			V
		I_{IH} = 5μA, 1.2V ≤ IOV_{DD} < 1.6V	0.9 × IOV_{DD}			V
		I_{IH} = 5μA, IOV_{DD} < 1.2V	IOV_{DD}			V
V_{IL}		I_{IL} = 5 μA, IOV_{DD} > 1.6V	–0.3		0.3 × IOV_{DD}	V
		I_{IL} = 5μA, 1.2V ≤ IOV_{DD} < 1.6V			0.1 × IOV_{DD}	V
		I_{IL} = 5μA, IOV_{DD} < 1.2V			0	V
V_{OH}		I_{OH} = 2 TTL loads	0.8 × IOV_{DD}			V
V_{OL}		I_{OL} = 2 TTL loads			0.1 × IOV_{DD}	V
	Capacitive Load			10		pF

(1) Applies to all DI, DO, and DIO pins shown in *Pin Configuration and Functions*.

7.12 I²S LJF and RJF Timing in Master Mode (see Figure 1)

		IOVDD = 1.8 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
$t_{d(WS)}$	WCLK delay		30		20	ns
$t_{d(DO-WS)}$	WCLK to DOUT delay (For LJF Mode only)		20		20	ns
$t_{d(DO-BCLK)}$	BCLK to DOUT delay		22		20	ns
$t_{s(DI)}$	DIN setup	8		8		ns
$t_{h(DI)}$	DIN hold	8		8		ns
t_r	BCLK rise time		24		12	ns
t_f	BCLK fall time		24		12	ns



All specifications at 25°C, DVdd = 1.8V

Figure 1. I²S LJF and RJF Timing in Master Mode

7.13 I²S LJF and RJF Timing in Slave Mode (see Figure 2)

		IOVDD = 1.8V		IOVDD = 3.3V		UNIT
		MIN	MAX	MIN	MAX	
$t_{H(BCLK)}$	BCLK high period	35		35		ns
$t_{L(BCLK)}$	BCLK low period	35		35		ns
$t_{s(WS)}$	WCLK setup	8		8		ns
$t_{h(WS)}$	WCLK hold	8		8		ns
$t_{d(DO-WS)}$	WCLK to DOUT delay (For LJF mode only)		20		20	ns
$t_{d(DO-BCLK)}$	BCLK to DOUT delay		22		22	ns
$t_{s(DI)}$	DIN setup	8		8		ns
$t_{h(DI)}$	DIN hold	8		8		ns
t_r	BCLK rise time		4 (1)		4 (1)	ns
t_f	BCLK fall time		4 (1)		4 (1)	ns

(1) The BCLK maximum rise and fall time can be as high as 10 ns, if the BCLK high and low period are greater than 50 ns.

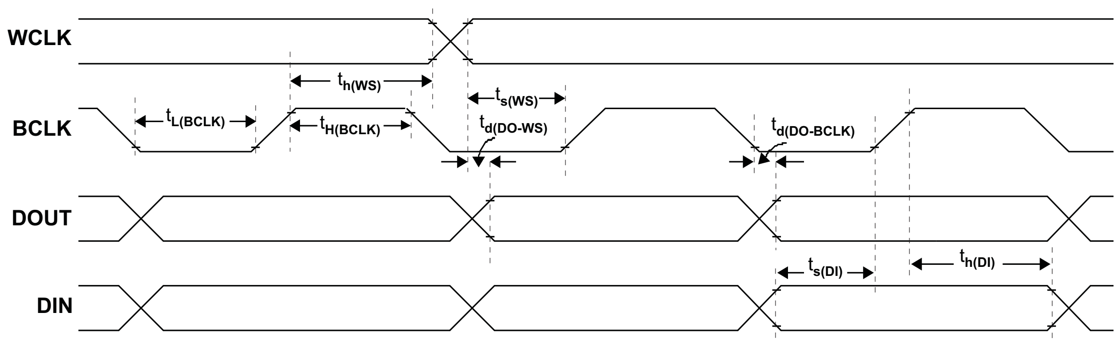
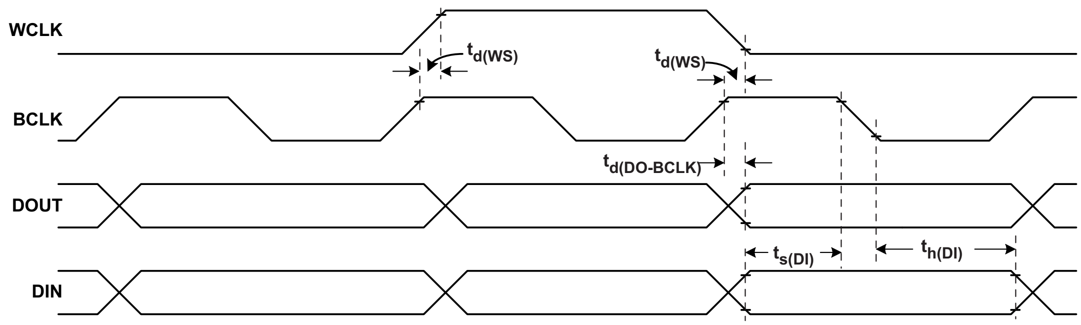


Figure 2. I²S LJF and RJF Timing in Slave Mode

7.14 DSP Timing in Master Mode (see Figure 3)

		IOVDD = 1.8V		IOVDD = 3.3V		UNIT
		MIN	MAX	MIN	MAX	
$t_{d(WS)}$	WCLK delay		30		20	ns
$t_{d(DO-BCLK)}$	BCLK to DOUT delay		22		20	ns
$t_{s(DI)}$	DIN setup	8		8		ns
$t_{h(DI)}$	DIN hold	8		8		ns
t_r	BCLK rise time		24		12	ns
t_f	BCLK fall time		24		12	ns



All specifications at 25°C, DVdd = 1.8V

Figure 3. DSP Timing in Master Mode

7.15 DSP Timing in Slave Mode (see Figure 4)

		IOVDD = 1.8V		IOVDD = 3.3V		UNIT
		MIN	MAX	MIN	MAX	
$t_{H(BCLK)}$	BCLK high period	35		35		ns
$t_{L(BCLK)}$	BCLK low period	35		35		ns
$t_{s(WS)}$	WCLK setup	8		8		ns
$t_{h(WS)}$	WCLK hold	8		8		ns
$t_{d(DO-BCLK)}$	BCLK to DOUT delay		22		22	ns
$t_{s(DI)}$	DIN setup	8		8		ns
$t_{h(DI)}$	DIN hold	8		8		ns
t_r	BCLK rise time		4 (1)		4 (1)	ns
t_f	BCLK fall time		4 (1)		4 (1)	ns

(1) The BCLK maximum rise and fall time can be as high as 10 ns, if the BCLK high and low period are greater than 50 ns.

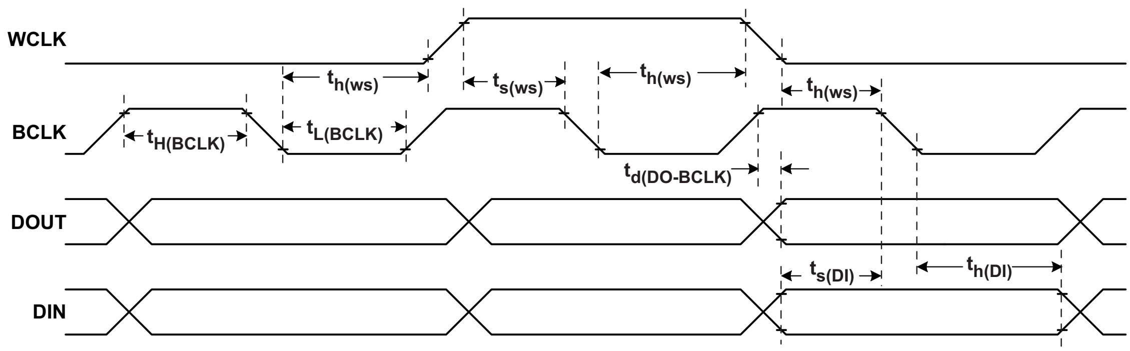


Figure 4. DSP Timing in Slave Mode

7.16 Digital Microphone PDM Timing (see Figure 5)

Based on design simulation. Not tested in actual silicon.

		IOVDD = 1.8V		IOVDD = 3.3V		UNIT
		MIN	MAX	MIN	MAX	
t_s	DIN setup	20		20		ns
t_h	DIN hold	5		5		ns
t_r	CLK rise time		4		4	ns
t_f	CLK fall time		4		4	ns

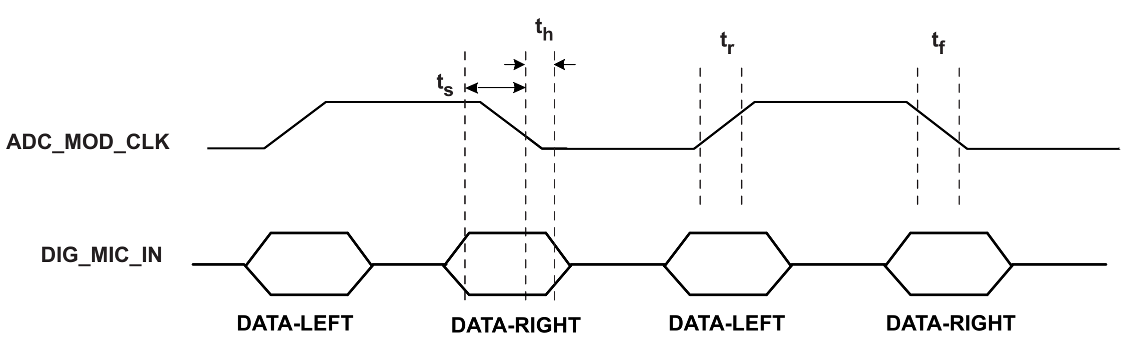


Figure 5. PDM Input Timing

7.17 I²C Interface Timing

		Standard-Mode			Fast-Mode			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{SCL}	SCL clock frequency	0		100	0		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0			0.8			μs
t_{LOW}	LOW period of the SCL clock	4.7			1.3			μs
t_{HIGH}	HIGH period of the SCL clock	4.0			0.6			μs
$t_{SU;STA}$	Setup time for a repeated START condition	4.7			0.8			μs
$t_{HD;DAT}$	Data hold time: For I2C bus devices	0		3.45	0		0.9	μs
$t_{SU;DAT}$	Data set-up time	250			100			ns
t_r	SDA and SCL Rise Time			1000	20+0.1C_b		300	ns
t_f	SDA and SCL Fall Time			300	20+0.1C_b		300	ns
$t_{SU;STO}$	Set-up time for STOP condition	4.0			0.8			μs
t_{BUF}	Bus free time between a STOP and START condition	4.7			1.3			μs
C_b	Capacitive load for each bus line			400			400	pF

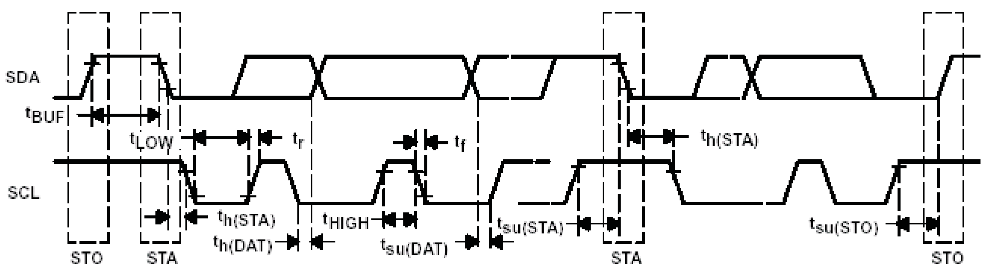
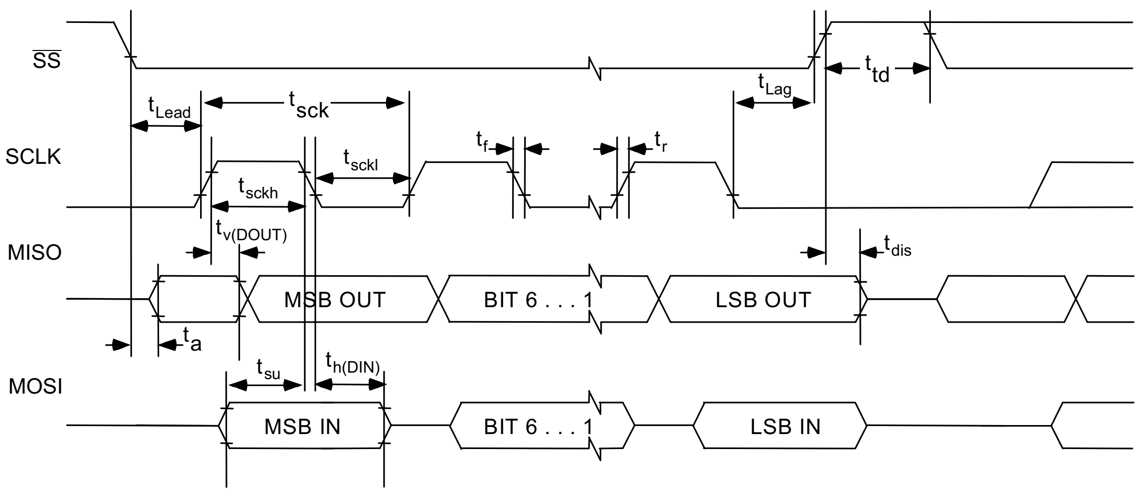


Figure 6. I²C Interface Timing

7.18 SPI Interface Timing (See Figure 7)

		IOVDD = 1.8V			IOVDD = 3.3V			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{sck}	SCLK Period[(1)]	100			50			ns
t_{sckh}	SCLK Pulse width High	50			25			ns
t_{sckl}	SCLK Pulse width Low	50			25			ns
t_{lead}	Enable Lead Time	30			20			ns
t_{trail}	Enable Trail Time	30			20			ns
$t_{d;seqxfr}$	Sequential Transfer Delay	40			20			ns
t_a	Slave DOUT access time			40			20	ns
t_{dis}	Slave DOUT disable time			40			20	ns
t_{su}	DIN data setup time	15			10			ns
$t_{h(DIN)}$	DIN data hold time	15			10			ns
$t_{v(DOUT)}$	DOUT data valid time			25			18	ns
t_r	SCLK Rise Time			4			4	ns
t_f	SCLK Fall Time			4			4	ns

(1) These parameters are based on characterization and are not tested in production.



At 25°C, DVdd = 1.8V

Figure 7. SPI Interface Timing Diagram

7.19 Typical Characteristics

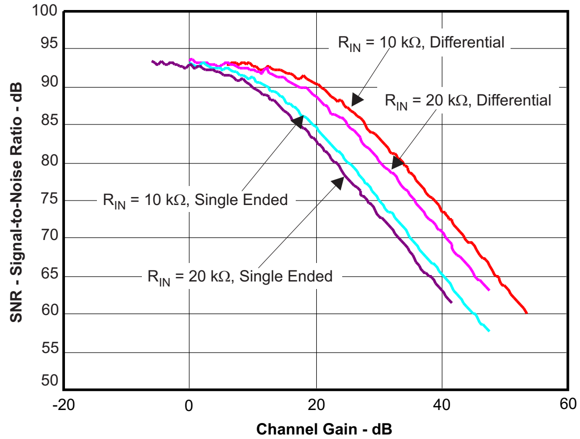


Figure 8. ADC SNR vs Channel Gain

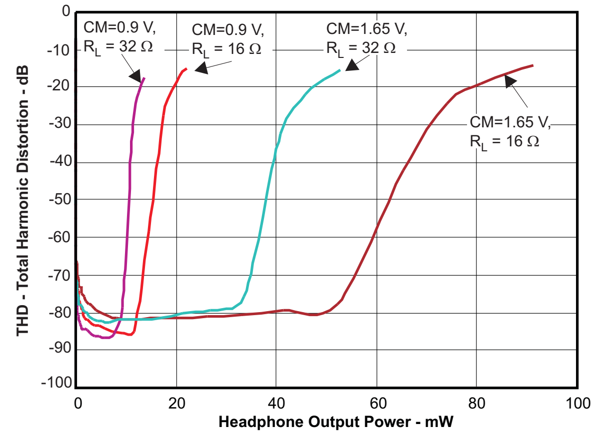


Figure 9. Total Harmonic Distortion vs Headphone Output Power

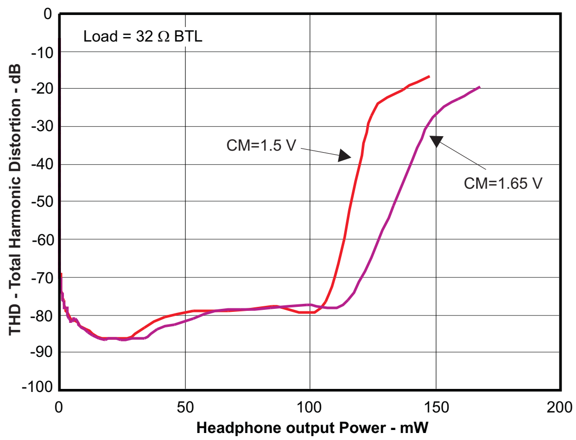


Figure 10. Total Harmonic Distortion vs Headphone Output Power

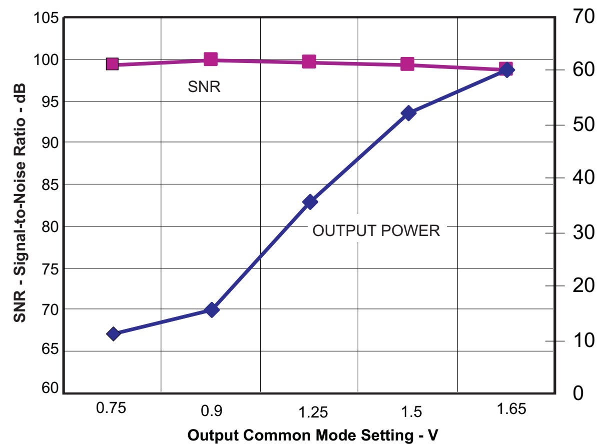


Figure 11. Headphone SNR and Output Power vs Output Common Mode Setting

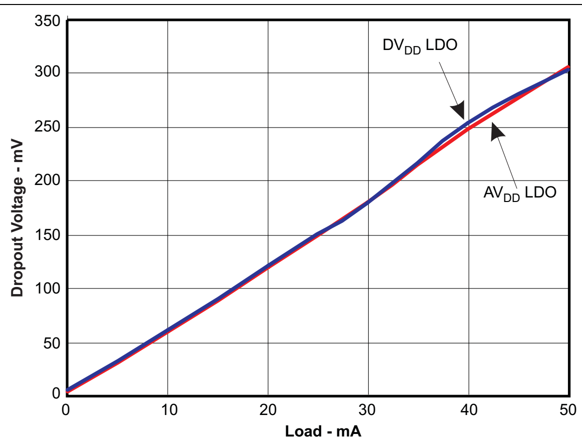


Figure 12. LDO Dropout Voltage vs Load Current

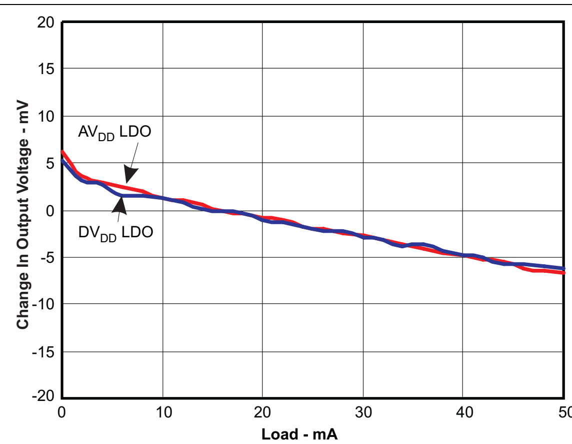


Figure 13. LDO Load Response

Typical Characteristics (continued)

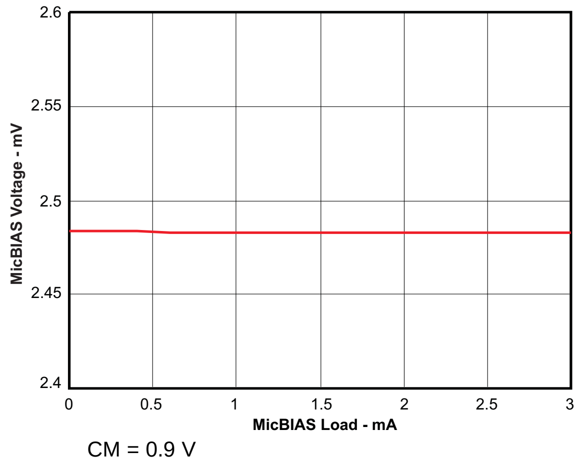


Figure 14. MICBIAS Mode 2, LDOIN OP Stage vs MICBIAS Load Current

7.20 Typical Characteristics, FFT

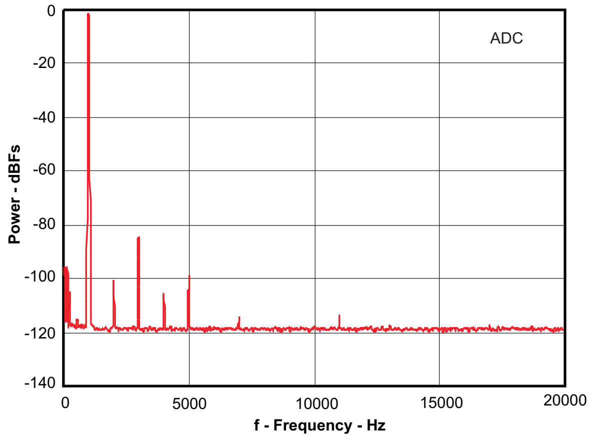


Figure 15. Single Ended Line Input to ADC FFT at -1dBr vs Frequency

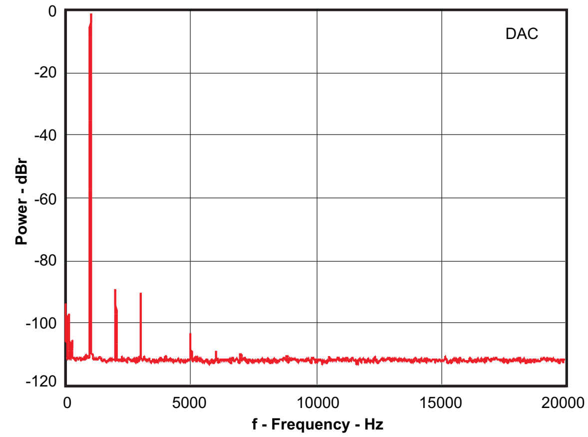


Figure 16. DAC Playback to Headphone FFT at -1dBFS vs Frequency

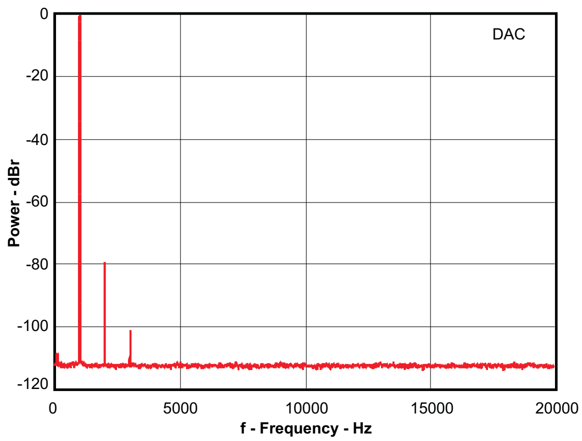


Figure 17. DAC Playback to Line-out FFT at -1dBFS vs Frequency

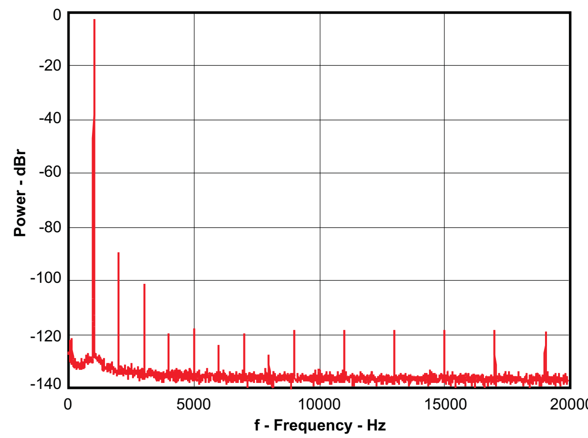


Figure 18. Line Input to Headphone FFT at 446mVrms vs Frequency

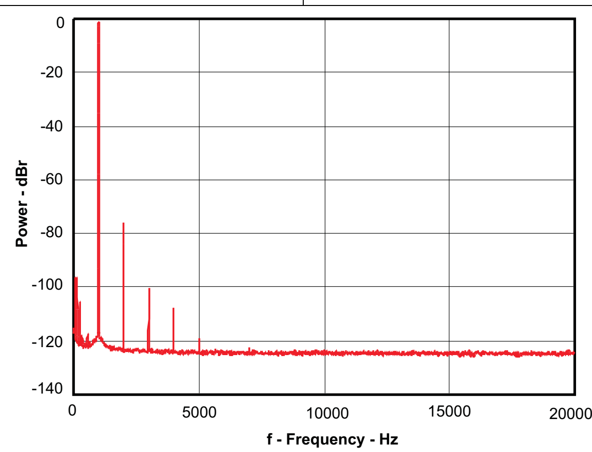


Figure 19. Line Input to Line-out FFT at 446mVrms vs Frequency

8 Parameter Measurement Information

All parameters are measured according to the conditions described in the *Specifications* section.

9 Detailed Description

9.1 Overview

The TLV320AIC3204 includes extensive register-based control of power, input/output channel configuration, gains, effects, pin-multiplexing and clocks, allowing precise targeting of the device to its application. Combined with the advanced PowerTune technology, the device covers operations from 8 kHz mono voice playback to audio stereo 192kHz DAC playback, making it ideal for portable battery-powered audio and telephony applications.

The record path of the TLV320AIC3204 covers operations from 8kHz mono to 192kHz stereo recording, and contains programmable input channel configurations covering single-ended and differential setups, as well as floating or mixing input signals. It also includes a digitally-controlled stereo microphone preamplifier and integrated microphone bias. Digital signal processing blocks can remove audible noise that may be introduced by mechanical coupling, e.g. optical zooming in a digital camera.

The playback path offers signal-processing blocks for filtering and effects, and supports flexible mixing of DAC and analog input signals as well as programmable volume controls. The playback path contains two high-power output drivers as well as two fully-differential outputs. The high-power outputs can be configured in multiple ways, including stereo and mono BTL.

The integrated PowerTune technology allows the device to be tuned to an optimum power-performance trade-off. Mobile applications frequently have multiple use cases requiring very low power operation while being used in a mobile environment. When used in a docked environment power consumption typically is less of a concern, while minimizing noise is important. With PowerTune, the TLV320AIC3204 addresses both cases.

The voltage supply range for the TLV320AIC3204 for analog is 1.5V–1.95V, and for digital it is 1.26V–1.95V. To ease system-level design, integrated LDOs generate the appropriate analog or digital supply from input voltages ranging from 1.8V to 3.6V. The device supports digital I/O voltages in the range of 1.1V–3.6V.

The required internal clock of the TLV320AIC3204 can be derived from multiple sources, including the MCLK pin, the BCLK pin, the GPIO pin or the output of the internal PLL, where the input to the PLL again can be derived from the MCLK pin, the BCLK or GPIO pins. Although using the PLL ensures the availability of a suitable clock signal, PLL use is not recommended for the lowest power settings. The PLL is highly programmable and can accept available input clocks in the range of 512 kHz to 50 MHz.

9.2 Functional Block Diagram

Figure 20 shows the basic functional blocks of the device.

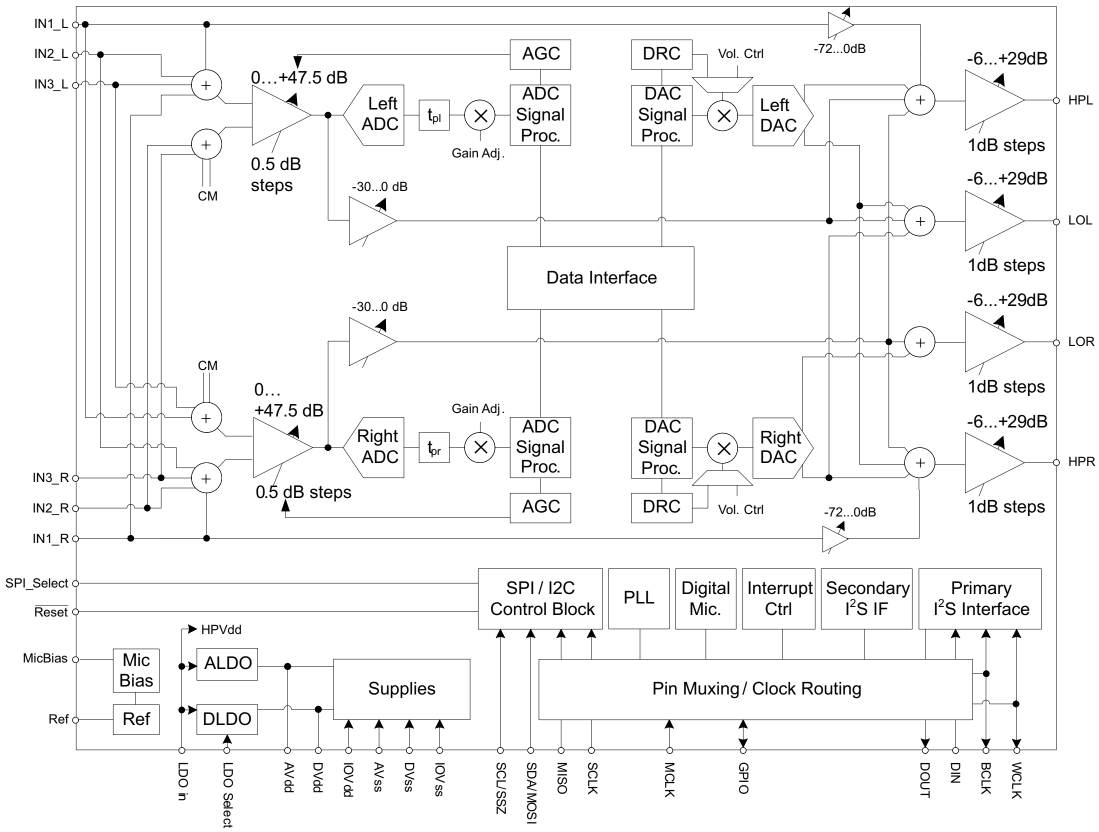


Figure 20. Block Diagram

9.3 Feature Description

9.3.1 Device Connections

9.3.1.1 Digital Pins

Only a small number of digital pins are dedicated to a single function; whenever possible, the digital pins have a default function, and also can be reprogrammed to cover alternative functions for various applications.

The fixed-function pins are Reset, LDO_Select and the SPI_Select pin, which are HW control pins. Depending on the state of SPI_Select, the two control-bus pins SCL/SS and SDA/MOSI are configured for either I²C or SPI protocol.

Other digital IO pins can be configured for various functions via register control. An overview of available functionality is given in *Multifunction Pins*.

9.3.1.1.1 Multifunction Pins

Table 1 shows the possible allocation of pins for specific functions. The PLL input, for example, can be programmed to be any of 4 pins (MCLK, BCLK, DIN, GPIO).

Feature Description (continued)

Table 1. Multifunction Pin Assignments

		1	2	3	4	5	6	7	8
	Pin Function	**MCLK**	**BCLK**	**WCLK**	**DIN MFP1**	**DOUT MFP2**	**DMDIN/ MFP3/ SCLK**	**DMCLK/ MFP4/ MISO**	**GPIO MFP5**
A	PLL Input	S(1)	S(2)		E				S(3)
B	Codec Clock Input	S(1),D(4)	S(2)						S(3)
C	I^2S BCLK input		S,D						
D	I^2S BCLK output		E(5)						
E	I^2S WCLK input			E, D					
F	I^2S WCLK output			E					
G	I^2S ADC word clock input						E		E
H	I^2S ADC WCLK out							E	E
I	I^2S DIN				E, D				
J	I^2S DOUT					E, D			
K	General Purpose Output I					E			
K	General Purpose Output II							E	
K	General Purpose Output III								E
L	General Purpose Input I				E				
L	General Purpose Input II						E		
L	General Purpose Input III								E
M	INT1 output					E		E	E
N	INT2 output					E		E	E
O	Digital Microphone Data Input				E		E		E
P	Digital Microphone Clock Output							E	E
Q	Secondary I^2S BCLK input						E		E
R	Secondary I^2S WCLK in						E		E
S	Secondary I^2S DIN						E		E
T	Secondary I^2S DOUT							E	
U	Secondary I^2S BCLK OUT					E		E	E
V	Secondary I^2S WCLK OUT					E		E	E
W	Headphone Detect Input						E		
X	Aux Clock Output					E		E	E

(1) S(1): The MCLK pin can drive the PLL and Codec Clock inputs **simultaneously**.
(2) S(2): The BCLK pin can drive the PLL and Codec Clock and audio interface bit clock inputs **simultaneously**.
(3) S(3): The GPIO/MFP5 pin can drive the PLL and Codec Clock inputs simultaneously.
(4) D: Default Function
(5) E: The pin is **exclusively** used for this function, no other function can be implemented with the same pin. (If GPIO/MFP5 has been allocated for General Purpose Output, it cannot be used as the INT1 output at the same time.)

9.3.1.2 Analog Pins

Analog functions can also be configured to a large degree. For minimum power consumption, analog blocks are powered down by default. The blocks can be powered up with fine granularity according to the application needs.

9.3.2 Analog Audio IO

The analog IO path of the TLV320AIC3204 features a large set of options for signal conditioning as well as signal routing:

- 6 analog inputs which can be mixed and-or multiplexed in single-ended and-or differential configuration
- 2 programmable gain amplifiers (PGA) with a range of 0 to +47.5dB
- 2 mixer amplifiers for analog bypass
- 2 low power analog bypass channels
- Mute function
- Automatic gain control (AGC)
- Built in microphone bias
- Stereo digital microphone interface
- Channel-to-channel phase adjustment
- Fast charge of ac-coupling capacitors
- Anti thump

9.3.2.1 Analog Low Power Bypass

The TLV320AIC3204 offers two analog-bypass modes. In either of the modes, an analog input signal can be routed from an analog input pin to an amplifier driving an analog output pin. Neither the ADC nor the DAC resources are required for such operation; this configuration supports low-power operation during analog-bypass mode.

In analog low-power bypass mode, line-level signals can be routed directly from the analog inputs IN1_L to the left headphone amplifier (HPL) and IN1_R to HPR.

9.3.2.2 ADC Bypass Using Mixer Amplifiers

In addition to the analog low-power bypass mode, another bypass mode uses the programmable gain amplifiers of the input stage in conjunction with a mixer amplifier. With this mode, microphone-level signals can be amplified and routed to the line or headphone outputs, fully bypassing the ADC and DAC.

To enable this mode, the mixer amplifiers are powered on via software command.

9.3.2.3 Headphone Outputs

The stereo headphone drivers on pins HPL and HPR can drive loads with impedances down to 16Ω in single-ended AC-coupled headphone configurations, or loads down to 32Ω in differential mode, where a speaker is connected between HPL and HPR. In single-ended drive configuration these drivers can drive up to 15mW power into each headphone channel while operating from 1.8V analog supplies. While running from the AV_{DD} supply, the output common-mode of the headphone driver is set by the common-mode setting of analog inputs in Page 1, Register 10, Bit D6, to allow maximum utilization of the analog supply range while simultaneously providing a higher output-voltage swing. In cases when higher output-voltage swing is required, the headphone amplifiers can run directly from the higher supply voltage on LDOIN input (up to 3.6V). To use the higher supply voltage for higher output signal swing, the output common-mode can be adjusted to either 1.25V, 1.5V or 1.65V by configuring Page 1, Register 10, Bits D5-D4. When the common-mode voltage is configured at 1.65V and LDOIN supply is 3.3V, the headphones can each deliver up to 40mW power into a 16Ω load.

The headphone drivers are capable of driving a mixed combination of DAC signal, left and right ADC PGA signal and line-bypass from analog input IN1_L and IN1_R by configuring Page 1, Register 12 and Page 1, Register 13 respectively. The ADC PGA signals can be attenuated up to 30dB before routing to headphone drivers by configuring Page 1, Register 24 and Page 1, Register 25. The analog line-input signals can be attenuated up to 72dB before routing by configuring Page 1, Register 22 and 23. The level of the DAC signal can be controlled using the digital volume control of the DAC in Page 0, Reg 65 and 66. To control the output-voltage swing of headphone drivers, the digital volume control provides a range of –6.0dB to +29.0dB (1) in steps of 1dB. These can be configured by programming Page 1, Register 16 and 17. These level controls are not meant to be used as dynamic volume control, but to set output levels during initial device configuration. Refer to for recommendations for using headphone volume control for achieving 0dB gain through the DAC channel with various configurations.

(1) If the device must be placed into 'mute' from the –6.0dB setting, set the device at a gain of –5.0dB first, then place the device into mute.

9.3.2.4 Line Outputs

The stereo line level drivers on LOL and LOR pins can drive a wide range of line level resistive impedances in the range of 600Ω to 10kΩ. The output common modes of line level drivers can be configured to equal either the analog input common-mode setting or to 1.65V. With output common-mode setting of 1.65V and DRVdd_HP supply at 3.3V the line-level drivers can drive up to 1Vrms output signal. The line-level drivers can drive out a mixed combination of DAC signal and attenuated ADC PGA signal. Signal mixing is register-programmable.

9.3.3 ADC

The TLV320AIC3204 includes a stereo audio ADC, which uses a delta-sigma modulator with a programmable oversampling ratio, followed by a digital decimation filter. The ADC supports sampling rates from 8kHz to 192kHz. In order to provide optimal system power management, the stereo recording path can be powered up one channel at a time, to support the case where only mono record capability is required.

The ADC path of the TLV320AIC3204 features a large set of options for signal conditioning as well as signal routing:

- Two ADCs
- Six analog inputs which can be mixed and-or multiplexed in single-ended and-or differential configuration
- Two programmable gain amplifiers (PGA) with a range of 0 to +47.5dB
- Two mixer amplifiers for analog bypass
- Two low power analog bypass channels
- Fine gain adjustment of digital channels with 0.1dB step size
- Digital volume control with a range of -12 to +20dB
- Mute function
- Automatic gain control (AGC)

In addition to the standard set of ADC features the TLV320AIC3204 also offers the following special functions:

- Built in microphone bias
- Stereo digital microphone interface
- Channel-to-channel phase adjustment
- Fast charge of ac-coupling capacitors
- Anti thump
- Adaptive filter mode

9.3.3.1 ADC Processing

The TLV320AIC3204 ADC channel includes a built-in digital decimation filter to process the oversampled data from the sigma-delta modulator to generate digital data at Nyquist sampling rate with high dynamic range. The decimation filter can be chosen from three different types, depending on the required frequency response, group delay and sampling rate.

9.3.3.1.1 ADC Processing Blocks

The TLV320AIC3204 offers a range of processing blocks which implement various signal processing capabilities along with decimation filtering. These processing blocks give users the choice of how much and what type of signal processing they may use and which decimation filter is applied.

The choice between these processing blocks is part of the PowerTune strategy to balance power conservation and signal-processing flexibility. Less signal-processing capability reduces the power consumed by the device. Table 2 gives an overview of the available processing blocks and their properties. The Resource Class Column (RC) gives an approximate indication of power consumption.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- Variable-tap FIR filter
- AGC

The processing blocks are tuned for common cases and can achieve high anti-alias filtering or low group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first order IIR, BiQuad and FIR filters have fully user-programmable coefficients. The Resource Class Column (RC) gives an approximate indication of power consumption.

Table 2. ADC Processing Blocks

Processing Blocks	Channel	Decimation Filter	1st Order IIR Available	Number BiQuads	FIR	Required AOSR Value	Resource Class
PRB_R1(1)	Stereo	A	Yes	0	No	128,64	6
PRB_R2	Stereo	A	Yes	5	No	128,64	8
PRB_R3	Stereo	A	Yes	0	25-Tap	128,64	8
PRB_R4	Right	A	Yes	0	No	128,64	3
PRB_R5	Right	A	Yes	5	No	128,64	4
PRB_R6	Right	A	Yes	0	25-Tap	128,64	4
PRB_R7	Stereo	B	Yes	0	No	64	3
PRB_R8	Stereo	B	Yes	3	No	64	4
PRB_R9	Stereo	B	Yes	0	20-Tap	64	4
PRB_R10	Right	B	Yes	0	No	64	2
PRB_R11	Right	B	Yes	3	No	64	2
PRB_R12	Right	B	Yes	0	20-Tap	64	2
PRB_R13	Stereo	C	Yes	0	No	32	3
PRB_R14	Stereo	C	Yes	5	No	32	4
PRB_R15	Stereo	C	Yes	0	25-Tap	32	4
PRB_R16	Right	C	Yes	0	No	32	2
PRB_R17	Right	C	Yes	5	No	32	2
PRB_R18	Right	C	Yes	0	25-Tap	32	2

(1) Default

For more detailed information see the *TLV320AIC3204 Application Reference Guide,* SLAA557.

9.3.4 DAC

The TLV320AIC3204 includes a stereo audio DAC supporting data rates from 8kHz to 192kHz. Each channel of the stereo audio DAC consists of a signal-processing engine with fixed processing blocks, a digital interpolation filter, multi-bit digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide enhanced performance at low sampling rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and signal images strongly suppressed within the audio band to beyond 20kHz. To handle multiple input rates and optimize power dissipation and performance, the TLV320AIC3204 allows the system designer to program the oversampling rates over a wide range from 1 to 1024. The system designer can choose higher oversampling ratios for lower input data rates and lower oversampling ratios for higher input data rates.

The TLV320AIC3204 DAC channel includes a built-in digital interpolation filter to generate oversampled data for the sigma-delta modulator. The interpolation filter can be chosen from three different types depending on required frequency response, group delay and sampling rate.

The DAC path of the TLV320AIC3204 features many options for signal conditioning and signal routing:

- 2 headphone amplifiers
  - Usable in single-ended or differential mode
  - Analog volume setting with a range of -6 to +29dB
  - Class-D mode
- 2 line-out amplifiers
  - Usable in single-ended or differential mode
  - Analog volume setting with a range of -6 to +29dB
- Digital volume control with a range of -63.5 to +24dB
- Mute function
- Dynamic range compression (DRC)

In addition to the standard set of DAC features the TLV320AIC3204 also offers the following special features:

- Built in sine wave generation (beep generator)
- Digital auto mute
- Adaptive filter mode

9.3.4.1 DAC Processing Blocks

The TLV320AIC3204 implements signal processing capabilities and interpolation filtering via processing blocks. These fixed processing blocks give users the choice of how much and what type of signal processing they may use and which interpolation filter is applied.

The choice between these processing blocks is part of the PowerTune strategy balancing power conservation and signal processing flexibility. Less signal processing capability will result in less power consumed by the device. Table 3 gives an overview over all available processing blocks of the DAC channel and their properties. The Resource Class Column (RC) gives an approximate indication of power consumption.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- 3D – Effect
- Beep Generator

The processing blocks are tuned for typical cases and can achieve high image rejection or low group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first-order IIR and biquad filters have fully user-programmable coefficients. The Resource Class Column (RC) gives an approximate indication of power consumption.

Table 3. Overview – DAC Predefined Processing Blocks

Processing Block No.	Interpolation Filter	Channel	1st Order IIR Available	Num. of Biquads	DRC	3D	Beep Generator	Resource Class
PRB_P1[(1)]	A	Stereo	No	3	No	No	No	8
PRB_P2	A	Stereo	Yes	6	Yes	No	No	12
PRB_P3	A	Stereo	Yes	6	No	No	No	10
PRB_P4	A	Left	No	3	No	No	No	4
PRB_P5	A	Left	Yes	6	Yes	No	No	6
PRB_P6	A	Left	Yes	6	No	No	No	6
PRB_P7	B	Stereo	Yes	0	No	No	No	6
PRB_P8	B	Stereo	No	4	Yes	No	No	8
PRB_P9	B	Stereo	No	4	No	No	No	8
PRB_P10	B	Stereo	Yes	6	Yes	No	No	10
PRB_P11	B	Stereo	Yes	6	No	No	No	8
PRB_P12	B	Left	Yes	0	No	No	No	3
PRB_P13	B	Left	No	4	Yes	No	No	4
PRB_P14	B	Left	No	4	No	No	No	4
PRB_P15	B	Left	Yes	6	Yes	No	No	6
PRB_P16	B	Left	Yes	6	No	No	No	4
PRB_P17	C	Stereo	Yes	0	No	No	No	3
PRB_P18	C	Stereo	Yes	4	Yes	No	No	6
PRB_P19	C	Stereo	Yes	4	No	No	No	4
PRB_P20	C	Left	Yes	0	No	No	No	2
PRB_P21	C	Left	Yes	4	Yes	No	No	3
PRB_P22	C	Left	Yes	4	No	No	No	2
PRB_P23	A	Stereo	No	2	No	Yes	No	8
PRB_P24	A	Stereo	Yes	5	Yes	Yes	No	12
PRB_P25	A	Stereo	Yes	5	Yes	Yes	Yes	12

(1) Default

For more detailed information see the *TLV320AIC3204 Application Reference Guide,* SLAA557.

9.3.5 PowerTune

The TLV320AIC3204 features PowerTune, a mechanism to balance power-versus-performance trade-offs at the time of device configuration. The device can be tuned to minimize power dissipation, to maximize performance, or to an operating point between the two extremes to best fit the application. The TLV320AIC3204 PowerTune modes are called PTM_R1 to PTM_R4 for the recording (ADC) path and PTM_P1 to PTM_P4 for the playback (DAC) path.

For more detailed information see the *TLV320AIC3204 Application Reference Guide,* SLAA557.

9.3.6 Digital Audio IO Interface

Audio data flows between the host processor and the TLV320AIC3204 on the digital audio data serial interface, or audio bus. This very flexible bus includes left or right-justified data options, support for I^2S or PCM protocols, programmable data length options, a TDM mode for multichannel operation, very flexible master-slave configurability for each bus clock line, and the ability to communicate with multiple devices within a system directly.

The audio bus of the TLV320AIC3204 can be configured for left or right-justified, I^2S, DSP, or TDM modes of operation, where communication with standard telephony PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits by configuring Page 0, Register 27, D(5:4). In addition, the word clock and bit clock can be independently configured in either Master or Slave mode, for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected ADC and DAC sampling frequencies.

The bit clock is used to clock in and clock out the digital audio data across the serial bus. When in Master mode, this signal can be programmed to generate variable clock pulses by controlling the bit-clock divider in Page 0, Register 30. The number of bit-clock pulses in a frame may need adjustment to accommodate various word lengths, and to support the case when multiple TLV320AIC3204s may share the same audio bus.

The TLV320AIC3204 also includes a feature to offset the position of start of data transfer with respect to the word-clock. Control the offset in terms of number of bit-clocks by programming Page 0, Register 28.

The TLV320AIC3204 also has the feature to invert the polarity of the bit-clock used to transfer the audio data as compared to the default clock polarity used. This feature can be used independently of the mode of audio interface chosen. Page 0, Register 29, D(3) configures bit clock polarity.

The TLV320AIC3204 further includes programmability (Page 0, Register 27, D(0)) to place the DOUT line into a hi-Z (3-state) condition during all bit clocks when valid data is not being sent. By combining this capability with the ability to program at what bit clock in a frame the audio data begins, time-division multiplexing (TDM) can be accomplished, enabling the use of multiple codecs on a single audio serial data bus. When the audio serial data bus is powered down while configured in master mode, the pins associated with the interface are put into a hi-Z output condition.

By default when the word-clocks and bit-clocks are generated by the TLV320AIC3204, these clocks are active only when the codec (ADC, DAC or both) are powered up within the device. This intermittent clock operation reduces power consumption. However, it also supports a feature when both the word clocks and bit-clocks can be active even when the codec in the device is powered down. This continuous clock feature is useful when using the TDM mode with multiple codecs on the same bus, or when word-clock or bit-clocks are used in the system as general-purpose clocks.

9.3.7 Clock Generation and PLL

The TLV320AIC3204 supports a wide range of options for generating clocks for the ADC and DAC sections as well as interface and other control blocks. The clocks for ADC and DAC require a source reference clock. This clock can be provided on variety of device pins such as MCLK, BCLK or GPI pins. The CODEC_CLKIN can then be routed through highly-flexible clock dividers to generate the various clocks required for the ADC and DAC sections. In the event that the desired audio clocks cannot be generated from the reference clocks on MCLK, BCLK or GPIO, the TLV320AIC3204 also provides the option of using the on-chip PLL which supports a wide range of fractional multiplication values to generate the required clocks. Starting from CODEC_CLKIN the TLV320AIC3204 provides several programmable clock dividers to help achieve a variety of sampling rates for ADC, DAC and clocks for the processing block.

To minimize power consumption, the system ideally provides a master clock that is a suitable integer multiple of the desired sampling frequencies. In such cases, internal dividers can be programmed to set up the required internal clock signals at very low power consumption. For cases where such master clocks are not available, the built-in PLL can be used to generate a clock signal that serves as an internal master clock. In fact, this master clock can also be routed to an output pin and may be used elsewhere in the system. The clock system is flexible enough that it even allows the internal clocks to be derived directly from an external clock source, while the PLL is used to generate some other clock that is only used outside the TLV320AIC3204.

For more detailed information see the *TLV320AIC3204 Application Reference Guide,* SLAA557.

9.3.8 Control Interfaces

The TLV320AIC3204 control interface supports SPI or I^2C communication protocols, with the protocol selectable using the SPI_SELECT pin. For SPI, SPI_SELECT should be tied high; for I^2C, SPI_SELECT should be tied low. Changing the state of SPI_SELECT during device operation is not recommended.

9.3.8.1 I²C Control

The TLV320AIC3204 supports the I^2C control protocol, and will respond to the I^2C address of 0011000. I^2C is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I^2C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pullup resistors, so the bus wires are HIGH when no device is driving them LOW. This circuit prevents two devices from conflicting; if two devices drive the bus simultaneously, there is no driver contention.

9.3.8.2 SPI Control

In the SPI control mode, the TLV320AIC3204 uses the pins SCL/$\overline{SS}$ as $\overline{SS}$, SCLK as SCLK, MISO as MISO, SDA/MOSI as MOSI; a standard SPI port with clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0). The SPI port allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master (in this case, the host processor) generates the synchronizing clock (driven onto SCLK) and initiates transmissions. The SPI slave devices (such as the TLV320AIC3204) depend on a master to start and synchronize transmissions. A transmission begins when initiated by an SPI master. The byte from the SPI master begins shifting in on the slave MOSI pin under the control of the master serial clock (driven onto SCLK). As the byte shifts in on the MOSI pin, a byte shifts out on the MISO pin to the master shift register.

For more detailed information see the *TLV320AIC3204 Application Reference Guide,* SLAA557.

9.4 Device Functional Modes

The following special functions are available to support advanced system requirements:

- Headset detection
- Interrupt generation
- Flexible pin multiplexing

For more detailed information see the *TLV320AIC3204 Application Reference Guide,* SLAA557.

9.5 Register Map

Table 4. Summary of Register Map

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
0	0	0x00	0x00	Page Select Register
0	1	0x00	0x01	Software Reset Register
0	2	0x00	0x02	Reserved Register
0	3	0x00	0x03	Reserved Register
0	4	0x00	0x04	Clock Setting Register 1, Multiplexers
0	5	0x00	0x05	Clock Setting Register 2, PLL P&R Values
0	6	0x00	0x06	Clock Setting Register 3, PLL J Values
0	7	0x00	0x07	Clock Setting Register 4, PLL D Values (MSB)
0	8	0x00	0x08	Clock Setting Register 5, PLL D Values (LSB)
0	9-10	0x00	0x09-0x0A	Reserved Register
0	11	0x00	0x0B	Clock Setting Register 6, NDAC Values
0	12	0x00	0x0C	Clock Setting Register 7, MDAC Values
0	13	0x00	0x0D	DAC OSR Setting Register 1, MSB Value
0	14	0x00	0x0E	DAC OSR Setting Register 2, LSB Value
0	15	0x00	0x0F	Reserved Register
0	16	0x00	0x10	Reserved Register
0	17	0x00	0x11	Reserved Register
0	18	0x00	0x12	Clock Setting Register 8, NADC Values
0	19	0x00	0x13	Clock Setting Register 9, MADC Values

Register Map (continued)

Table 4. Summary of Register Map (continued)

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
0	20	0x00	0x14	ADC Oversampling (AOSR) Register
0	21	0x00	0x15	Reserved Register
0	22	0x00	0x16	Reserved Register
0	23	0x00	0x17	Reserved Register
0	24	0x00	0x18	Reserved Register
0	25	0x00	0x19	Clock Setting Register 10, Multiplexers
0	26	0x00	0x1A	Clock Setting Register 11, CLKOUT M divider value
0	27	0x00	0x1B	Audio Interface Setting Register 1
0	28	0x00	0x1C	Audio Interface Setting Register 2, Data offset setting
0	29	0x00	0x1D	Audio Interface Setting Register 3
0	30	0x00	0x1E	Clock Setting Register 12, BCLK N Divider
0	31	0x00	0x1F	Audio Interface Setting Register 4, Secondary Audio Interface
0	32	0x00	0x20	Audio Interface Setting Register 5
0	33	0x00	0x21	Audio Interface Setting Register 6
0	34	0x00	0x22	Digital Interface Misc. Setting Register
0	35	0x00	0x23	Reserved Register
0	36	0x00	0x24	ADC Flag Register
0	37	0x00	0x25	DAC Flag Register 1
0	38	0x00	0x26	DAC Flag Register 2
0	39-41	0x00	0x27-0x29	Reserved Register
0	42	0x00	0x2A	Sticky Flag Register 1
0	43	0x00	0x2B	Interrupt Flag Register 1
0	44	0x00	0x2C	Sticky Flag Register 2
0	45	0x00	0x2D	Sticky Flag Register 3
0	46	0x00	0x2E	Interrupt Flag Register 2
0	47	0x00	0x2F	Interrupt Flag Register 3
0	48	0x00	0x30	INT1 Interrupt Control Register
0	49	0x00	0x31	INT2 Interrupt Control Register
0	50-51	0x00	0x32-0x33	Reserved Register
0	52	0x00	0x34	GPIO/MFP5 Control Register
0	53	0x00	0x35	DOUT/MFP2 Function Control Register
0	54	0x00	0x36	DIN/MFP1 Function Control Register
0	55	0x00	0x37	MISO/MFP4 Function Control Register
0	56	0x00	0x38	SCLK/MFP3 Function Control Register
0	57-59	0x00	0x39-0x3B	Reserved Registers
0	60	0x00	0x3C	DAC Signal Processing Block Control Register
0	61	0x00	0x3D	ADC Signal Processing Block Control Register
0	62	0x00	0x3E	Reserved Register
0	63	0x00	0x3F	DAC Channel Setup Register 1
0	64	0x00	0x40	DAC Channel Setup Register 2
0	65	0x00	0x41	Left DAC Channel Digital Volume Control Register
0	66	0x00	0x42	Right DAC Channel Digital Volume Control Register
0	67	0x00	0x43	Headset Detection Configuration Register
0	68	0x00	0x44	DRC Control Register 1
0	69	0x00	0x45	DRC Control Register 2

Register Map (continued)

Table 4. Summary of Register Map (continued)

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
0	70	0x00	0x46	DRC Control Register 3
0	71	0x00	0x47	Beep Generator Register 1
0	72	0x00	0x48	Beep Generator Register 2
0	73	0x00	0x49	Beep Generator Register 3
0	74	0x00	0x4A	Beep Generator Register 4
0	75	0x00	0x4B	Beep Generator Register 5
0	76	0x00	0x4C	Beep Generator Register 6
0	77	0x00	0x4D	Beep Generator Register 7
0	78	0x00	0x4E	Beep Generator Register 8
0	79	0x00	0x4F	Beep Generator Register 9
0	80	0x00	0x50	Reserved Register
0	81	0x00	0x51	ADC Channel Setup Register
0	82	0x00	0x52	ADC Fine Gain Adjust Register
0	83	0x00	0x53	Left ADC Channel Volume Control Register
0	84	0x00	0x54	Right ADC Channel Volume Control Register
0	85	0x00	0x55	ADC Phase Adjust Register
0	86	0x00	0x56	Left Channel AGC Control Register 1
0	87	0x00	0x57	Left Channel AGC Control Register 2
0	88	0x00	0x58	Left Channel AGC Control Register 3
0	89	0x00	0x59	Left Channel AGC Control Register 4
0	90	0x00	0x5A	Left Channel AGC Control Register 5
0	91	0x00	0x5B	Left Channel AGC Control Register 6
0	92	0x00	0x5C	Left Channel AGC Control Register 7
0	93	0x00	0x5D	Left Channel AGC Control Register 8
0	94	0x00	0x5E	Right Channel AGC Control Register 1
0	95	0x00	0x5F	Right Channel AGC Control Register 2
0	96	0x00	0x60	Right Channel AGC Control Register 3
0	97	0x00	0x61	Right Channel AGC Control Register 4
0	98	0x00	0x62	Right Channel AGC Control Register 5
0	99	0x00	0x63	Right Channel AGC Control Register 6
0	100	0x00	0x64	Right Channel AGC Control Register 7
0	101	0x00	0x65	Right Channel AGC Control Register 8
0	102	0x00	0x66	DC Measurement Register 1
0	103	0x00	0x67	DC Measurement Register 2
0	104	0x00	0x68	Left Channel DC Measurement Output Register 1
0	105	0x00	0x69	Left Channel DC Measurement Output Register 2
0	106	0x00	0x6A	Left Channel DC Measurement Output Register 3
0	107	0x00	0x6B	Right Channel DC Measurement Output Register 1
0	108	0x00	0x6C	Right Channel DC Measurement Output Register 2
0	109	0x00	0x6D	Right Channel DC Measurement Output Register 3
0	110-127	0x00	0x6E-0x7F	Reserved Register
1	0	0x01	0x00	Page Select Register
1	1	0x01	0x01	Power Configuration Register
1	2	0x01	0x02	LDO Control Register
1	3	0x01	0x03	Playback Configuration Register 1

Register Map (continued)

Table 4. Summary of Register Map (continued)

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
1	4	0x01	0x04	Playback Configuration Register 2
1	5-8	0x01	0x05-0x08	Reserved Register
1	9	0x01	0x09	Output Driver Power Control Register
1	10	0x01	0x0A	Common Mode Control Register
1	11	0x01	0x0B	Over Current Protection Configuration Register
1	12	0x01	0x0C	HPL Routing Selection Register
1	13	0x01	0x0D	HPR Routing Selection Register
1	14	0x01	0x0E	LOL Routing Selection Register
1	15	0x01	0x0F	LOR Routing Selection Register
1	16	0x01	0x10	HPL Driver Gain Setting Register
1	17	0x01	0x11	HPR Driver Gain Setting Register
1	18	0x01	0x12	LOL Driver Gain Setting Register
1	19	0x01	0x13	LOR Driver Gain Setting Register
1	20	0x01	0x14	Headphone Driver Startup Control Register
1	21	0x01	0x15	Reserved Register
1	22	0x01	0x16	IN1_L to HPL Volume Control Register
1	23	0x01	0x17	IN1_R to HPR Volume Control Register
1	24	0x01	0x18	Mixer Amplifier Left Volume Control Register
1	25	0x01	0x19	Mixer Amplifier Right Volume Control Register
1	26-50	0x01	0x1A-0x32	Reserved Register
1	51	0x01	0x33	MICBIAS Configuration Register
1	52	0x01	0x34	Left MICPGA Positive Terminal Input Routing Configuration Register
1	53	0x01	0x35	Reserved Register
1	54	0x01	0x36	Left MICPGA Negative Terminal Input Routing Configuration Register
1	55	0x01	0x37	Right MICPGA Positive Terminal Input Routing Configuration Register
1	56	0x01	0x38	Reserved Register
1	57	0x01	0x39	Right MICPGA Negative Terminal Input Routing Configuration Register
1	58	0x01	0x3A	Floating Input Configuration Register
1	59	0x01	0x3B	Left MICPGA Volume Control Register
1	60	0x01	0x3C	Right MICPGA Volume Control Register
1	61	0x01	0x3D	ADC Power Tune Configuration Register
1	62	0x01	0x3E	ADC Analog Volume Control Flag Register
1	63	0x01	0x3F	DAC Analog Gain Control Flag Register
1	64-70	0x01	0x40-0x46	Reserved Register
1	71	0x01	0x47	Analog Input Quick Charging Configuration Register
1	72-122	0x01	0x48-0x7A	Reserved Register
1	123	0x01	0x7B	Reference Power-up Configuration Register
1	124-127	0x01	0x7C-0x7F	Reserved Register
8	0	0x08	0x00	Page Select Register
8	1	0x08	0x01	ADC Adaptive Filter Configuration Register
8	2-7	0x08	0x02-0x07	Reserved
8	8-127	0x08	0x08-0x7F	ADC Coefficients Buffer-A C(0:29)
9-16	0	0x09-0x10	0x00	Page Select Register
9-16	1-7	0x09-0x10	0x01-0x07	Reserved
9-16	8-127	0x09-0x10	0x08-0x7F	ADC Coefficients Buffer-A C(30:255)

Register Map (continued)

Table 4. Summary of Register Map (continued)

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
26-34	0	0x1A-0x22	0x00	Page Select Register
26-34	1-7	0x1A-0x22	0x01-0x07	Reserved.
26-34	8-127	0x1A-0x22	0x08-0x7F	ADC Coefficients Buffer-B C(0:255)
44	0	0x2C	0x00	Page Select Register
44	1	0x2C	0x01	DAC Adaptive Filter Configuration Register
44	2-7	0x2C	0x02-0x07	Reserved
44	8-127	0x2C	0x08-0x7F	DAC Coefficients Buffer-A C(0:29)
45-52	0	0x2D-0x34	0x00	Page Select Register
45-52	1-7	0x2D-0x34	0x01-0x07	Reserved.
45-52	8-127	0x2D-0x34	0x08-0x7F	DAC Coefficients Buffer-A C(30:255)
62-70	0	0x3E-0x46	0x00	Page Select Register
62-70	1-7	0x3E-0x46	0x01-0x07	Reserved.
62-70	8-127	0x3E-0x46	0x08-0x7F	DAC Coefficients Buffer-B C(0:255)

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TLV320AIC3204 is a highly integrated stereo audio codec with integrated processing blocks and flexible digital audio interface options. It enables many different types of audio platforms having a need for stereo audio record and playback and needing to interface with other devices in the system over a digital audio interface.

10.2 Typical Application

Figure 21 shows a typical circuit configuration for a system using theTLV320AIC3204.

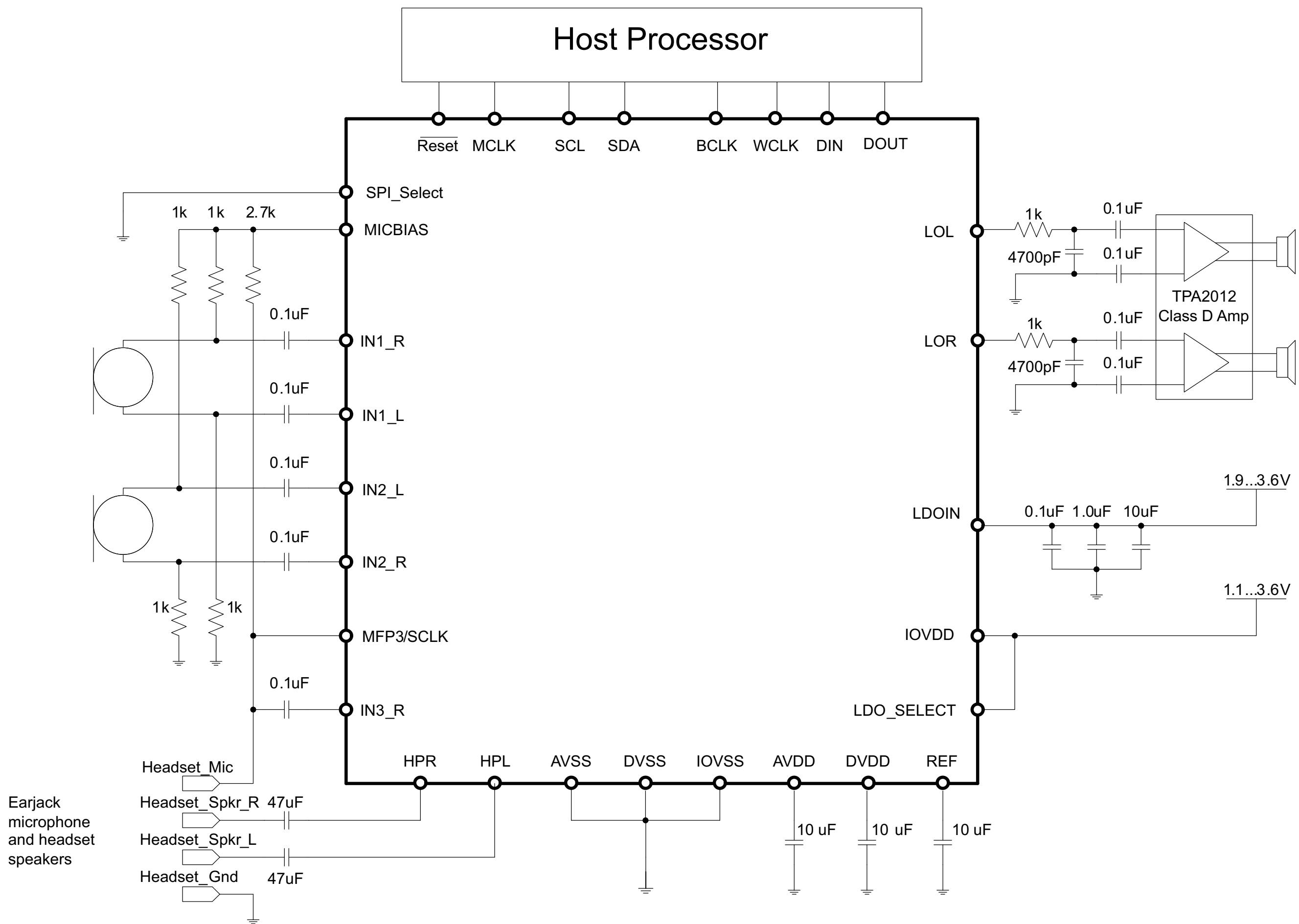


Figure 21. Typical Circuit Configuration

Typical Application (continued)

10.2.1 Design Requirements

10.2.1.1 Reference Filtering Capacitor

The TLV320AIC3204 has a built-in bandgap used to generate reference voltages and currents for the device. To achieve high SNR, the reference voltage on REF should be filtered using a 10-µF capacitor from REF terminal to ground.

10.2.1.2 MICBIAS

The TLV320AIC3204 has a built-in bias voltage output for biasing of microphones. No intentional capacitors should be connected directly to the MICBIAS output for filtering.

10.2.2 Detailed Design Procedures

10.2.2.1 Analog Input Connection

The analog inputs to TLV320AIC3204 should be ac-coupled to the device terminals to allow decoupling of signal source's common mode voltage with that of TLV320AIC3204's common mode voltage. The input coupling capacitor in combination with the selected input impedance of TLV320AIC3204 forms a high-pass filter.

$$F_c = 1/(2 \times \pi \times R_{eq}C_c) \quad (1)$$

$$C_c = 1/(2 \times \pi \times R_{eq}F_c) \quad (2)$$

For high fidelity audio recording application it is desirable to keep the cutoff frequency of the high pass filter as low as possible. For single-ended input mode, the equivalent input resistance R_{eq} can be calculated as

$$R_{eq} = R_{in} \times (1 + 2g)/(1+g) \quad (3)$$

where g is the analog PGA gain calculated in linear terms.

$$g = 10000 \times 2^{floor(G/6)}/R_{in} \quad (4)$$

where G is the analog PGA gain programmed in P1_R59-R60 (in dB) and R_{in} is the value of the resistor programmed in P1_R52-R57 and assumes $R_{in} = R_{cm}$ (as defined in P1_R52-R57).

For differential input mode, R_{eq} of the half circuit can be calculated as:

$$R_{eq} = R_{in} \quad (5)$$

where R_{in} is the value of the resistor programmed in P1_R52-R57, assuming symmetrical inputs.

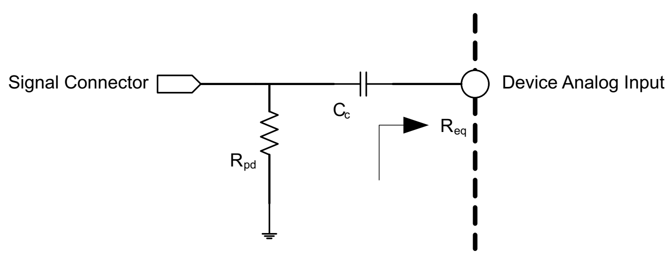


Figure 22. Analog Input Connection With Pull-down Resistor

When the analog signal is connected to the system through a connector such as audio jack, it is recommended to put a pull-down resistor on the signal as shown in Figure 22. The pulldown resistor helps keep the signal grounded and helps improve noise immunity when no source is connected to the connector. The pulldown resistor value should be chosen large enough to avoid loading of signal source.

Each analog input of the TLV320AIC3204 is capable of handling signal amplitude of 0.5 Vrms. If the input signal source can drive signals higher than the maximum value, an external resistor divider network as shown in Figure 23 should be used to attenuate the signal to less than 0.5Vrms before connecting the signal to the device. The resistor values of the network should be chosen to provide desired attenuation as well as Equation 6.

$$R_1 || R_2 << R_{eq} \quad (6)$$

Typical Application (continued)

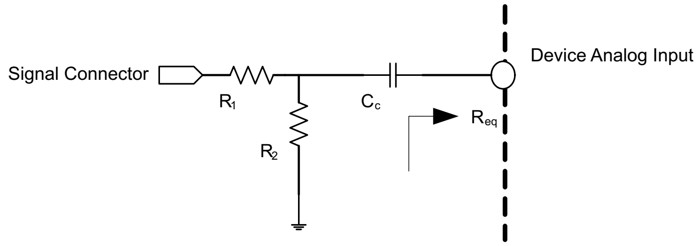


Figure 23. Analog Input Connection With Resistor Divider Network

Whenever any of the analog input terminals IN1_L, IN2_L, IN3_L, IN1_R, IN2_R or IN3_R are not used in an application, it is recommended to short the unused input terminals together (if convenient) and connect them to ground using a small capacitor (example 0.1 µF).

10.2.2.2 Analog Output Connection

The line outputs of the TLV320AIC3204 drive a signal biased around the device common mode voltage. To avoid loading the common mode with the load, it is recommended to connect the single-ended load through an ac-coupling capacitor. The ac-coupling capacitor in combination with the load impedance forms a high pass filter.

$$F_c = 1/(2 \times \pi \times R_L C_c) \quad (7)$$

$$C_c = 1/(2 \times \pi \times R_L F_c) \quad (8)$$

For high fidelity playback, the cutoff frequency of the resultant high-pass filter should be kept low. For example with R_L of 10 kΩ, using 1-µF coupling capacitor results in a cut-off frequency of 8 Hz.

For differential lineout configurations, the load should be directly connected between the differential outputs, with no coupling capacitor.

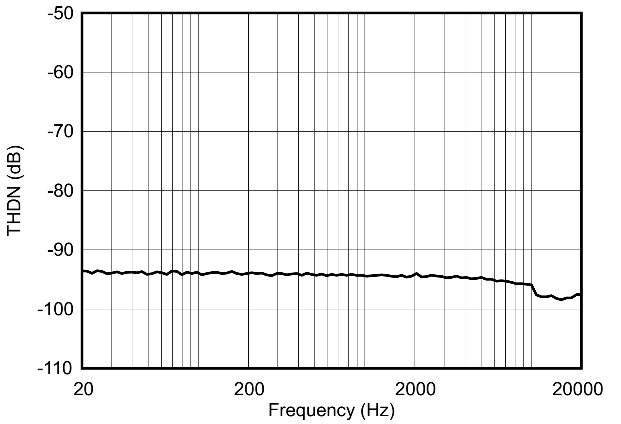
Whenever any of the analog output terminals LOL, LOR, HPL or HPR are not used in an application, they should be left open or not connected.

Typical Application (continued)

10.2.3 Application Curves

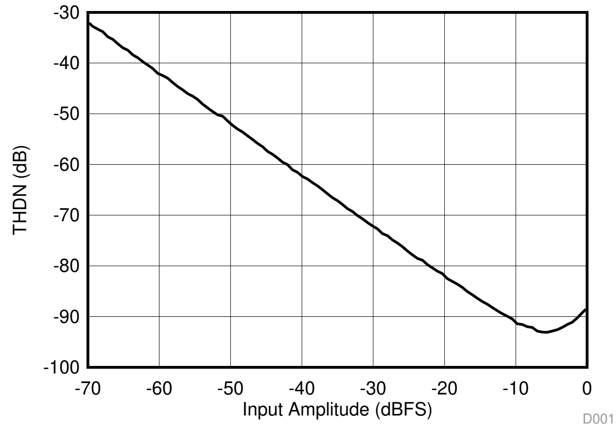
Figure 24 shows the excellent low-distortion performance of the TLV320AIC3204 in a system over the 20-Hz to 20-kHz audio spectrum.

Figure 25 shows the distortion performance of the TLV320AIC3204 in a system over the input amplitude range.



Differential Lineout R_{load} = 10 kΩ CM = 0.9 V
Input Amplitude = -3 dBFS

Figure 24. Total Harmonic Distortion + Noise vs Input Frequency



Differential Lineout R_{load} = 10 kΩ CM = 0.9 V
Frequency = 997 Hz

Figure 25. Total Harmonic Distortion + Noise vs Input Amplitude

11 Power Supply Recommendations

Device power consumption largely depends on PowerTune configuration.

The TLV320AIC3204 needs several power supplies for its operation.

The AVDD and LDOIN power inputs are used to power the analog circuits including analog to digital converters, digital to analog converters, programmable gain amplifiers, headphone amplifiers etc. The analog blocks in TLV320AIC3204 have high power supply rejection ratio, however it is recommended that these supplies be powered by well regulated power supplies like low dropout regulators (LDO) for optimal performance. When these power terminals are driven from a common power source, the current drawn from the source will depend upon blocks enabled inside the device. However as an example when all the internal blocks powered are enabled the source should be able to deliver 150mA of current.

The DVDD powers the digital core of TLV320AIC3204, including the audio serial interface, control interfaces (SPI or I2C), clock generation and PLL. The DVDD power can be driven by high efficiency switching regulators or low drop out regulators. When the PRB modes are used then the peak current load on DVDD supply source could be approximately 20 mA.

The IOVDD powers the digital input and digital output buffers of TLV320AIC3204. The current consumption of this power depends on configuration of digital terminals as inputs or outputs. When the digital terminals are configured as outputs, the current consumption would depend on switching frequency of the signal and the load on the output terminal, which depends on board design and input capacitance of other devices connected to the signal.

Refer to Figure 21 for recommendations on decoupling capacitors.

Refer to the application note SLAA492 for power supply sequencing information.

For more detailed information, see the *TLV320AIC3204 Application Reference Guide,* SLAA557.

12 Layout

12.1 Layout Guidelines

Each system design and PCB layout is unique. The layout should be carefully reviewed in the context of a specific PCB design. However, the following guidelines can optimize TLV320AIC3204 performance:

- Connect the thermal pad to ground.
- The decoupling capacitors for the power supplies should be placed close to the device terminals. Figure 21 shows the recommended decoupling capacitors for the TLV320AIC3204.
- The TLV320AIC3204 internal voltage references must be filtered using external capacitors. Place the filter capacitors on REF near the device terminals for optimal performance.
- For analog differential audio signals, the signals should be routed differentially on the PCB for better noise immunity. Avoid crossing of digital and analog signals to avoid undesirable crosstalk.

12.2 Layout Example

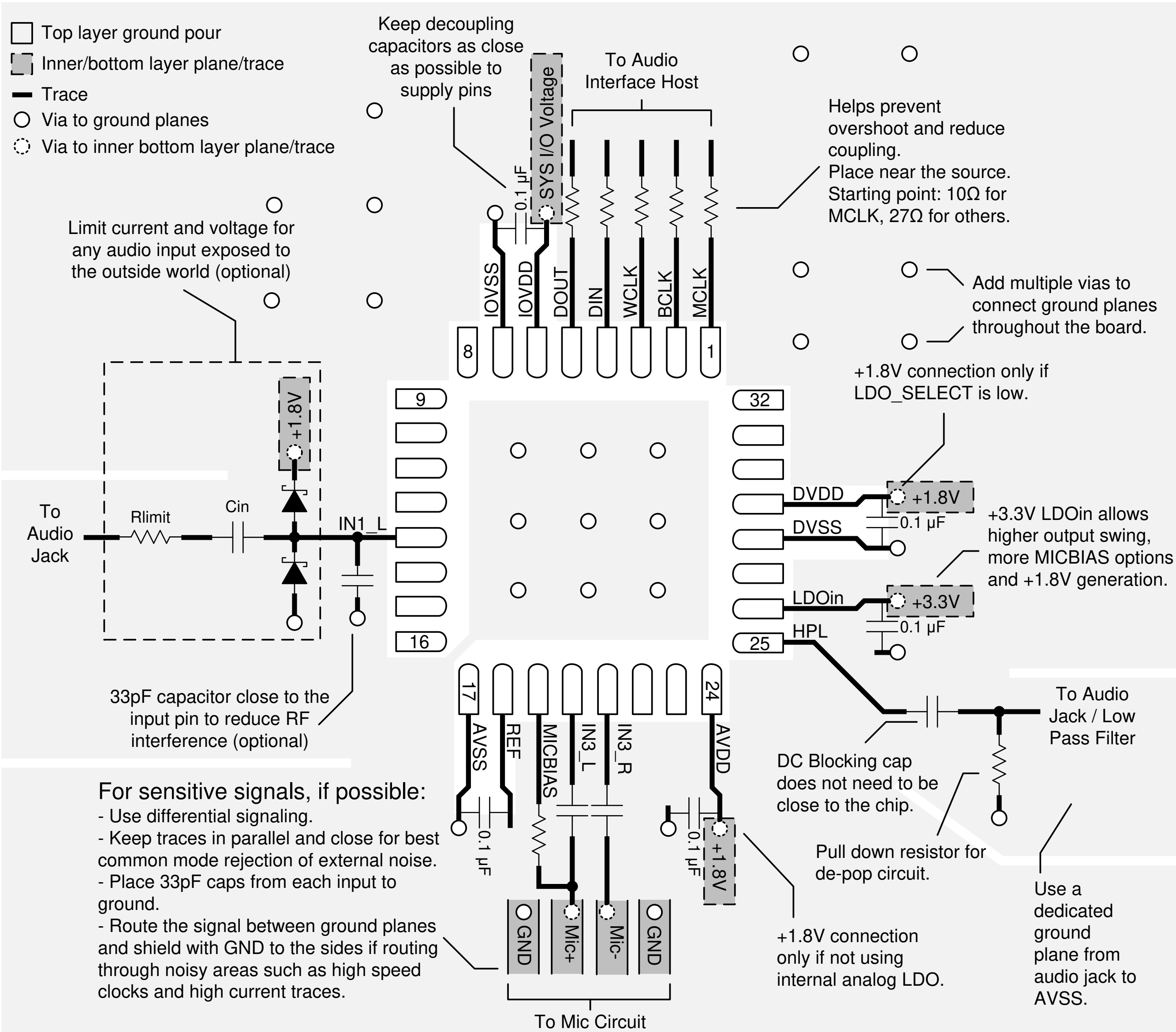


Figure 26. TLV320AIC3204 Layout

Example layout views can be found in the EVM User Guide:

- http://www.ti.com/tool/TLV320AIC3204EVM-K

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

Texas Instruments, *TLV320AIC32x4 Power Supply Sequencing* application report

Texas Instruments, *Core Voltage Accumulation* application report

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.4 Trademarks

PowerTune, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA02197IRHBR	ACTIVE	VQFN	RHB	32	3000	TBD	Call TI	Call TI	-40 to 85		Samples
TLV320AIC3204IRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AIC 3204	Samples
TLV320AIC3204IRHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AIC 3204	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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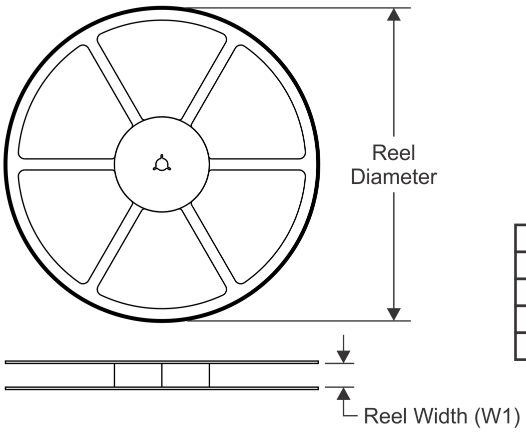
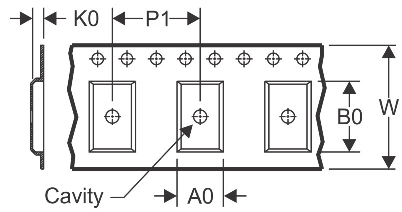
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

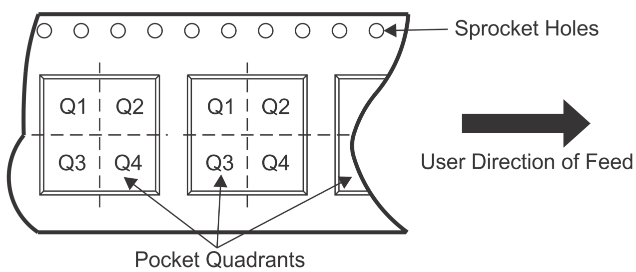


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

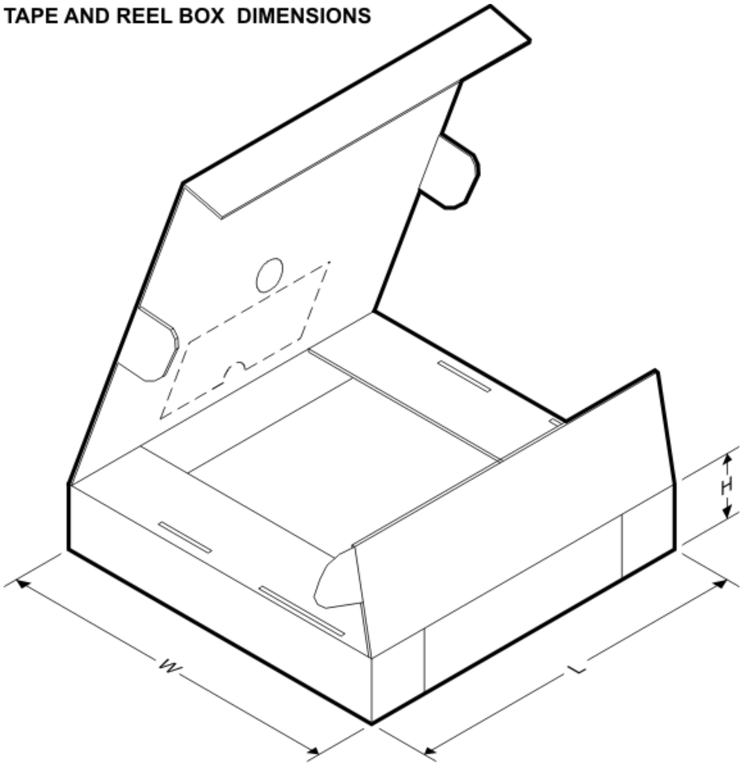
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV320AIC3204IRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TLV320AIC3204IRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV320AIC3204IRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
TLV320AIC3204IRHBT	VQFN	RHB	32	250	210.0	185.0	35.0

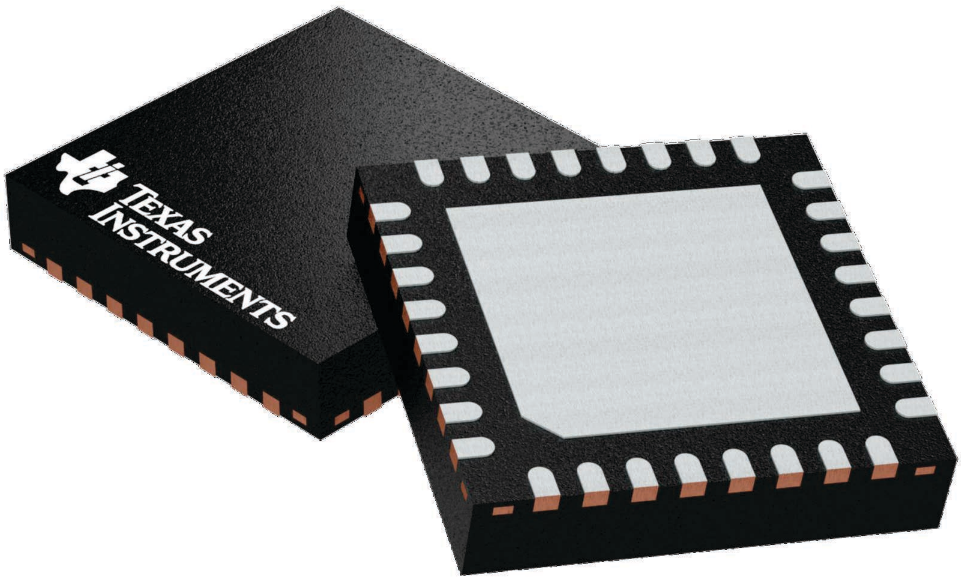
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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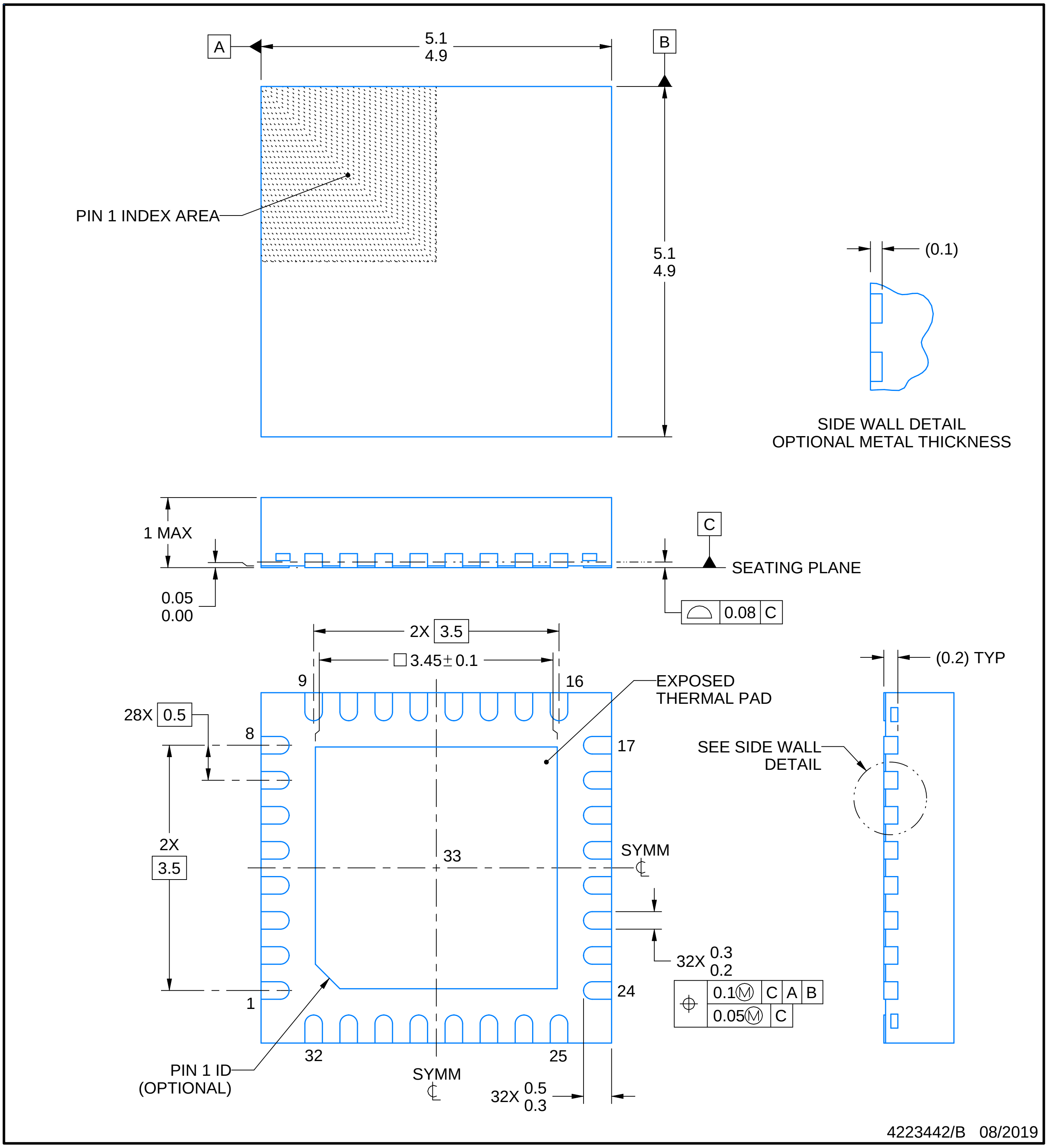
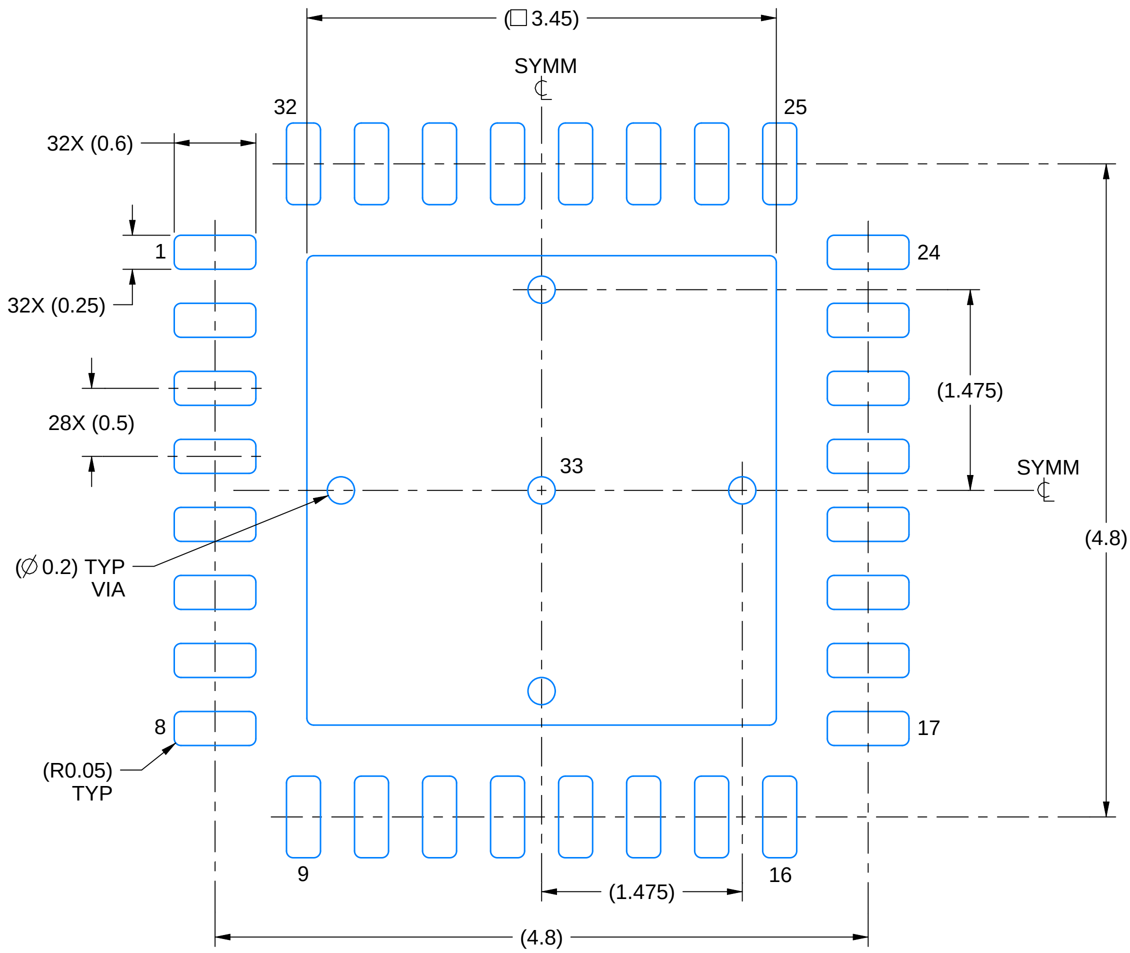
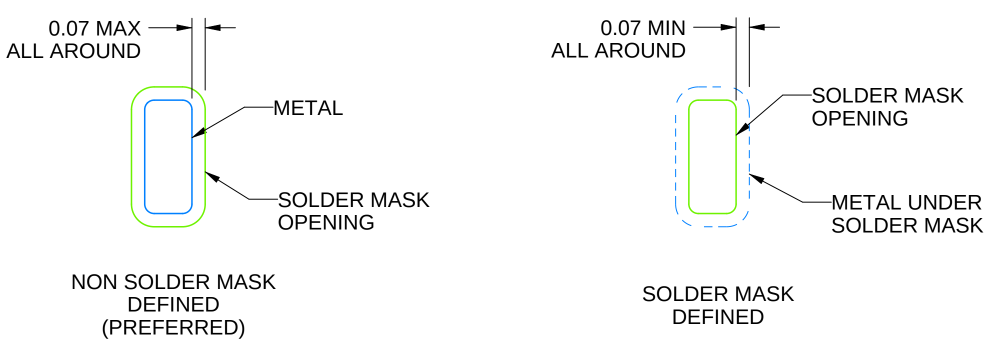


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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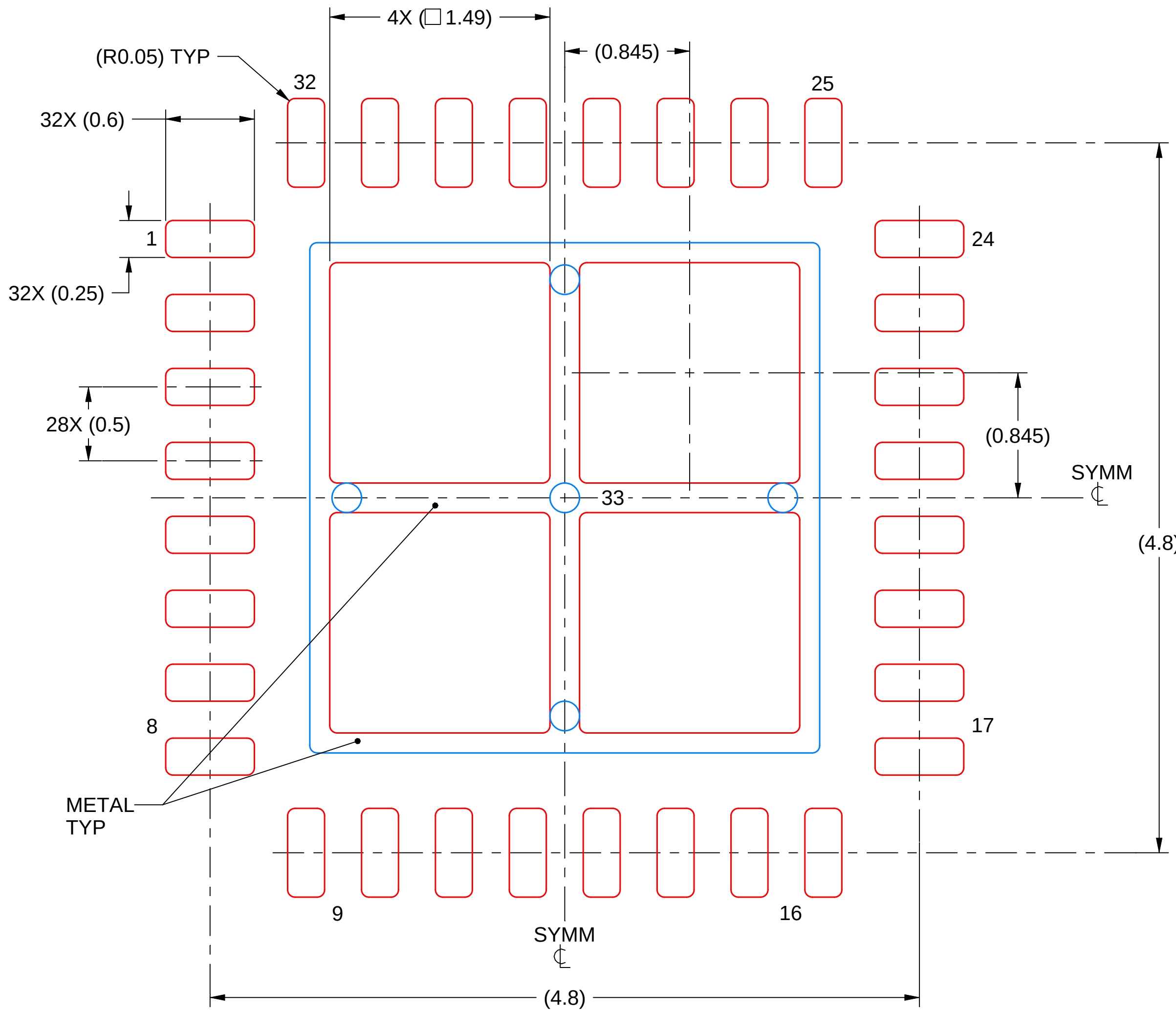
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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