TSL2561

Light-to-Digital Converter

General Description

The TSL2561 are light-to-digital converters that transform light intensity to a digital signal output capable of direct I^2C interface. Each device combines one broadband photodiode (visible plus infrared) and one infrared-responding photodiode on a single CMOS integrated circuit capable of providing a near-photopic response over an effective 20-bit dynamic range (16-bit resolution). Two integrating ADCs convert the photodiode currents to a digital output that represents the irradiance measured on each channel. This digital output can be input to a microprocessor where illuminance (ambient light level) in lux is derived using an empirical formula to approximate the human eye response. The TSL2561 device supports a traditional level style interrupt that remains asserted until the firmware clears it.

While useful for general purpose light sensing applications, the TSL2561 devices are designed particularly for display panels (LCD, OLED, etc.) with the purpose of extending battery life and providing optimum viewing in diverse lighting conditions. Display panel backlighting, which can account for up to 30 to 40 percent of total platform power, can be automatically managed. Both devices are also ideal for controlling keyboard illumination based upon ambient lighting conditions. Illuminance information can further be used to manage exposure control in digital cameras. The TSL2561 devices are ideal in notebook/tablet PCs, LCD monitors, flat-panel televisions, cell phones, and digital cameras. In addition, other applications include street light control, security lighting, sunlight harvesting, machine vision, and automotive instrumentation clusters.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TSL2561, Light-to-Digital Converter is listed below:

Figure 1:
Added Value of Using TSL2561

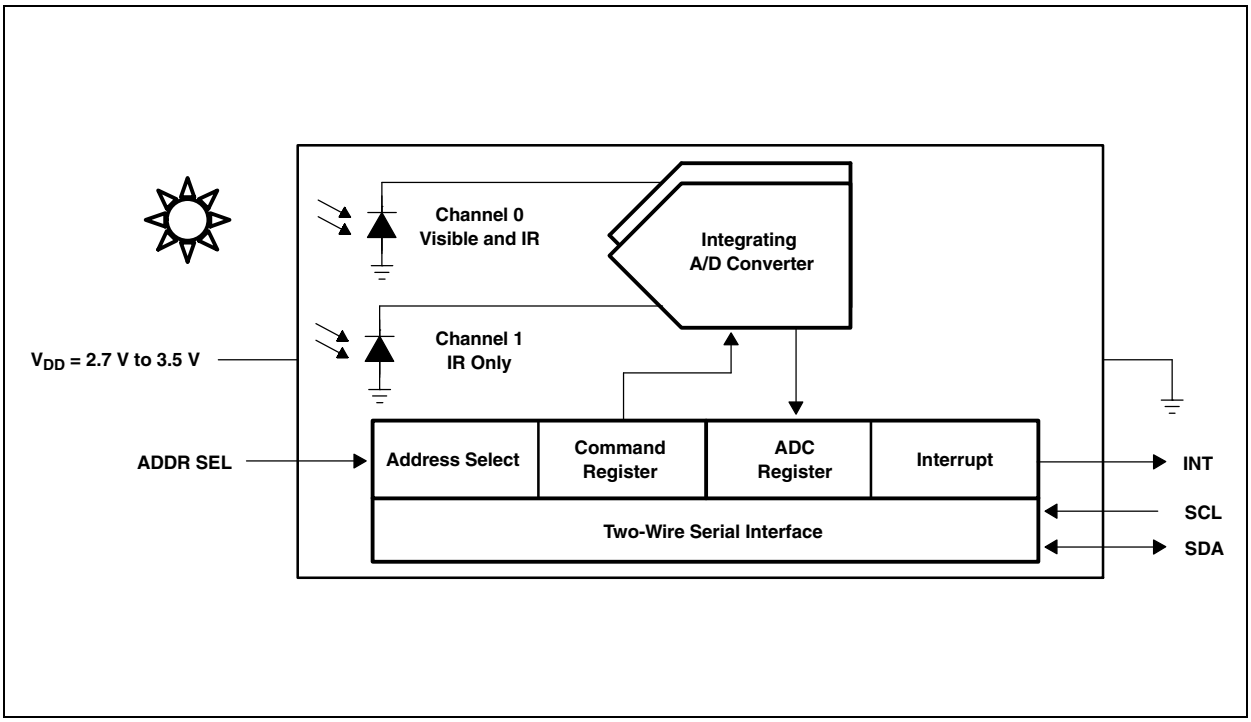
Benefits	Features
• Enables Operation in IR Light Environments	• Patented Dual-Diode Architecture
• Enables Dark Room to High Lux Sunlight Operation	• 1M:1 Dynamic Range
• Reduces Micro-Processor Interrupt Overhead	• Programmable Interrupt Function
• Digital Interface is Less Susceptible to Noise	• I^2C Digital Interface
• Reduces Board Space Requirements while Simplifying Designs	• Available in 2.6mm x 3.8mm TMB Packages

- Approximates Human Eye Response
- Programmable Interrupt Function with User-Defined Upper and Lower Threshold Settings
- 16-Bit Digital Output with I^2C Fast-Mode at 400kHz
- Programmable Analog Gain and Integration Time Supporting 1,000,000-to-1 Dynamic Range
- Automatically Rejects 50/60Hz Lighting Ripple
- Low Active Power (0.75mW typical) with Power Down Mode

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
TSL2561 Block Diagram



Detailed Description

The TSL2561 is a second-generation ambient light sensor device. It contains two integrating analog-to-digital converters (ADC) that integrate currents from two photodiodes. Integration of both channels occurs simultaneously. Upon completion of the conversion cycle, the conversion result is transferred to the Channel 0 and Channel 1 data registers, respectively. The transfers are double-buffered to ensure that the integrity of the data is maintained. After the transfer, the device automatically begins the next integration cycle.

Communication to the device is accomplished through a standard, two wire I^2C serial bus. Consequently, the TSL2561 device can be easily connected to a microcontroller or embedded controller. No external circuitry is required for signal conditioning, thereby saving PCB real estate as well. Since the output of the TSL2561 device is digital, the output is effectively immune to noise when compared to an analog signal.

The TSL2561 device also supports an interrupt feature that simplifies and improves system efficiency by eliminating the need to poll a sensor for a light intensity value. The primary purpose of the interrupt function is to detect a meaningful change in light intensity. The concept of a *meaningful change* can be defined by the user both in terms of light intensity and time, or persistence, of that change in intensity. The TSL2561 device has the ability to define a threshold above and below the current light level. An interrupt is generated when the value of a conversion exceeds either of these limits.

Pin Assignments

The TSL2561 pin assignments are described below:

Figure 3:
Pin Diagram of Package T 6-Lead TMB (Top View)

Package T 6-Lead TMB:
Package drawings are not to scale

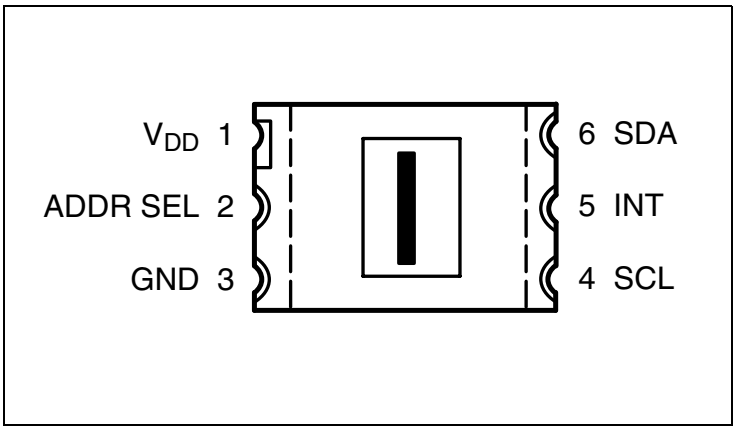


Figure 4:
Terminal Functions

Terminal		Type	Description
Name	Pin No.		
ADDR SEL	2	I	I^2C address select - three-state
GND	3		Power supply ground. All voltages are referenced to GND.
INT	5	O	Interrupt - open drain output (active low)
SCL	4	I	I^2C serial clock input terminal
SDA	6	I/O	I^2C serial data I/O terminal
V_{DD}	1		Supply voltage

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings over Operating Free-Air Temperature Range (unless otherwise noted)

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage [1]		3.8	V
V_O	Digital output voltage range	-0.5	3.8	V
I_O	Digital output current	-1	20	mA
T_{strg}	Storage temperature range	-40	85	°C
ESD_{HBM}	ESD tolerance, human body model	±2000		V

Note(s):

1. All voltages are with respect to GND.

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Unit
V_{DD}	Supply voltage	2.7	3	3.6	V
T_A	Operating free-air temperature	-30		70	°C
V_{IL}	SCL, SDA input low voltage	-0.5		0.8	V
V_{IH}	SCL, SDA input high voltage	2.1		3.6	V

Figure 7:
Electrical Characteristics over Recommended Operating Free-Air Temperature Range (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Active		0.24	0.6	mA
		Power down		3.2	15	µA
V_{OL}	INT, SDA output low voltage	3mA sink current	0		0.4	V
		6mA sink current	0		0.6	V
I_{LEAK}	Leakage current		-5		5	µA

Figure 8:
Operating Characteristics, High Gain (16×), V_{DD} = 3V, T_A = 25°C (unless otherwise noted) (1), (2), (3), (4)

Symbol	Parameter	Test Conditions	Channel	TSL2561T			Unit
				Min	Typ	Max	
f_{OSC}	Oscillator frequency			690	735	780	kHz
	Dark ADC count value	E_e = 0, T_{int} = 402ms	Ch0	0		4	counts
			Ch1	0		4	
	Full scale ADC count value (5)	T_{int} > 178ms	Ch0			65535	counts
			Ch1			65535	
		T_{int} = 101ms	Ch0			37177	
			Ch1			37177	
		T_{int} = 13.7ms	Ch0			5047	
			Ch1			5047	
	ADC count value	λ_p = 640nm, T_{int} = 101ms E_e = 36.3µW/cm^2	Ch0	750	1000	1250	counts
			Ch1		200		
		λ_p = 940nm, T_{int} = 101ms E_e = 119µW/cm^2	Ch0	700	1000	1300	
			Ch1		820		
		λ_p = 640nm, T_{int} = 101ms E_e = 41µW/cm^2	Ch0				counts
			Ch1				
		λ_p = 940nm, T_{int} = 101ms E_e = 135µW/cm^2	Ch0				
			Ch1				
	ADC count value ratio: Ch1/Ch0	λ_p = 640nm, T_{int} = 101ms		0.15	0.20	0.25	
		λ_p = 940nm, T_{int} = 101ms		0.69	0.82	0.95	
R_e	Irradiance responsivity	λ_p = 640nm, T_{int} = 101ms	Ch0		27.5		counts/ (µW/cm^2)
			Ch1		5.5		
		λ_p = 940nm, T_{int} = 101ms	Ch0		8.4		
			Ch1		6.9		

Symbol	Parameter	Test Conditions	Channel	TSL2561T			Unit
				Min	Typ	Max	
R_V	Illuminance responsivity	Fluorescent light source: T_{int} = 402ms	Ch0		36		counts/lux
			Ch1		4		
		Incandescent light source: T_{int} = 402ms	Ch0		144		
			Ch1		72		
	ADC count value ratio: Ch1/Ch0	Fluorescent light source: T_{int} = 402ms			0.11		
		Incandescent light source: T_{int} = 402ms			0.5		
R_V	Illuminance responsivity, low gain mode (6)	Fluorescent light source: T_{int} = 402ms	Ch0		2.3		counts/lux
			Ch1		0.25		
		Incandescent light source: T_{int} = 402ms	Ch0		9		
			Ch1		4.5		
	(Sensor Lux)/(actual Lux), high gain mode (7)	Fluorescent light source: T_{int} = 402ms		0.65	1	1.35	
		Incandescent light source: T_{int} = 402ms		0.60	1	1.40	

Note(s):

1. Optical measurements are made using small-angle incident radiation from light-emitting diode optical sources. Visible 640nm LEDs and infrared 940nm LEDs are used for final product testing for compatibility with high-volume production.
2. The 640nm irradiance E_e is supplied by an AlInGaP light-emitting diode with the following characteristics: peak wavelength λ_p = 640nm and spectral halfwidth $\Delta\lambda½$ = 17nm.
3. The 940nm irradiance E_e is supplied by a GaAs light-emitting diode with the following characteristics: peak wavelength λ_p = 940nm and spectral halfwidth $\Delta\lambda½$ = 40nm.
4. Integration time T_{int}, is dependent on internal oscillator frequency (f_{osc}) and on the integration field value in the timing register as described in the *Register Set* section. For nominal f_{osc} = 735kHz, nominal T_{int} = (number of clock cycles)/f_{osc}.
   Field value 00: T_{int} = (11 × 918)/f_{osc} = 13.7ms
   Field value 01: T_{int} = (81 × 918)/f_{osc} = 101ms
   Field value 10: T_{int} = (322 × 918)/f_{osc} = 402ms
   Scaling between integration times vary proportionally as follows: 11/322 = 0.034 (field value 00), 81/322 = 0.252 (field value 01), and 322/322 = 1 (field value 10).
5. Full scale ADC count value is limited by the fact that there is a maximum of one count per two oscillator frequency periods and also by a 2-count offset.
   Full scale ADC count value = ((number of clock cycles)/2 – 2)
   Field value 00: Full scale ADC count value = ((11 × 918)/2 – 2) = 5047
   Field value 01: Full scale ADC count value = ((81 × 918)/2 – 2) = 37177
   Field value 10: Full scale ADC count value = 65535, which is limited by 16-bit register. This full scale ADC count value is reached for 131074 clock cycles, which occurs for T_{int} = 178ms for nominal f_{osc} = 735kHz.

6. Low gain mode has 16× lower gain than high gain mode: (1/16 = 0.0625).
7. The sensor Lux is calculated using the empirical formula shown in Calculating Lux of this data sheet based on measured Ch0 and Ch1 ADC count values for the light source specified. Actual Lux is obtained with a commercial luxmeter. The range of the (sensor Lux) / (actual Lux) ratio is estimated based on the variation of the 640nm and 940nm optical parameters. Devices are not 100% tested with fluorescent or incandescent light sources.

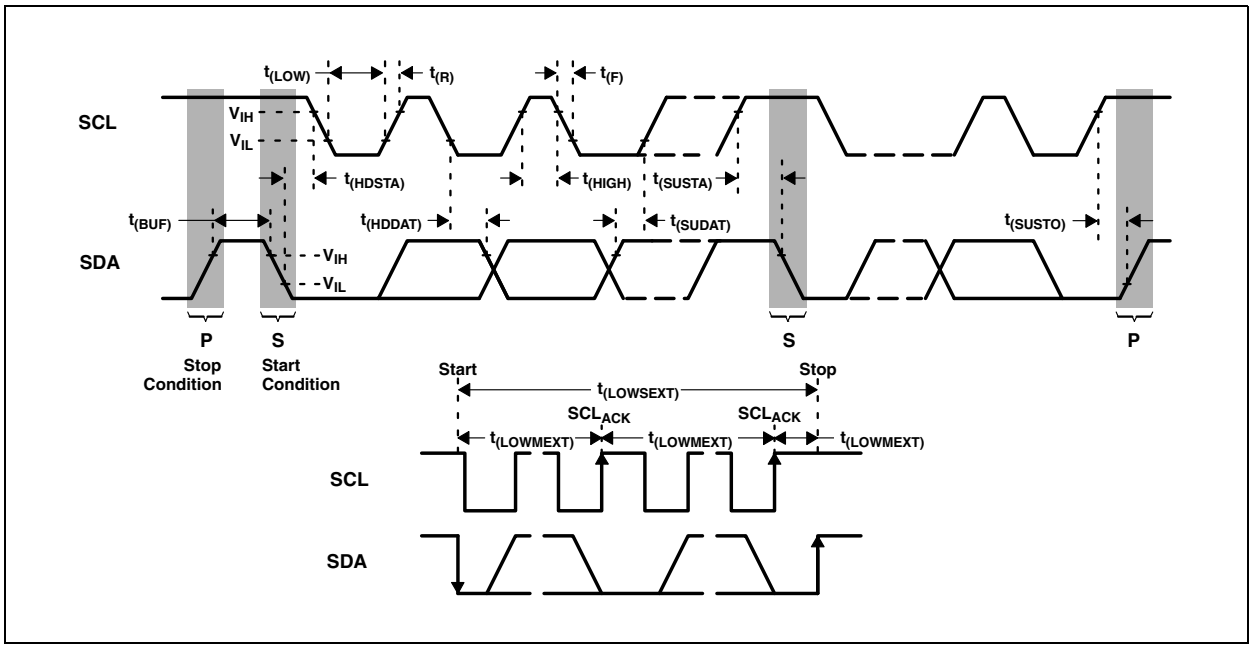
Figure 9:
AC Electrical Characteristics, V_{DD} = 3V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter (1)	Test Conditions	Min	Typ	Max	Unit
$t_{(CONV)}$	Conversion time		12	100	400	ms
$f_{(SCL)}$	Clock frequency (I^2C)		0		400	kHz
$t_{(BUF)}$	Bus free time between start and stop condition		1.3			µs
$t_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated.		0.6			µs
$t_{(SUSTA)}$	Repeated start condition setup time		0.6			µs
$t_{(SUSTO)}$	Stop condition setup time		0.6			µs
$t_{(HDDAT)}$	Data hold time		0		0.9	µs
$t_{(SUDAT)}$	Data setup time		100			ns
$t_{(LOW)}$	SCL clock low period		1.3			µs
$t_{(HIGH)}$	SCL clock high period		0.6			µs
t_F	Clock/data fall time				300	ns
t_R	Clock/data rise time				300	ns
C_i	Input pin capacitance				10	pF

Note(s):

1. Specified by design and characterization; not production tested.

Figure 10:
Timing Diagrams



Typical Characteristics

Figure 11:
Spectral Responsivity

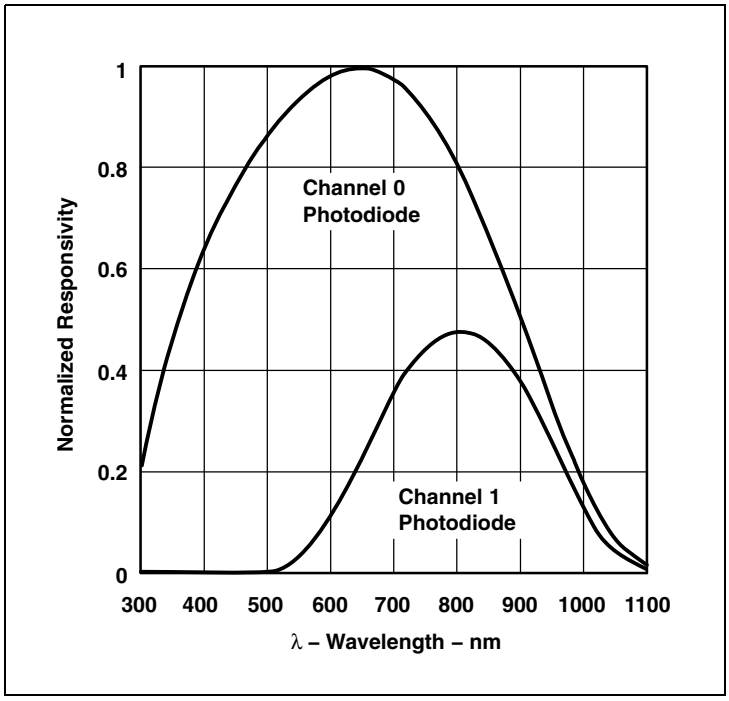
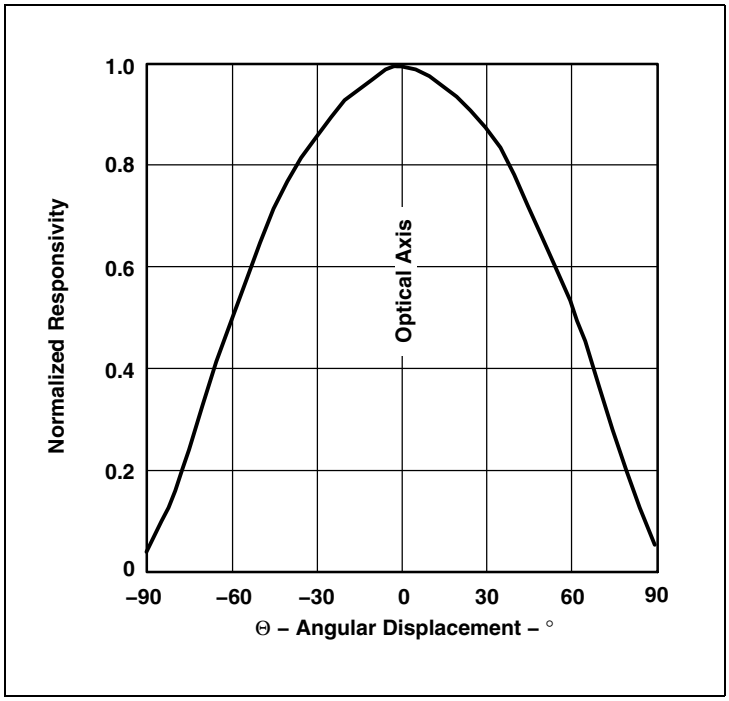


Figure 12:
Normalized Responsivity vs. Angular Displacement - T Package



Principles of Operation

Analog-to-Digital Converter

The TSL2561 contains two integrating analog-to-digital converters (ADC) that integrate the currents from the channel 0 and channel 1 photodiodes. Integration of both channels occurs simultaneously, and upon completion of the conversion cycle the conversion result is transferred to the channel 0 and channel 1 data registers, respectively. The transfers are double buffered to ensure that invalid data is not read during the transfer. After the transfer, the device automatically begins the next integration cycle.

Digital Interface

Interface and control of the TSL2561 is accomplished through a two-wire serial interface to a set of registers that provide access to device control functions and output data. The serial interface is compatible with I^2C bus Fast-Mode. The TSL2561 offers three slave addresses that are selectable via an external pin (ADDR SEL). The slave address options are shown in Figure 13.

Figure 13:
Slave Address Selection

ADDR SEL Terminal Level	Slave Address
GND	0101001
Float	0111001
V_{DD}	1001001

Note(s):

1. The Slave Addresses are 7 bits. A read/write bit should be appended to the slave address by the master device to properly communicate with the TSL2561 device.

Register Set

The TSL2561 is controlled and monitored by sixteen registers (three are reserved) and a Command Register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The Register Set is summarized in Figure 14.

Figure 14:
Register Address

Address	Register Name	Register Function
--	COMMAND	Specifies register address
0h	CONTROL	Control of basic functions
1h	TIMING	Integration time/gain control
2h	THRESHLOWLOW	Low byte of low interrupt threshold
3h	THRESHLOWHIGH	High byte of low interrupt threshold
4h	THRESHHIGHLOW	Low byte of high interrupt threshold
5h	THRESHHIGHHIGH	High byte of high interrupt threshold
6h	INTERRUPT	Interrupt control
7h	--	Reserved
8h	CRC	Factory test - not a user register
9h	--	Reserved
Ah	ID	Part number/Rev ID
Bh	--	Reserved
Ch	DATA0LOW	Low byte of ADC channel 0
Dh	DATA0HIGH	High byte of ADC channel 0
Eh	DATA1LOW	Low byte of ADC channel 1
Fh	DATA1HIGH	High byte of ADC channel 1

The mechanics of accessing a specific register depends on the specific I^2C protocol used. Refer to the section on I^2C protocols. In general, the Command Register is written first to specify the specific control/status register for following read/write operations.

Command Register

The Command Register specifies the address of the target register for subsequent read and write operations. The Send Byte protocol is used to configure the Command Register. The Command Register contains eight bits as described in Figure 15. The Command Register defaults to 00h at power on.

Figure 15:
Command Register

7	6	5	4	3	2	1	0
CMD	CLEAR	WORD	BLOCK	ADDRESS			

Field	Bit	Description
CMD	7	Select Command Register. Must write as 1.
CLEAR	6	Interrupt clear. Clears any pending interrupt. This bit is a write-one-to-clear bit. It is self clearing.
WORD	5	I^2C Write/Read Word Protocol. 1 indicates that this I^2C transaction is using either the I^2C Write Word or Read Word protocol.
BLOCK	4	Block Write/Read Protocol. 1 indicates that this transaction is using either the Block Write or the Block Read protocol.(1)
ADDRESS	3:0	Register Address. This field selects the specific control or status register for following write and read commands according to Figure 14.

Note(s):

1. An I^2C block transaction will continue until the Master sends a stop condition.

Control Register (0h)

The Control Register contains two bits and is primarily used to power the TSL2561 device up and down as shown in Figure 16.

Figure 16:
Control Register

7	6	5	4	3	2	1	0
Resv	Resv	Resv	Resv	Resv	Resv	POWER	

Field	Bit	Description
Resv	7:2	Reserved. Write as 0.
POWER	1:0	Power up/power down. By writing a 03h to this register, the device is powered up. By writing a 00h to this register, the device is powered down(1).

Note(s):

1. If a value of 03h is written, the value returned during a read cycle will be 03h. This feature can be used to verify that the device is communicating properly.

Timing Register (1h)

The Timing Register controls both the integration time and the gain of the ADC channels. A common set of control bits is provided that controls both ADC channels. The Timing Register defaults to 02h at power on.

Figure 17:
Timing Register

7	6	5	4	3	2	1	0
Resv	Resv	Resv	GAIN	Manual	Resv	INTEG	

Field	Bit	Description
Resv	7:5	Reserved. Write as 0.
GAIN	4	Switches gain between low gain and high gain modes. Writing a 0 selects low gain (1×); writing a 1 selects high gain (16×).
Manual	3	Manual timing control. Writing a 1 begins an integration cycle. Writing a 0 stops an integration cycle(1)
Resv	2	Reserved. Write as 0.
INTEG	1:0	Integrate time. This field selects the integration time for each conversion.

Note(s):

1. This field only has meaning when INTEG = 11. It is ignored at all other times.

Integration time is dependent on the INTEG FIELD VALUE and the internal clock frequency. Nominal integration times and respective scaling between integration times scale proportionally as shown in Figure 18. See Note4 and Note5 for detailed information regarding how the scale values were obtained; see Calculating Lux for further information on how to calculate lux.

Figure 18:
Integration Time

INTEG Field Value	Scale	Nominal Integration Time
00	0.034	13.7ms
01	0.252	101ms
10	1	402ms
11	--	N/A

The manual timing control feature is used to manually start and stop the integration time period. If a particular integration time period is required that is not listed in Figure 18, then this feature can be used. For example, the manual timing control can be used to synchronize the TSL256x device with an external light source (e.g. LED). A start command to begin integration can be initiated by writing a 1 to this bit field. Correspondingly, the integration can be stopped by simply writing a 0 to the same bit field.

Interrupt Threshold Register (2h – 5h)

The Interrupt Threshold registers store the values to be used as the high and low trigger points for the comparison function for interrupt generation. If the value generated by channel 0 crosses below or is equal to the low threshold specified, an interrupt is asserted on the interrupt pin. If the value generated by channel 0 crosses above the high threshold specified, an interrupt is asserted on the interrupt pin. Registers THRESHLOWLOW and THRESHLOWHIGH provide the low byte and high byte, respectively, of the lower interrupt threshold. Registers THRESHHIGHLOW and THRESHHIGHHIGH provide the low and high bytes, respectively, of the upper interrupt threshold. The high and low bytes from each set of registers are combined to form a 16-bit threshold value. The interrupt threshold registers default to 00h on power up.

Figure 19:
Interrupt Threshold Register

Register	Address	Bits	Description
THRESHLOWLOW	2h	7:0	ADC channel 0 lower byte of the low threshold
THRESHLOWHIGH	3h	7:0	ADC channel 0 upper byte of the low threshold
THRESHHIGHLOW	4h	7:0	ADC channel 0 lower byte of the high threshold
THRESHHIGHHIGH	5h	7:0	ADC channel 0 upper byte of the high threshold

Note(s):

1. Since two 8-bit values are combined for a single 16-bit value for each of the high and low interrupt thresholds, the Send Byte protocol should not be used to write to these registers. Any values transferred by the Send Byte protocol with the MSB set would be interpreted as the COMMAND field and stored as an address for subsequent read/write operations and not as the interrupt threshold information as desired. The Write Word protocol should be used to write byte-paired registers. For example, the THRESHLOWLOW and THRESHLOWHIGH registers (as well as the THRESHHIGHLOW and THRESHHIGHHIGH registers) can be written together to set the 16-bit ADC value in a single transaction.

Interrupt Control Register (6h)

The Interrupt Register controls the extensive interrupt capabilities of the TSL2561.The interrupt persist bit field (PERSIST) provides control over when interrupts occur. A value of 0 causes an interrupt to occur after every integration cycle regardless of the threshold settings. A value of 1 results in an interrupt after one integration time period outside the threshold window. A value of *N* (where *N* is 2 through15) results in an interrupt only if the value remains outside the threshold window for *N* consecutive integration cycles. For example, if *N* is equal to 10 and the integration time is 402ms, then the total time is approximately 4 seconds.

When a level Interrupt is selected, an interrupt is generated whenever the last conversion results in a value outside of the programmed threshold window. The interrupt is active-low and remains asserted until cleared by writing the Command Register with the CLEAR bit set.

Note(s): Interrupts are based on the value of Channel 0 only.

Figure 20:
Interrupt Control Register

7	6	5	4	3	2	1	0
Resv	Resv	INTR		PERSIST			

Field	Bits	Description
Resv	7:6	Reserved. Write as 0.
INTR	5:4	INTR Control Select. This field determines mode of interrupt logic according to Figure 21, below.

Field	Bits	Description
PERSIST	3:0	Interrupt persistence. Controls rate of interrupts to the host processor as shown in Figure 22, below.

Figure 21:
Interrupt Control Select

INTR Field Value	Read Value
00	Interrupt output disabled
01	Level Interrupt
10	Reserved
11	Test Mode: Sets interrupt and functions as mode 10

Note(s):

1. Field value of 11 may be used to test interrupt connectivity in a system or to assist in debugging interrupt service routine software.

Figure 22:
Interrupt Persistence Select

Persist Field Value	Interrupt Persist Function
0000	Every ADC cycle generates interrupt
0001	Any value outside of threshold range
0010	2 integration time periods out of range
0011	3 integration time periods out of range
0100	4 integration time periods out of range
0101	5 integration time periods out of range
0110	6 integration time periods out of range
0111	7 integration time periods out of range
1000	8 integration time periods out of range
1001	9 integration time periods out of range
1010	10 integration time periods out of range
1011	11 integration time periods out of range
1100	12 integration time periods out of range
1101	13 integration time periods out of range
1110	14 integration time periods out of range
1111	15 integration time periods out of range

ID Register (Ah)

The ID Register provides the value for both the part number and silicon revision number for that part number. It is a read-only register, whose value never changes.

Figure 23:
ID Register

7	6	5	4	3	2	1	0
PARTNO				REVNO			

Field	Bits	Description	
PARTNO	7:4	Part Number Identification:	
		Field Value	**Device Number**
		0101	TSL2561T
REVNO	3:0	Revision number identification	

ADC Channel Data Registers (Ch – Fh)

The ADC channel data are expressed as 16-bit values spread across two registers. The ADC channel 0 data registers, DATA0LOW and DATA0HIGH provide the lower and upper bytes, respectively, of the ADC value of channel 0. Registers DATA1LOW and DATA1HIGH provide the lower and upper bytes, respectively, of the ADC value of channel 1. All channel data registers are read-only and default to 00h on power up.

Figure 24:
ADC Channel Data Registers

Register	Address	Bits	Description
DATA0LOW	Ch	7:0	ADC channel 0 lower byte
DATA0HIGH	Dh	7:0	ADC channel 0 upper byte
DATA1LOW	Eh	7:0	ADC channel 1 lower byte
DATA1HIGH	Fh	7:0	ADC channel 1 upper byte

The upper byte data registers can only be read following a read to the corresponding lower byte register. When the lower byte register is read, the upper eight bits are strobed into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

Note(s): The Read Word protocol can be used to read byte-paired registers. For example, the DATA0LOW and DATA0HIGH registers (as well as the DATA1LOW and DATA1HIGH registers) may be read together to obtain the 16-bit ADC value in a single transaction.

Device Operation

Basic Operation

After applying V_{DD}, the device will initially be in the power-down state. To operate the device, issue a command to access the Control Register followed by the data value 03h to power up the device. At this point, both ADC channels will begin a conversion at the default integration time of 400ms. After 400ms, the conversion results will be available in the DATA0 and DATA1 registers.

Configuring the Timing Register

The command, timing, and control registers are initialized to default values on power up. Setting these registers to the desired values would be part of a normal initialization or setup procedure. In addition, to maximize the performance of the device under various conditions, the integration time and gain may be changed often during operation.

Interrupts

The interrupt feature of the TSL2561 device simplifies and improves system efficiency by eliminating the need to poll the sensor for a light intensity value. Interrupt styles are determined by the INTR field in the Interrupt Register. The interrupt feature may be disabled by writing a field value of 00h to the Interrupt Control Register so that polling can be performed.

The versatility of the interrupt feature provides many options for interrupt configuration and usage. The primary purpose of the interrupt function is to provide a *meaningful change* in light intensity. However, it also be used as an end-of-conversion signal. The concept of a *meaningful* change can be defined by the user both in terms of light intensity and time, or persistence, of that change in intensity. The TSL2561 device implements two 16-bit-wide interrupt threshold registers that allow the user to define a threshold above and below the current light level. An interrupt will then be generated when the value of a conversion exceeds either of these limits. For simplicity of programming, the threshold comparison is accomplished only with Channel 0. This simplifies calculation of thresholds that are based, for example, on a percent of the current light level. It is adequate to use only one channel when calculating light intensity differences since, for a given light source, the channel 0 and channel 1 values are linearly proportional to each other and thus both values scale linearly with light intensity.

To further control when an interrupt occurs, the TSL2561 device provides an interrupt persistence feature. This feature allows the user to specify a number of conversion cycles for which a light intensity exceeding either interrupt threshold must persist before actually generating an interrupt. This can be used to

prevent transient changes in light intensity from generating an unwanted interrupt. With a value of 1, an interrupt occurs immediately whenever either threshold is exceeded. With values of *N*, where *N* can range from 2 to 15, *N* consecutive conversions must result in values outside the interrupt window for an interrupt to be generated. For example, if *N* is equal to 10 and the integration time is 402ms, then an interrupt will not be generated unless the light level persists for more than 4 seconds outside the threshold.

An interrupt is cleared by setting the CLEAR bit (bit 6) in the Command Register.

To configure the interrupt as an end-of-conversion signal, the interrupt PERSIST field is set to 0. An interrupt will be generated upon completion of each conversion. The interrupt threshold registers are ignored.

In order to generate an interrupt on demand during system test or debug, a test mode (INTR = 11) can be used.

Calculating Lux

The TSL2561 is intended for use in ambient light detection applications such as display backlight control, where adjustments are made to display brightness or contrast based on the brightness of the ambient light, as perceived by the human eye. Conventional silicon detectors respond strongly to infrared light, which the human eye does not see. This can lead to significant error when the infrared content of the ambient light is high, such as with incandescent lighting, due to the difference between the silicon detector response and the brightness perceived by the human eye.

This problem is overcome in the TSL2561 through the use of two photodiodes. One of the photodiodes (channel 0) is sensitive to both visible and infrared light, while the second photodiode (channel 1) is sensitive primarily to infrared light. An integrating ADC converts the photodiode currents to digital outputs. Channel 1 digital output is used to compensate for the effect of the infrared component of light on the channel 0 digital output. The ADC digital outputs from the two channels are used in a formula to obtain a value that approximates the human eye response in the commonly used Illuminance unit of Lux:

T Package

For $0 < CH1/CH0 \leq 0.50$

$Lux = 0.0304 \times CH0 - 0.062 \times CH0 \times ((CH1/CH0)^{1.4})$

For $0.50 < CH1/CH0 \leq 0.61$

$Lux = 0.0224 \times CH0 - 0.031 \times CH1$

For $0.61 < CH1/CH0 \leq 0.80$

$Lux = 0.0128 \times CH0 - 0.0153 \times CH1$

For $0.80 < CH1/CH0 \leq 1.30$

$Lux = 0.00146 \times CH0 - 0.00112 \times CH1$

For $CH1/CH0 > 1.30$

$Lux = 0$

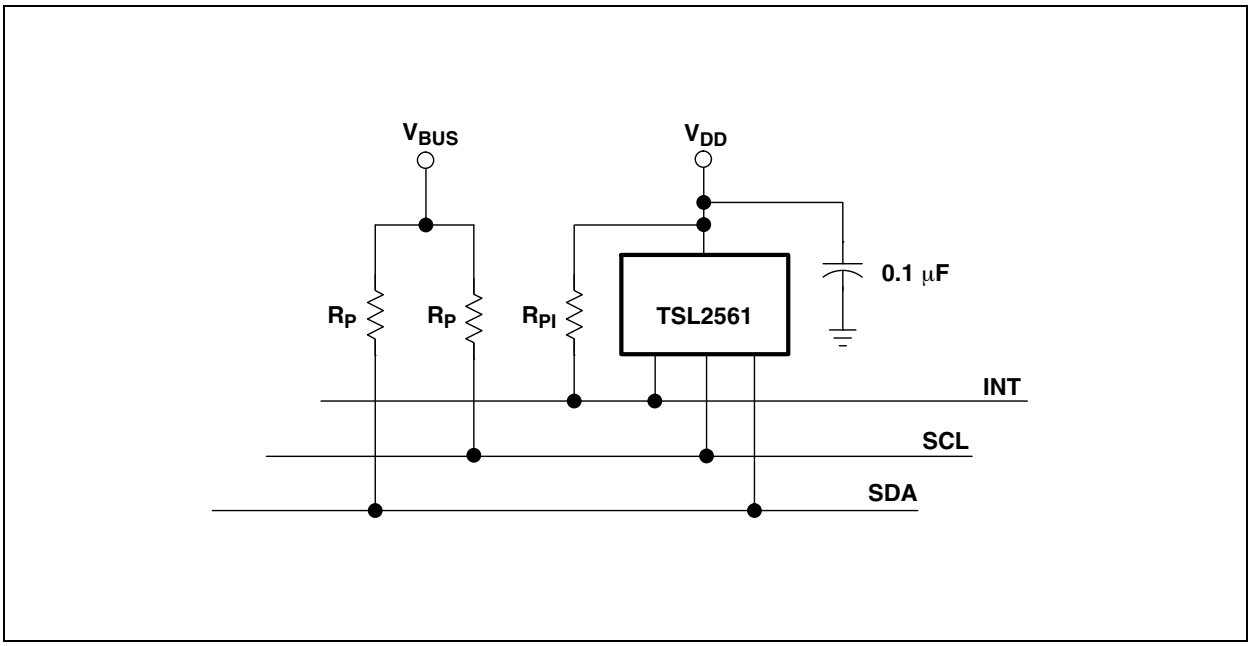
The formulas shown above were obtained by optical testing with fluorescent and incandescent light sources, and apply only to open-air applications. Optical apertures (e.g. light pipes) will affect the incident light on the device.

Application Information: Hardware

Power Supply Decoupling and Application Hardware Circuit

The power supply lines must be decoupled with a 0.1µF capacitor placed as close to the device package as possible (Figure 25). The bypass capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents caused by internal logic switching.

Figure 25:
Bus Pull-Up Resistors



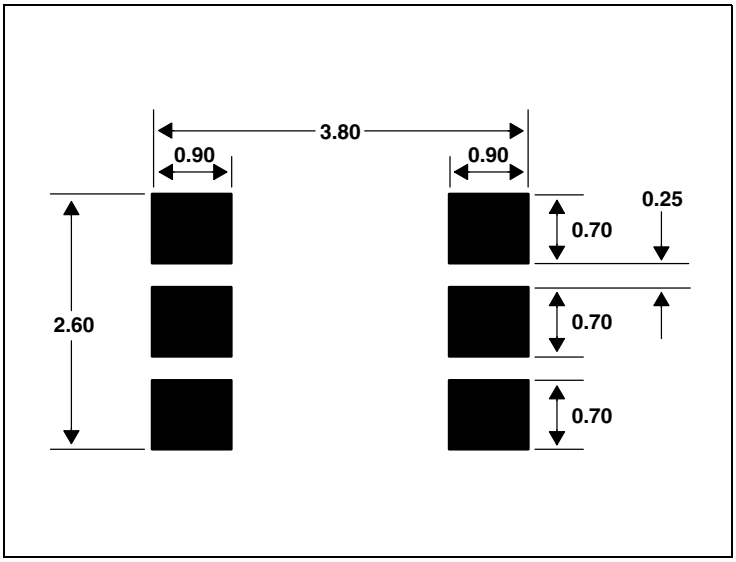
Pull-up resistors (R_p) maintain the SDAH and SCLH lines at a *high* level when the bus is free and ensure the signals are pulled up from a low to a high level within the required rise time. For a complete description of I^2C maximum and minimum R_p values, please review the I^2C Specification at http://www.nxp.com.

A pull-up resistor (RPI) is also required for the interrupt (INT), which functions as a wired-AND signal in a similar fashion to the SCL and SDA lines. A typical impedance value between 10kΩ and 100kΩ can be used. Please note that while Figure 25 shows INT being pulled up to V_{DD}, the interrupt can optionally be pulled up to V_{BUS}.

PCB Pad Layout

Suggested PCB pad layout guidelines for the TMB-6 (T) surface mount package is shown in Figure 26.

Figure 26:
Suggested T Package PCB Layout

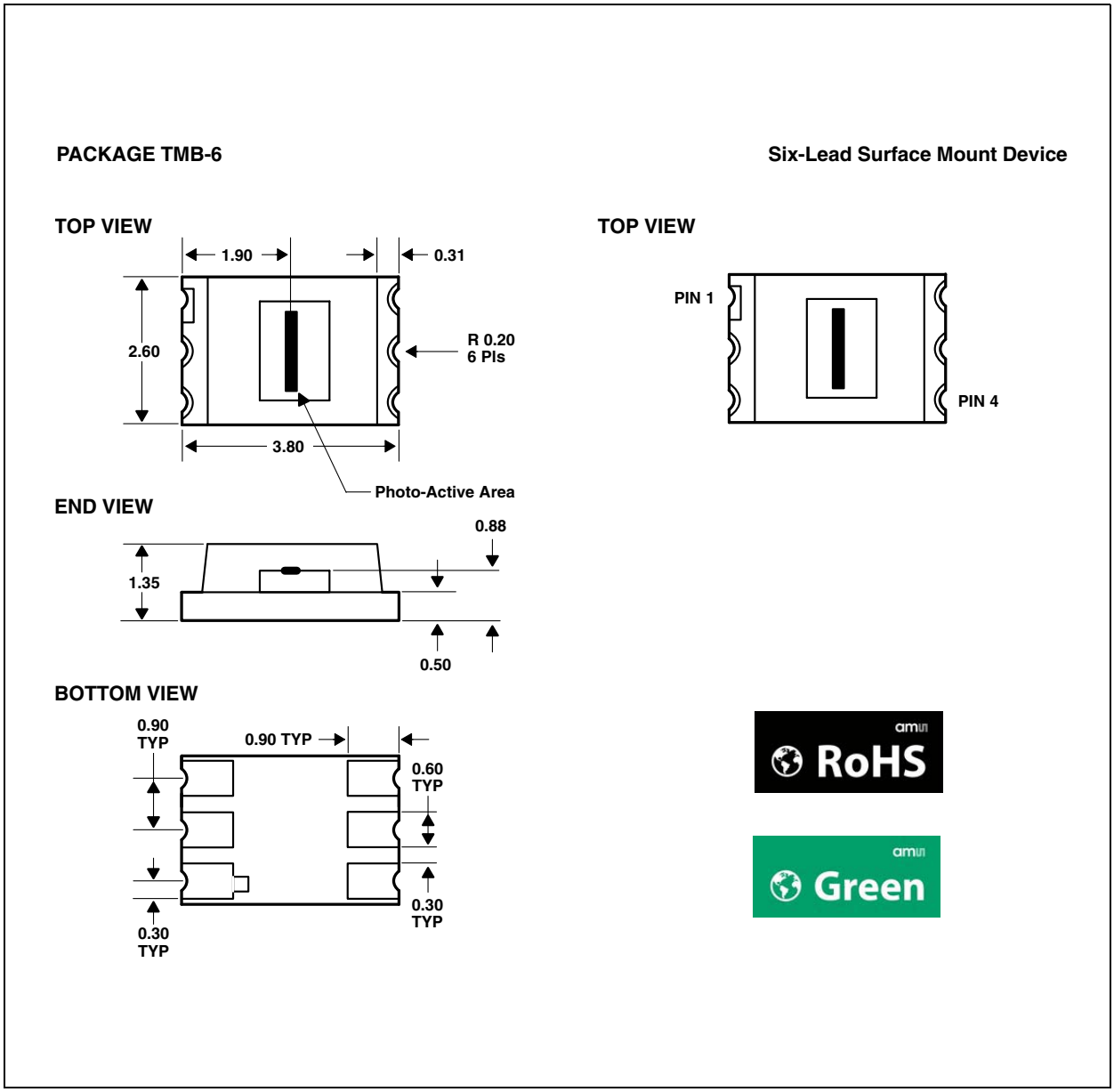


Note(s):

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

Packaging Mechanical Data

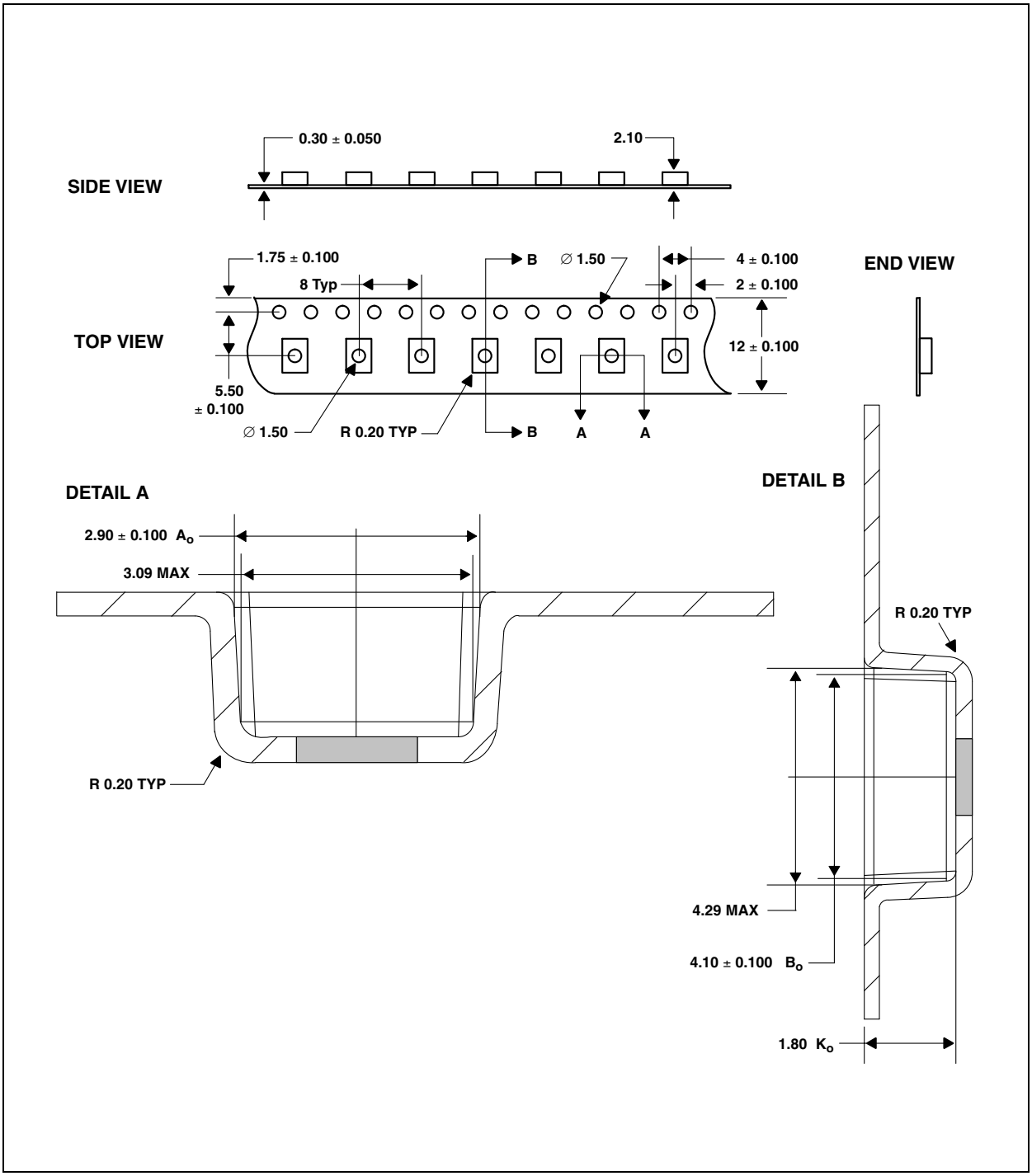
Figure 27:
Package T - Six-Lead TMB Plastic Surface Mount Packaging Configuration



Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ±0.20mm unless otherwise noted.
2. The photo-active area is 1398µm by 203µm.
3. Package top surface is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.55.
4. Contact finish is 0.5µm minimum of soft gold plated over a 18µm thick copper foil pattern with a 5µm to 9µm nickel barrier.
5. The underside of the package includes copper traces used to connect the pads during package substrate fabrication. Accordingly, exposed traces and vias should not be placed under the footprint of the TMB package in a PCB layout.
6. This package contains no lead (Pb).
7. This drawing is subject to change without notice.

Figure 28:
TSL2561 TMB Carrier Tape



Note(s):

1. All linear dimensions are in millimeters.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing A_o, B_o, and K_o are defined in ANSI EIA Standard 481-B 2001.
4. Each reel is 178 millimeters in diameter and contains 1000 parts.
5. **ams** AG packaging tape and reel conform to the requirements of EIA Standard 481-B.
6. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.

Manufacturing Information

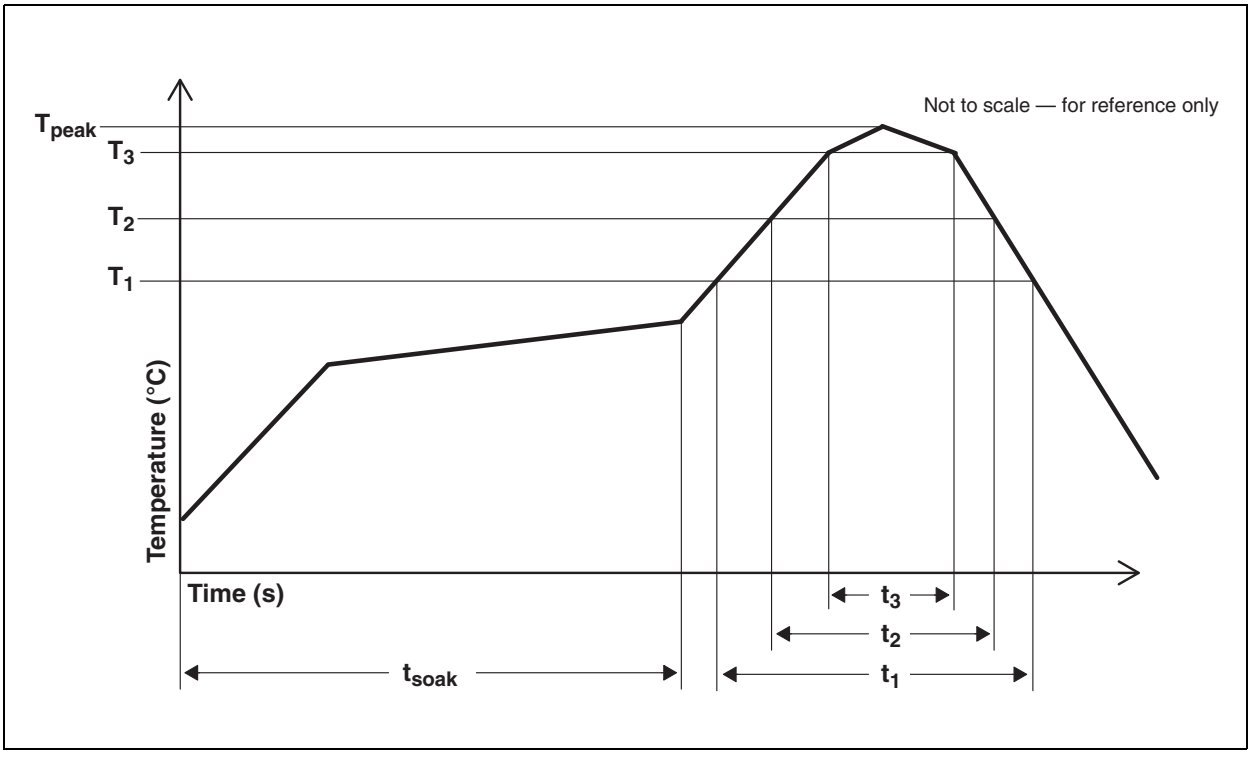
The T packages have been tested and have demonstrated an ability to be reflow soldered to a PCB substrate. The process, equipment, and materials used in these test are detailed below.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 29:
TSL2561 Solder Reflow Profile

Parameter	Reference	TSL2561
Average temperature gradient in preheating		2.5°C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217°C	t_1	Max 60 s
Time above 230°C	t_2	Max 50 s
Time above T_{peak} -10°C	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	260° C (-0°C/+5°C)
Temperature gradient in cooling		Max -5°C/s

Figure 30:
TSL2561 Solder Reflow Profile Graph



Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package molding compound. To ensure the package molding compound contains the smallest amount of absorbed moisture possible, each device is dry-baked prior to being packed for shipping. Devices are packed in a sealed aluminized envelope with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

The T package have been assigned a moisture sensitivity level of MSL 3 and the devices should be stored under the following conditions:

- Temperature Range: 5°C to 50°C
- Relative Humidity: 60% maximum
- Total Time: 6 months from the date code on the aluminized envelope - if unopened
- Opened Time: 168 hours or fewer

Rebaking will be required if the devices have been stored unopened for more than 6 months or if the aluminized envelope has been open for more than 168 hours. If rebaking is required, it should be done at 90°C for 4 hours.

Ordering & Contact Information

Figure 31:
Ordering Information

Ordering Code	Device	Interface	Package - Leads	Package Designator
TSL2561T	TSL2561	I^2C	TMB-6	T

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Revision Information

Changes from 1-00 (2016-May-05) to current revision 1-01 (2018-Apr-23)	Page
Removed all instances of TSL2560CS/T/FN/CL and TSL2561CS/FN/CL	
Updated Figure 4	5
Removed I^2C Protocols including figures	
Updated text under Figure 14 (Replaced all instances of SMBus with I^2C)	14
Updated Figure 15 and notes under it (Replaced all instances of SMB with I^2C)	15
Updated text under Interrupt Control Register (6h)	18
Updated Figure 21	19
Renamed “Application Information: Software” to “Device Operation”	22
Removed pseudo code under Basic Operation	22
Removed pseudo code under Configuring the Timing Register	22
Updated text and removed pseudo code under Interrupts	22
Removed Simplified Lux Calculation including pseudo code	

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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